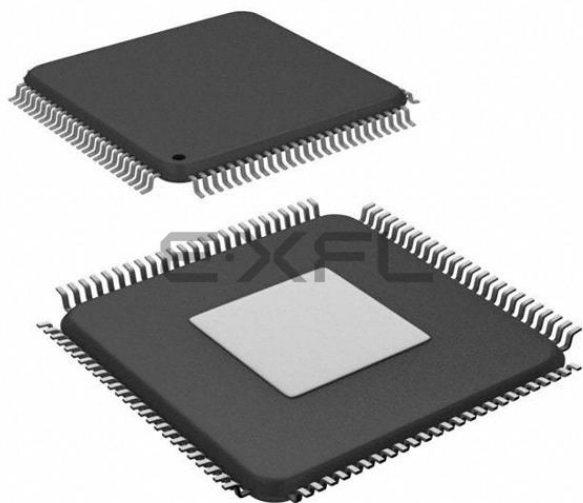




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Details

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	18K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe164gn-16f80l-aa

XE164xN Data Sheet

Revision History: V1.4 2013-02

Previous Versions:

V1.3, 2011-07

V1.2, 2010-04

V1.1, 2009-07

V1.0, 2009-03 Preliminary

Page	Subjects (major changes since last revision)
36	Added AB step marking.
87	Errata SWD_X.P002 implemented: V_{SWD} tolerance boundaries for 5.5 V are changed.
89	Clarified "Coding of bit fields LEVxV" descriptions. Matched with Operating Conditions: marked some coding values "out of valid operation range".
90	Errata FLASH_X.P001 implemented: Test Condition for Flash parameter N_{ER} corrected

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Summary of Features

1.2 Definition of Feature Variants

The XE164xN types are offered with several Flash memory sizes. [Table 2](#) and [Table 3](#) describe the location of the available Flash memory.

Table 2 Continuous Flash Memory Ranges

Total Flash Size	1st Range ¹⁾	2nd Range	3rd Range
320 Kbytes	C0'0000 _H ... C0'FFFF _H	C1'0000 _H ... C4'FFFF _H	n.a.
192 Kbytes	C0'0000 _H ... C0'FFFF _H	C1'0000 _H ... C1'FFFF _H	C4'0000 _H ... C4'FFFF _H
128 Kbytes	C0'0000 _H ... C0'FFFF _H	C4'0000 _H ... C4'FFFF _H	n.a.

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

Table 3 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0 ¹⁾	Flash 1
320	256	64
192	128	64
128	64	64

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

The XE164xN types are offered with different interface options. [Table 4](#) lists the available channels for each option.

Table 4 Interface Channel Association

Total Number	Available Channels / Message Objects
6 ADC0 channels	CH0, CH2 ... CH5, CH8
11 ADC0 channels	CH0, CH2 ... CH5, CH8 ... CH11, CH13, CH15
5 ADC1 channels	CH0, CH2, CH4 ... CH6
2 CAN nodes	CAN0, CAN1 64 message objects
4 serial channels	U0C0, U0C1, U1C0, U1C1
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1

Summary of Features

The XE164xN types are offered with several SRAM memory sizes. **Figure 1** shows the allocation rules for PSRAM and DSRAM. Note that the rules differ:

- PSRAM allocation starts from the **lower** address
- DSRAM allocation starts from the **higher** address

For example 8 Kbytes of PSRAM will be allocated at E0'0000h-E0'1FFFh and 8 Kbytes of DSRAM will be at 00'C000h-00'DFFFh.

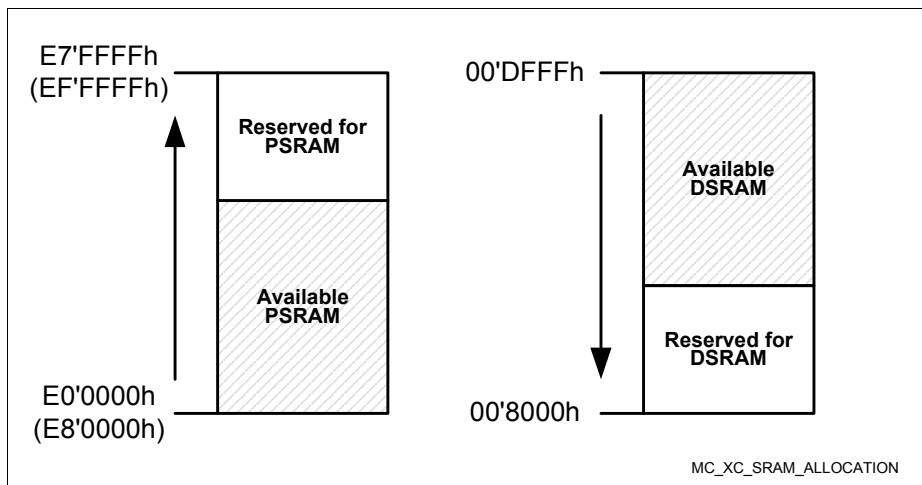


Figure 1 **SRAM Allocation**

General Device Information

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
6	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output
	T3OUT	O1	St/B	GPT12E Timer T3 Toggle Latch Output
	T6OUT	O2	St/B	GPT12E Timer T6 Toggle Latch Output
	TDO_A	OH / IH	St/B	JTAG Test Data Output / DAP1 Input/Output If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	ESR2_1	I	St/B	ESR2 Trigger Input 1
7	P7.3	O0 / I	St/B	Bit 3 of Port 7, General Purpose Input/Output
	EMUX1	O1	St/B	External Analog MUX Control Output 1 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_DOUT	O3	St/B	USIC0 Channel 0 Shift Data Output
	TMS_C	IH	St/B	JTAG Test Mode Selection Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	U0C1_DX0F	I	St/B	USIC0 Channel 1 Shift Data Input
8	P7.1	O0 / I	St/B	Bit 1 of Port 7, General Purpose Input/Output
	EXTCLK	O1	St/B	Programmable Clock Signal Output
	BRKIN_C	I	St/B	OCDS Break Signal Input
9	P7.4	O0 / I	St/B	Bit 4 of Port 7, General Purpose Input/Output
	EMUX2	O1	St/B	External Analog MUX Control Output 2 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C1_SCLK OUT	O3	St/B	USIC0 Channel 1 Shift Clock Output
	TCK_C	IH	St/B	DAP0/JTAG Clock Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	U0C0_DX0D	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX1E	I	St/B	USIC0 Channel 1 Shift Clock Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
44	P4.1	O0 / I	St/B	Bit 1 of Port 4, General Purpose Input/Output
	CC2_CC25	O3 / I	St/B	CAPCOM2 CC25IO Capture Inp./ Compare Out.
	CS1	OH	St/B	External Bus Interface Chip Select 1 Output
	T4EUDB	I	St/B	GPT12E Timer T4 External Up/Down Control Input
	ESR1_8	I	St/B	ESR1 Trigger Input 8
45	P2.4	O0 / I	St/B	Bit 4 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CC2_CC17	O3 / I	St/B	CAPCOM2 CC17IO Capture Inp./ Compare Out.
	A17	OH	St/B	External Bus Interface Address Line 17
	ESR1_0	I	St/B	ESR1 Trigger Input 0
	U0C0_DX0F	I	St/B	USIC0 Channel 0 Shift Data Input
46	RxDC1A	I	St/B	CAN Node 1 Receive Data Input
	P2.5	O0 / I	St/B	Bit 5 of Port 2, General Purpose Input/Output
	U0C0_SCLK OUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CC2_CC18	O3 / I	St/B	CAPCOM2 CC18IO Capture Inp./ Compare Out.
	A18	OH	St/B	External Bus Interface Address Line 18
	U0C0_DX1D	I	St/B	USIC0 Channel 0 Shift Clock Input
47	ESR1_10	I	St/B	ESR1 Trigger Input 10
	P4.2	O0 / I	St/B	Bit 2 of Port 4, General Purpose Input/Output
	CC2_CC26	O3 / I	St/B	CAPCOM2 CC26IO Capture Inp./ Compare Out.
	CS2	OH	St/B	External Bus Interface Chip Select 2 Output
	T2INA	I	St/B	GPT12E Timer T2 Count/Gate Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
87	P1.3	O0 / I	St/B	Bit 3 of Port 1, General Purpose Input/Output
	U1C0_SELO 7	O2	St/B	USIC1 Channel 0 Select/Control 7 Output
	U2C0_SELO 4	O3	St/B	USIC2 Channel 0 Select/Control 4 Output
	A11	OH	St/B	External Bus Interface Address Line 11
	ESR2_4	I	St/B	ESR2 Trigger Input 4
89	P10.14	O0 / I	St/B	Bit 14 of Port 10, General Purpose Input/Output
	U1C0_SELO 1	O1	St/B	USIC1 Channel 0 Select/Control 1 Output
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	$\overline{\text{RD}}$	OH	St/B	External Bus Interface Read Strobe Output
	ESR2_2	I	St/B	ESR2 Trigger Input 2
	U0C1_DX0C	I	St/B	USIC0 Channel 1 Shift Data Input
90	P1.4	O0 / I	St/B	Bit 4 of Port 1, General Purpose Input/Output
	U1C1_SELO 4	O2	St/B	USIC1 Channel 1 Select/Control 4 Output
	U2C0_SELO 5	O3	St/B	USIC2 Channel 0 Select/Control 5 Output
	A12	OH	St/B	External Bus Interface Address Line 12
	U2C0_DX2B	I	St/B	USIC2 Channel 0 Shift Control Input
91	P10.15	O0 / I	St/B	Bit 15 of Port 10, General Purpose Input/Output
	U1C0_SELO 2	O1	St/B	USIC1 Channel 0 Select/Control 2 Output
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U1C0_DOUT	O3	St/B	USIC1 Channel 0 Shift Data Output
	ALE	OH	St/B	External Bus Interf. Addr. Latch Enable Output
	U0C1_DX1C	I	St/B	USIC0 Channel 1 Shift Clock Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
92	P1.5	O0 / I	St/B	Bit 5 of Port 1, General Purpose Input/Output
	U1C1_SELO3	O2	St/B	USIC1 Channel 1 Select/Control 3 Output
	BRKOUT	O3	St/B	OCDS Break Signal Output
	A13	OH	St/B	External Bus Interface Address Line 13
	U2C0_DX0C	I	St/B	USIC2 Channel 0 Shift Data Input
93	P1.6	O0 / I	St/B	Bit 6 of Port 1, General Purpose Input/Output
	U1C1_SELO2	O2	St/B	USIC1 Channel 1 Select/Control 2 Output
	U2C0_DOUT	O3	St/B	USIC2 Channel 0 Shift Data Output
	A14	OH	St/B	External Bus Interface Address Line 14
	U2C0_DX0D	I	St/B	USIC2 Channel 0 Shift Data Input
94	P1.7	O0 / I	St/B	Bit 7 of Port 1, General Purpose Input/Output
	U1C1_MCLKOUT	O2	St/B	USIC1 Channel 1 Master Clock Output
	U2C0_SCLKOUT	O3	St/B	USIC2 Channel 0 Shift Clock Output
	A15	OH	St/B	External Bus Interface Address Line 15
	U2C0_DX1C	I	St/B	USIC2 Channel 0 Shift Clock Input
95	XTAL2	O	Sp/M	Crystal Oscillator Amplifier Output
96	XTAL1	I	Sp/M	Crystal Oscillator Amplifier Input To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Voltages on XTAL1 must comply to the core supply voltage V_{DDIM} .
	ESR2_9	I	St/B	ESR2 Trigger Input 9
97	PORST	I	In/B	Power On Reset Input A low level at this pin resets the XE164xN completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pull-up device will hold this pin high when nothing is driving it.

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
2, 25, 27, 50, 52, 75, 77, 100	V_{DDPB}	-	PS/B	Digital Pad Supply Voltage for Domain B Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. <i>Note: The on-chip voltage regulators and all ports except P5, P6 and P15 are fed from supply voltage V_{DDPB}.</i>
1, 26, 51, 76	V_{SS}	-	PS/--	Digital Ground All V_{SS} pins must be connected to the ground-line or ground-plane. <i>Note: Also the exposed pad is connected internally to V_{SS}. To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground. For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.</i>

- 1) To generate the reference clock output for bus timing measurement, f_{SYS} must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.

3.1 Memory Subsystem and Organization

The memory space of the XE164xN is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 7 XE164xN Memory Map ¹⁾

Address Area	Start Loc.	End Loc.	Area Size ²⁾	Notes
IMB register space	FF'FF00 _H	FF'FFFF _H	256 Bytes	
Reserved	F0'0000 _H	FF'FEFF _H	< 1 Mbyte	Minus IMB registers
Reserved for EPSRAM	E8'4000 _H	EF'FFFF _H	496 Kbytes	Mirrors EPSRAM
Emulated PSRAM	E8'0000 _H	E8'3FFF _H	up to 16 Kbytes	With Flash timing
Reserved for PSRAM	E0'4000 _H	E7'FFFF _H	496 Kbytes	Mirrors PSRAM
PSRAM	E0'0000 _H	E0'3FFF _H	up to 16 Kbytes	Program SRAM
Reserved for Flash	C5'0000 _H	DF'FFFF _H	1,728 Kbytes	
Flash 1	C4'0000 _H	C4'FFFF _H	64 Kbytes	
Flash 0	C0'0000 _H	C3'FFFF _H	256 Kbytes ³⁾	Minus res. seg.
External memory area	40'0000 _H	BF'FFFF _H	8 Mbytes	
External IO area ⁴⁾	21'0000 _H	3F'FFFF _H	1,984 Kbytes	
Reserved	20'BC00 _H	20'FFFF _H	17 Kbytes	
USIC0–2 alternate regs.	20'B000 _H	20'BBFF _H	3 Kbytes	Accessed via EBC
MultiCAN alternate regs.	20'8000 _H	20'AFFF _H	12 Kbytes	Accessed via EBC
Reserved	20'5800 _H	20'7FFF _H	10 Kbytes	
USIC0–2 registers	20'4000 _H	20'57FF _H	6 Kbytes	Accessed via EBC
Reserved	20'6800 _H	20'7FFF _H	6 Kbytes	
MultiCAN registers	20'0000 _H	20'3FFF _H	16 Kbytes	Accessed via EBC
External memory area	01'0000 _H	1F'FFFF _H	1984 Kbytes	
SFR area	00'FE00 _H	00'FFFF _H	0.5 Kbytes	
Dualport RAM (DPRAM)	00'F600 _H	00'FDFF _H	2 Kbytes	
Reserved for DPRAM	00'F200 _H	00'F5FF _H	1 Kbytes	
ESFR area	00'F000 _H	00'F1FF _H	0.5 Kbytes	
XSFR area	00'E000 _H	00'EFFF _H	4 Kbytes	
Data SRAM (DSRAM)	00'A000 _H	00'DFFF _H	16 Kbytes	

3.6 Interrupt System

The architecture of the XE164xN supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Using a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed. With the PEC just one cycle is 'stolen' from the current CPU activity to perform the PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XE164xN has eight PEC channels, each with fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of $7/11^{1)}$ CPU clocks, the XE164xN can react quickly to the occurrence of non-deterministic events.

Interrupt Nodes and Source Selection

The interrupt system provides 96 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

Trap Processing

The XE164xN provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called 'Hardware Traps'. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

¹⁾ Depending if the jump cache is used or not.

Functional Description

Table 8 Compare Modes (cont'd)

Compare Modes	Function
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

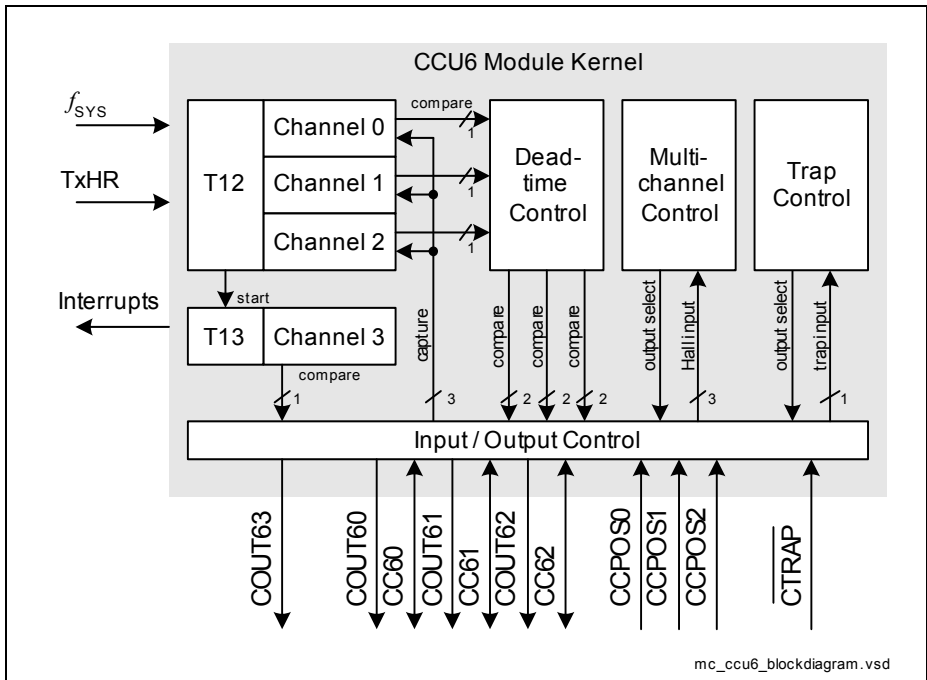


Figure 7 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

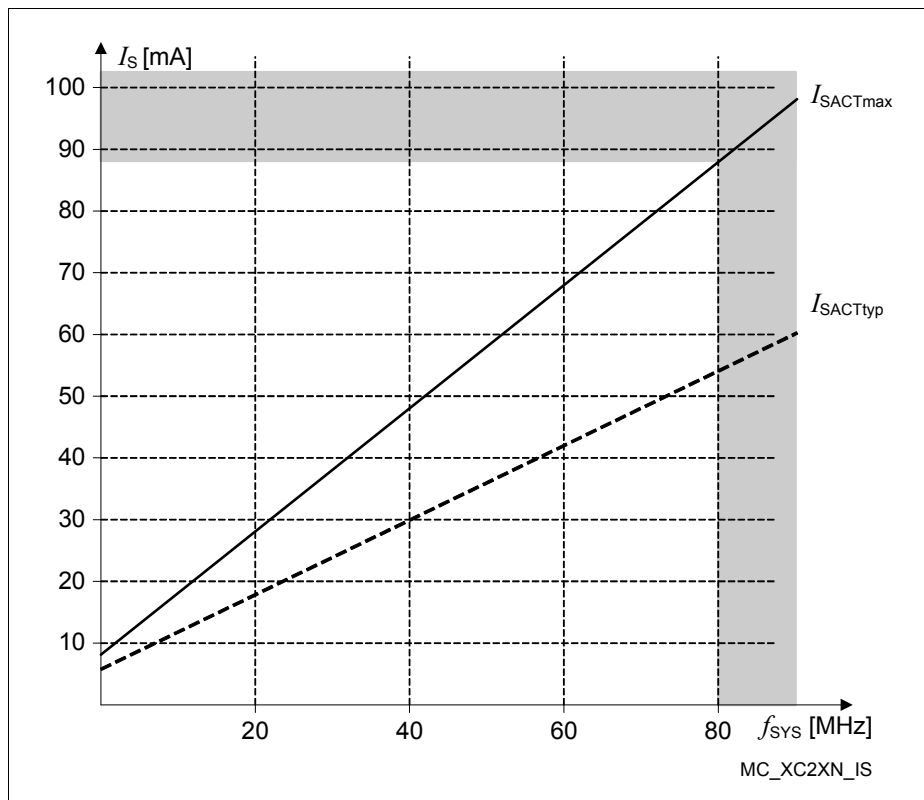


Figure 14 Supply Current in Active Mode as a Function of Frequency

Note: Operating Conditions apply.

Table 18 Leakage Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Leakage supply current ¹⁾	I_{LK1} CC	–	0.03	0.04	mA	$T_J = 25\text{ }^{\circ}\text{C}^{(1)}$
		–	0.5	1.2	mA	$T_J = 85\text{ }^{\circ}\text{C}^{(1)}$
		–	1.9	5.5	mA	$T_J = 125\text{ }^{\circ}\text{C}^{(1)}$
		–	3.9	12.2	mA	$T_J = 150\text{ }^{\circ}\text{C}^{(1)}$

¹⁾ All inputs (including pins configured as inputs) are set at 0 V to 0.1 V or at $V_{DDP} - 0.1$ V to V_{DDP} and all outputs (including pins configured as outputs) are disconnected.

Electrical Parameters

Sample time and conversion time of the XE164xN's A/D converters are programmable. The timing above can be calculated using [Table 20](#).

The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

Table 20 A/D Converter Computation Table

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}	INPCRx.7-0 (STC)	Sample Time¹⁾ t_s
000000 _B	f_{SYS}	00 _H	$t_{\text{ADCI}} \times 2$
000001 _B	$f_{\text{SYS}} / 2$	01 _H	$t_{\text{ADCI}} \times 3$
000010 _B	$f_{\text{SYS}} / 3$	02 _H	$t_{\text{ADCI}} \times 4$
:	$f_{\text{SYS}} / (\text{DIVA}+1)$	:	$t_{\text{ADCI}} \times (\text{STC}+2)$
111110 _B	$f_{\text{SYS}} / 63$	FE _H	$t_{\text{ADCI}} \times 256$
111111 _B	$f_{\text{SYS}} / 64$	FF _H	$t_{\text{ADCI}} \times 257$

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

Converter Timing Example A:

Assumptions: $f_{\text{SYS}} = 80 \text{ MHz}$ (i.e. $t_{\text{SYS}} = 12.5 \text{ ns}$), DIVA = 03_H, STC = 00_H

Analog clock $f_{\text{ADCI}} = f_{\text{SYS}} / 4 = 20 \text{ MHz}$, i.e. $t_{\text{ADCI}} = 50 \text{ ns}$

Sample time $t_s = t_{\text{ADCI}} \times 2 = 100 \text{ ns}$

Conversion 10-bit:

$$t_{\text{C10}} = 13 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 13 \times 50 \text{ ns} + 2 \times 12.5 \text{ ns} = 0.675 \mu\text{s}$$

Conversion 8-bit:

$$t_{\text{C8}} = 11 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 11 \times 50 \text{ ns} + 2 \times 12.5 \text{ ns} = 0.575 \mu\text{s}$$

Converter Timing Example B:

Assumptions: $f_{\text{SYS}} = 40 \text{ MHz}$ (i.e. $t_{\text{SYS}} = 25 \text{ ns}$), DIVA = 02_H, STC = 03_H

Analog clock $f_{\text{ADCI}} = f_{\text{SYS}} / 3 = 13.3 \text{ MHz}$, i.e. $t_{\text{ADCI}} = 75 \text{ ns}$

Sample time $t_s = t_{\text{ADCI}} \times 5 = 375 \text{ ns}$

Conversion 10-bit:

$$t_{\text{C10}} = 16 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 16 \times 75 \text{ ns} + 2 \times 25 \text{ ns} = 1.25 \mu\text{s}$$

Conversion 8-bit:

$$t_{\text{C8}} = 14 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 14 \times 75 \text{ ns} + 2 \times 25 \text{ ns} = 1.10 \mu\text{s}$$

4.5 System Parameters

The following parameters specify several aspects which are important when integrating the XE164xN into an application system.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 21 Various System Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Short-term deviation of internal clock source frequency ¹⁾	Δf_{INT} CC	-1	—	1	%	$\Delta T_J \leq 10^\circ\text{C}$
Internal clock source frequency	f_{INT} CC	4.8	5.0	5.2	MHz	
Wakeup clock source frequency ²⁾	f_{WU} CC	400	—	700	kHz	FREQSEL= 00
		210	—	390	kHz	FREQSEL= 01
		140	—	260	kHz	FREQSEL= 10
		110	—	200	kHz	FREQSEL= 11
Startup time from power-on with code execution from Flash	t_{SPO} CC	1.5	2.0	2.4	ms	$f_{\text{WU}} = 500 \text{ kHz}$
Startup time from stopover mode with code execution from PSRAM	t_{SSO} CC	11 / $f_{\text{WU}}^{3)}$	—	12 / $f_{\text{WU}}^{3)}$	μs	
Core voltage (PVC) supervision level	V_{PVC} CC	$V_{\text{LV}} - 0.03$	V_{LV}	$V_{\text{LV}} + 0.07^{4)}$	V	⁵⁾
Supply watchdog (SWD) supervision level	V_{SWD} CC	$V_{\text{LV}} - 0.10^{6)}$	V_{LV}	$V_{\text{LV}} + 0.15$	V	voltage_range= lower ⁵⁾
		$V_{\text{LV}} - 0.15$	V_{LV}	$V_{\text{LV}} + 0.15$	V	voltage_range= upper ⁵⁾
		$V_{\text{LV}} - 0.30$	V_{LV}	$V_{\text{LV}} + 0.30$	V	$V_{\text{LV}} = 5.5 \text{ V}^{5)}$

1) The short-term frequency deviation refers to a timeframe of a few hours and is measured relative to the current frequency at the beginning of the respective timeframe. This parameter is useful to determine a time span for re-triggering a LIN synchronization.

Electrical Parameters

Table 27 Standard Pad Parameters for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise and Fall times (10% - 90%)	t_{RF} CC	—	—	23 + 0.6 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Medium
		—	—	11.6 + 0.22 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Strong ; Driver_Edge= Medium
		—	—	4.2 + 0.14 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Strong ; Driver_Edge= Sharp
		—	—	20.6 + 0.22 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Strong ; Driver_Edge= Slow
		—	—	212 + 1.9 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Weak

1) An output current above $|I_{Oxnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and $\Sigma -I_{OH}$) must remain below 50 mA.

Electrical Parameters

Table 28 Standard Pad Parameters for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise and Fall times (10% - 90%)	t_{RF} CC	—	—	37 + 0.65 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Medium
		—	—	24 + 0.3 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Strong ; Driver_Edge= Medium
		—	—	6.2 + 0.24 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Strong ; Driver_Edge= Sharp
		—	—	34 + 0.3 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Strong ; Driver_Edge= Slow
		—	—	500 + 2.5 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Weak

1) An output current above $|I_{Oxnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and $\Sigma -I_{OH}$) must remain below 50 mA.

Table 32 External Bus Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output valid delay for $\overline{RD}$, $WR(L/H)$	t_{10} CC	–	11	20	ns	
Output valid delay for BHE, ALE	t_{11} CC	–	10	21	ns	
Address output valid delay for A23 ... A0	t_{12} CC	–	11	22	ns	
Address output valid delay for AD15 ... AD0 (MUX mode)	t_{13} CC	–	10	22	ns	
Output valid delay for $\overline{CS}$	t_{14} CC	–	10	13	ns	
Data output valid delay for AD15 ... AD0 (write data, MUX mode)	t_{15} CC	–	10	22	ns	
Data output valid delay for D15 ... D0 (write data, DEMUX mode)	t_{16} CC	–	10	22	ns	
Output hold time for $\overline{RD}$, $WR(L/H)$	t_{20} CC	-2	8	10	ns	
Output hold time for $\overline{BHE}$, ALE	t_{21} CC	-2	8	10	ns	
Address output hold time for AD15 ... AD0	t_{23} CC	-3	8	10	ns	
Output hold time for $\overline{CS}$	t_{24} CC	-3	8	11	ns	
Data output hold time for D15 ... D0 and AD15 ... AD0	t_{25} CC	-3	8	10	ns	
Input setup time for READY, D15 ... D0, AD15 ... AD0	t_{30} SR	29	17	–	ns	
Input hold time READY, D15 ... D0, AD15 ... AD0 ¹⁾	t_{31} SR	0	-9	–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of $\overline{RD}$. Address changes before the end of $\overline{RD}$ have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of $\overline{RD}$.

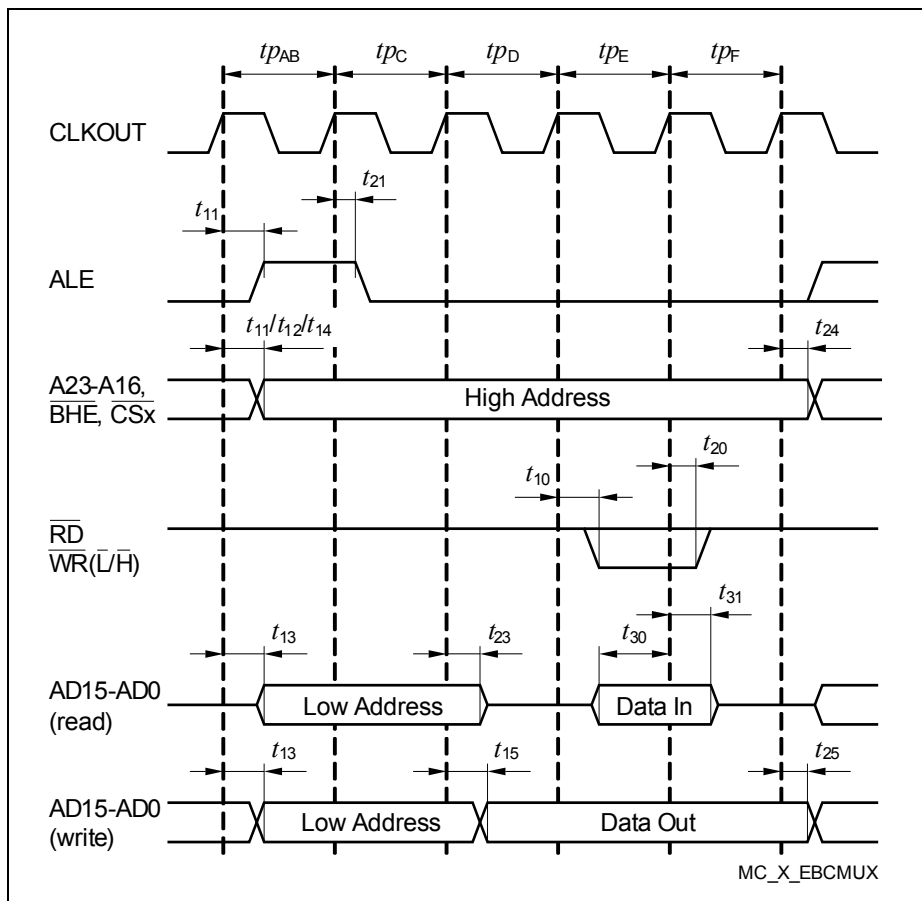


Figure 23 Multiplexed Bus Cycle

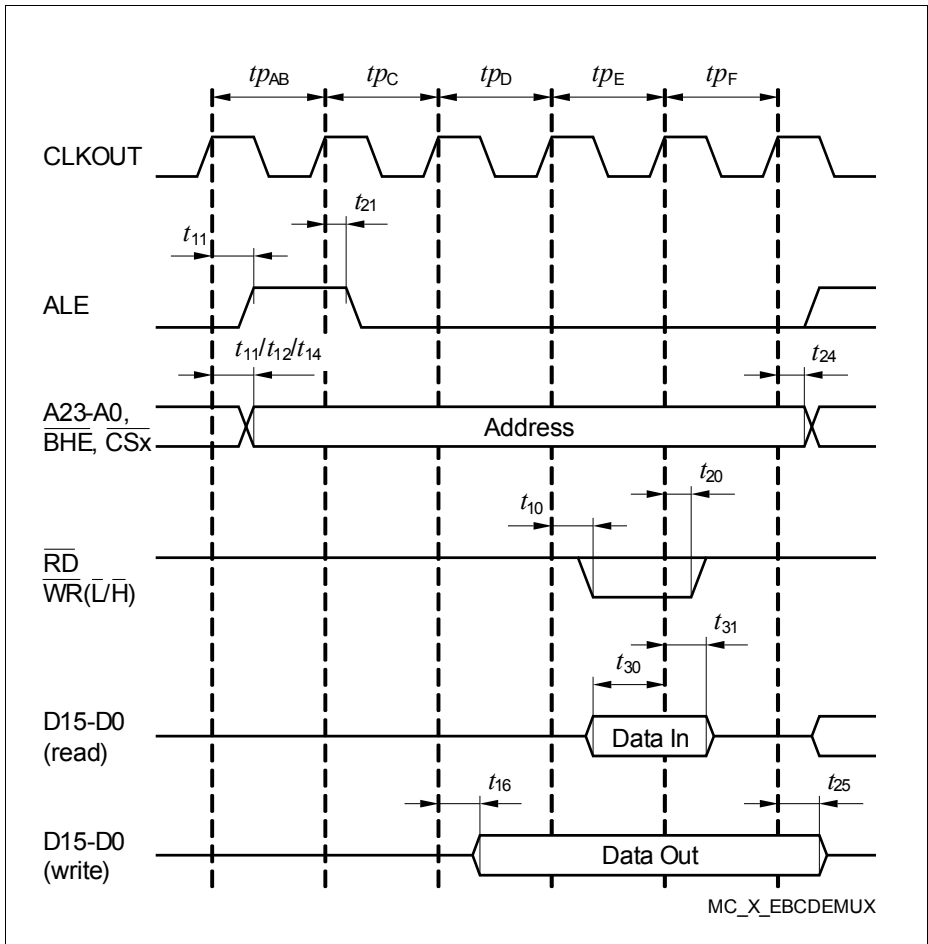


Figure 24 Demultiplexed Bus Cycle

4.7.5.1 Bus Cycle Control with the READY Input

The duration of an external bus cycle can be controlled by the external circuit using the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

An asynchronous READY signal puts no timing constraints on the input signal but incurs a minimum of one waitstate due to the additional synchronization stage. The minimum