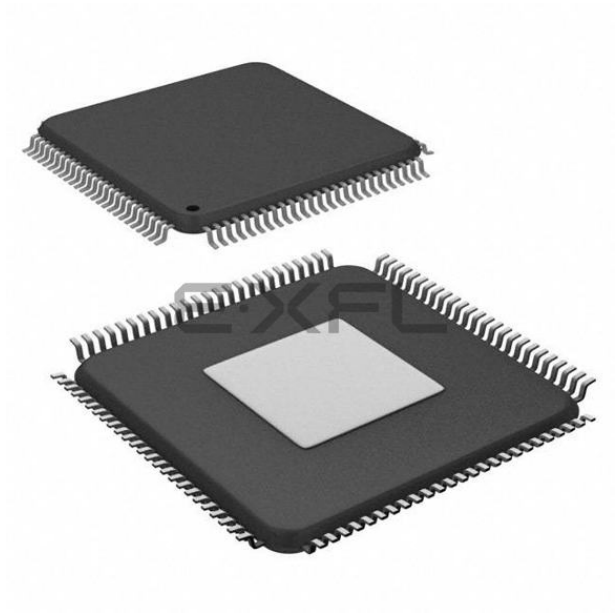
Infineon Technologies - SAF-XE164GN-24F80L AA Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	26K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe164gn-24f80l-aa

XE164xN Data Sheet
Revision History: V1.4 2013-02

Previous Versions:
V1.3, 2011-07
V1.2, 2010-04
V1.1, 2009-07
V1.0, 2009-03 Preliminary

Page	Subjects (major changes since last revision)
36	Added AB step marking.
87	Errata SWD_X.P002 implemented: V_{SWD} tolerance boundaries for 5.5 V are changed.
89	Clarified “Coding of bit fields LEVxV” descriptions. Matched with Operating Conditions: marked some coding values “out of valid operation range”.
90	Errata FLASH_X.P001 implemented: Test Condition for Flash parameter N_{ER} corrected

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- On-Chip Peripheral Modules
  - Two synchronizable A/D Converters with up to 16 channels, 10-bit resolution, conversion time below 1 µs, optional data preprocessing (data reduction, range check), broken wire detection
  - 16-channel general purpose capture/compare unit (CC2)
  - Two capture/compare units for flexible PWM signal generation (CCU6x)
  - Multi-functional general purpose timer unit with 5 timers
  - Up to 6 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
  - On-chip MultiCAN interface (Rev. 2.0B active) with 64 message objects (Full CAN/Basic CAN) on up to 2 CAN nodes and gateway functionality
  - On-chip system timer and on-chip real time clock
- Up to 12 Mbytes external address space for code and data
  - Programmable external bus characteristics for different address ranges
  - Multiplexed or demultiplexed external address/data buses
  - Selectable address bus width
  - 16-bit or 8-bit data bus width
  - Four programmable chip-select signals
- Single power supply from 3.0 V to 5.5 V
- Power reduction and wake-up modes
- Programmable watchdog timer and oscillator watchdog
- Up to 76 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via Device Access Port (DAP) or JTAG interface
- 100-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the temperature range:
  - SAF-…: -40°C to 85°C
  - SAK-…: -40°C to 125°C
- the package and the type of delivery.

For ordering codes for the XE164xN please contact your sales representative or local distributor.

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
54	P2.7	O0 / I	St/B	**Bit 7 of Port 2, General Purpose Input/Output**
	U0C1_SELO 0	O1	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	U0C0_SELO 1	O2	St/B	**USIC0 Channel 0 Select/Control 1 Output**
	CC2_CC20	O3 / I	St/B	**CAPCOM2 CC20IO Capture Inp./ Compare Out.**
	A20	OH	St/B	**External Bus Interface Address Line 20**
	U0C1_DX2C	I	St/B	**USIC0 Channel 1 Shift Control Input**
	RxDC1C	I	St/B	**CAN Node 1 Receive Data Input**
	ESR2_7	I	St/B	**ESR2 Trigger Input 7**
55	P0.1	O0 / I	St/B	**Bit 1 of Port 0, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CCU61_CC6 1	O3	St/B	**CCU61 Channel 1 Output**
	A1	OH	St/B	**External Bus Interface Address Line 1**
	U1C0_DX0B	I	St/B	**USIC1 Channel 0 Shift Data Input**
	CCU61_CC6 1INA	I	St/B	**CCU61 Channel 1 Input**
	U1C0_DX1A	I	St/B	**USIC1 Channel 0 Shift Clock Input**
56	P2.8	O0 / I	DP/B	**Bit 8 of Port 2, General Purpose Input/Output**
	U0C1_SCLK OUT	O1	DP/B	**USIC0 Channel 1 Shift Clock Output**
	EXTCLK	O2	DP/B	**Programmable Clock Signal Output** [1]
	CC2_CC21	O3 / I	DP/B	**CAPCOM2 CC21IO Capture Inp./ Compare Out.**
	A21	OH	DP/B	**External Bus Interface Address Line 21**
	U0C1_DX1D	I	DP/B	**USIC0 Channel 1 Shift Clock Input**

3 Functional Description

The architecture of the XE164xN combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources. This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XE164xN.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XE164xN.

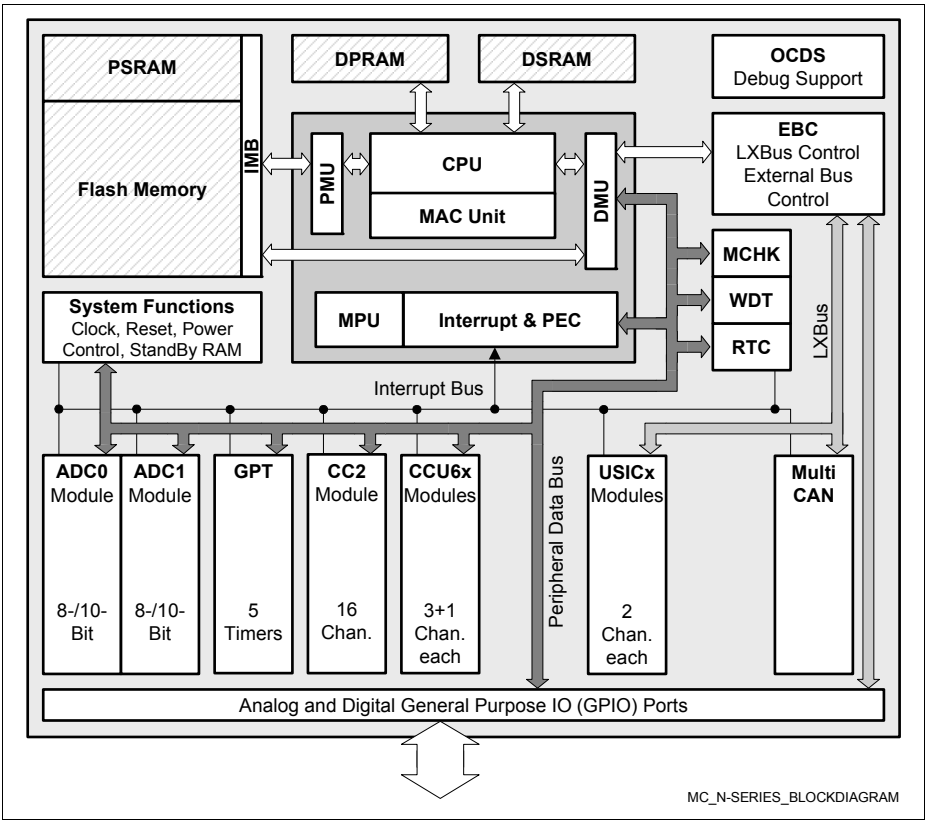

Figure 4 Block Diagram

Up to 16 Kbytes of on-chip Data SRAM (DSRAM) are used for storage of general user data. The DSRAM is accessed via a separate interface and is optimized for data access.

Note: The actual size of the DSRAM depends on the quoted device type.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, …, RL7, RH7) General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

8 Kbytes of on-chip Stand-By SRAM (SBRAM) provide storage for system-relevant user data that must be preserved while the major part of the device is powered down. The SBRAM is accessed via a specific interface and is powered in domain M.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XE166 Family. In order to ensure upward compatibility they should either not be accessed or written with zeros.

In order to meet the requirements of designs where more memory is required than is available on chip, up to 12 Mbytes (approximately, see **Table 7**) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

The on-chip Flash memory stores code, constant data, and control data. The 320 Kbytes of on-chip Flash memory consist of 1 module of 64 Kbytes (preferably for data storage) and 1 module of 256 Kbytes. Each module is organized in 4-Kbyte sectors. The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

Note: The actual size of the Flash memory depends on the chosen device type.

Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.
For Flash parameters, please see **Section 4.6**.

1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

Table 8 Compare Modes (cont'd)

Compare Modes	Function
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

3.9 Capture/Compare Units CCU6x

The XE164xN types feature the CCU60, CCU61 unit(s).

CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

Timer 13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

Additional Features

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC drives
- Output levels can be selected and adapted to the power stage

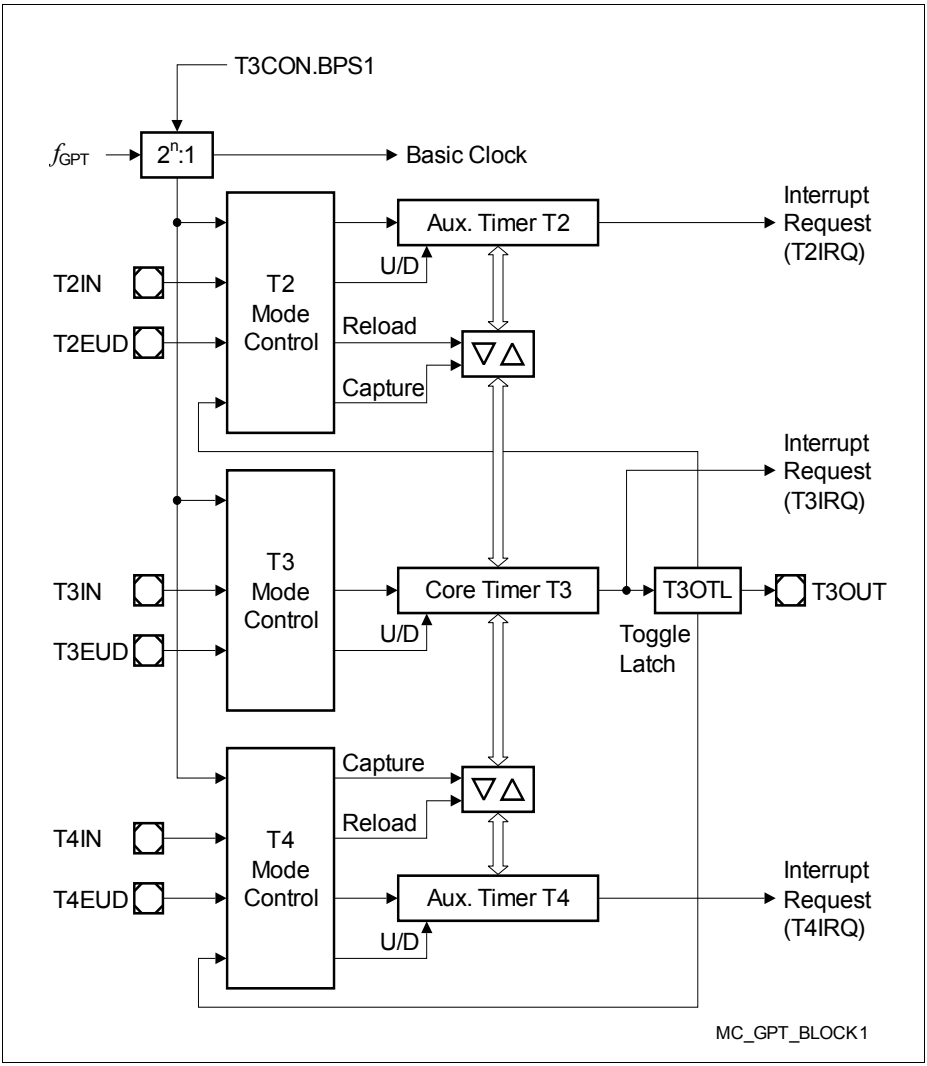

Figure 8 Block Diagram of GPT1

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time-based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long-term measurements
- Alarm interrupt at a defined time

Table 10 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2 / 4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Unused instruction[1)]	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4

Table 10 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

1) The Enter Power Down Mode instruction is not used in the XE164xN, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

4.3.1 DC Parameters for Upper Voltage Area

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Note: Operating Conditions apply.

Table 15 is valid under the following conditions: $V_{DDP} \leq$ 5.5 V; V_{DDP}typ. 5 V; $V_{DDP} \geq$ 4.5 V

Table 15 DC Characteristics for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs). To be doubled for double bond pins.[1)]	C_{IO} CC	–	–	10	pF	not subject to production test
Input Hysteresis[2)]	HYS CC	0.11 x V_{DDP}	–	–	V	R_S= 0 Ohm
Absolute input leakage current on pins of analog ports[3)]	$\|I_{OZ1}\|$ CC	–	10	200	nA	$V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Absolute input leakage current for all other pins. To be doubled for double bond pins.[3)1)4)]	$\|I_{OZ2}\|$ CC	–	0.2	5	µA	$T_J \leq$ 110 °C; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
		–	0.2	15	µA	$T_J \leq$ 150 °C; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Pull Level Force Current[5)]	$\|I_{PLF}\|$ SR	250	–	–	µA	$V_{IN} \geq V_{IHmin}$*(pull down_enabled)*; $V_{IN} \leq V_{ILmax}$*(pull up_enabled)*
Pull Level Keep Current[6)]	$\|I_{PLK}\|$ SR	–	–	30	µA	$V_{IN} \geq V_{IHmin}$*(pull up_enabled)*; $V_{IN} \leq V_{ILmax}$*(pull down_enabled)*
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	–	0.3 x V_{DDP}	V	

4.3.2 DC Parameters for Lower Voltage Area

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Note: Operating Conditions apply.

Table 16 is valid under the following conditions: $V_{DDP} \geq$ 3.0 V; V_{DDP}typ. 3.3 V; $V_{DDP} \leq$ 4.5 V

Table 16 DC Characteristics for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs). To be doubled for double bond pins.[1]	C_{IO} CC	–	–	10	pF	not subject to production test
Input Hysteresis[2]	HYS CC	0.07 x V_{DDP}	–	–	V	R_S= 0 Ohm
Absolute input leakage current on pins of analog ports[3]	$\|I_{OZ1}\|$ CC	–	10	200	nA	$V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Absolute input leakage current for all other pins. To be doubled for double bond pins.[3][1][4]	$\|I_{OZ2}\|$ CC	–	0.2	2.5	µA	$T_J \leq$ 110 °C; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
		–	0.2	8	µA	$T_J \leq$ 150 °C; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Pull Level Force Current[5]	$\|I_{PLF}\|$ SR	150	–	–	µA	$V_{IN} \geq V_{IHmin}$*(pull down)* ; $V_{IN} \leq V_{ILmax}$*(pull up)*
Pull Level Keep Current[6]	$\|I_{PLK}\|$ SR	–	–	10	µA	$V_{IN} \geq V_{IHmin}$*(pull up)* ; $V_{IN} \leq V_{ILmax}$*(pull down)*
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	–	0.3 x V_{DDP}	V	

Note: A fraction of the leakage current flows through domain DMP_A (pin V_{DDPA}). This current can be calculated as 7,000 $\times$ $e^{-\alpha}$, with α = 5000 / (273 + 1.3 $\times$ T_J). For T_J = 150°C, this results in a current of 160 μA.

Leakage Power Consumption Calculation

The leakage power consumption can be calculated according to the following formula:

$I_{LK1} = 530{,}000 \times e^{-\alpha}$ with $\alpha = 5000 / (273 + B \times T_J)$

Parameter B must be replaced by

- 1.0 for typical values
- 1.3 maximum values

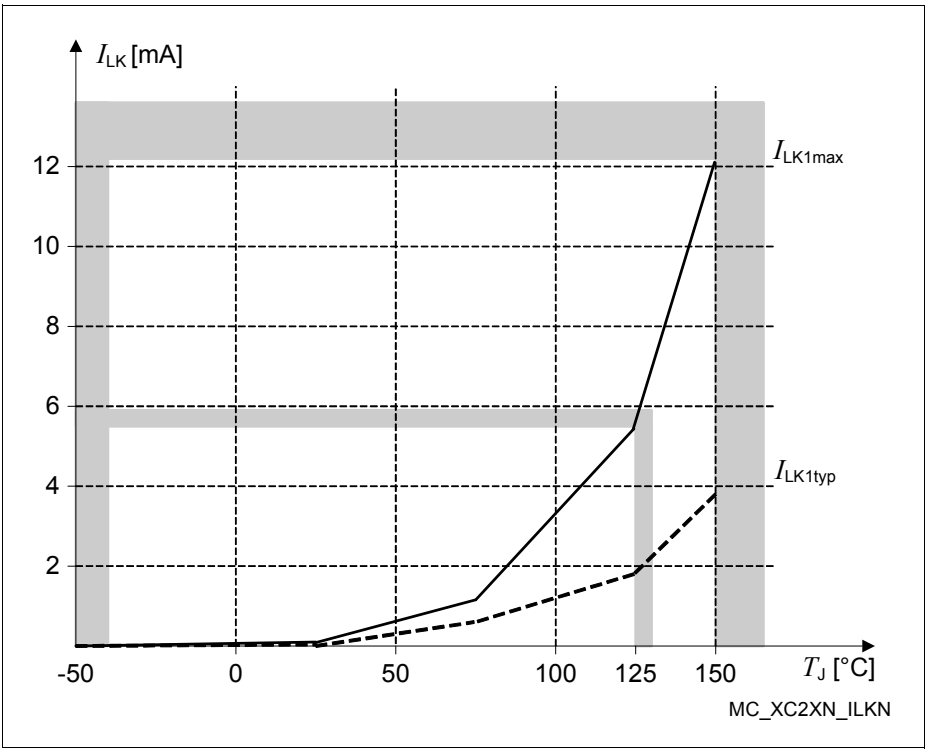

Figure 15 Leakage Supply Current as a Function of Temperature

Sample time and conversion time of the XE164xN's A/D converters are programmable. The timing above can be calculated using **Table 20**.
The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

Table 20 A/D Converter Computation Table

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}	INPCRx.7-0 (STC)	Sample Time[1] t_S
000000_B	f_{SYS}	00_H	$t_{ADCI} \times 2$
000001_B	f_{SYS} / 2	01_H	$t_{ADCI} \times 3$
000010_B	f_{SYS} / 3	02_H	$t_{ADCI} \times 4$
:	f_{SYS} / (DIVA+1)	:	$t_{ADCI} \times$ (STC+2)
111110_B	f_{SYS} / 63	FE_H	$t_{ADCI} \times 256$
111111_B	f_{SYS} / 64	FF_H	$t_{ADCI} \times 257$

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

Converter Timing Example A:

Assumptions: f_{SYS} = 80 MHz (i.e. t_{SYS} = 12.5 ns), DIVA = 03_H, STC = 00_H
Analog clock f_{ADCI} = f_{SYS} / 4 = 20 MHz, i.e. t_{ADCI} = 50 ns
Sample time t_S = $t_{ADCI} \times 2$ = 100 ns

Conversion 10-bit:

t_{C10} = $13 \times t_{ADCI} + 2 \times t_{SYS}$ = 13×50 ns + 2×12.5 ns = 0.675 µs

Conversion 8-bit:

t_{C8} = $11 \times t_{ADCI} + 2 \times t_{SYS}$ = 11×50 ns + 2×12.5 ns = 0.575 µs

Converter Timing Example B:

Assumptions: f_{SYS} = 40 MHz (i.e. t_{SYS} = 25 ns), DIVA = 02_H, STC = 03_H
Analog clock f_{ADCI} = f_{SYS} / 3 = 13.3 MHz, i.e. t_{ADCI} = 75 ns
Sample time t_S = $t_{ADCI} \times 5$ = 375 ns

Conversion 10-bit:

t_{C10} = $16 \times t_{ADCI} + 2 \times t_{SYS}$ = 16×75 ns + 2×25 ns = 1.25 µs

Conversion 8-bit:

t_{C8} = $14 \times t_{ADCI} + 2 \times t_{SYS}$ = 14×75 ns + 2×25 ns = 1.10 µs

4.5 System Parameters

The following parameters specify several aspects which are important when integrating the XE164xN into an application system.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 21 Various System Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Short-term deviation of internal clock source frequency[1]	Δf_{INT} CC	-1	–	1	%	$\Delta T_J \leq 10°C$
Internal clock source frequency	f_{INT} CC	4.8	5.0	5.2	MHz	
Wakeup clock source frequency[2]	f_{WU} CC	400	–	700	kHz	FREQSEL= 00
		210	–	390	kHz	FREQSEL= 01
		140	–	260	kHz	FREQSEL= 10
		110	–	200	kHz	FREQSEL= 11
Startup time from power-on with code execution from Flash	t_{SPO} CC	1.5	2.0	2.4	ms	f_{WU}= 500 kHz
Startup time from stopover mode with code execution from PSRAM	t_{SSO} CC	11 / f_{WU}[3]	–	12 / f_{WU}[3]	µs	
Core voltage (PVC) supervision level	V_{PVC} CC	V_{LV} - 0.03	V_{LV}	V_{LV} + 0.07[4]	V	[5]
Supply watchdog (SWD) supervision level	V_{SWD} CC	V_{LV} - 0.10[6]	V_{LV}	V_{LV} + 0.15	V	voltage_range= lower [5]
		V_{LV} - 0.15	V_{LV}	V_{LV} + 0.15	V	voltage_range= upper [5]
		V_{LV} - 0.30	V_{LV}	V_{LV} + 0.30	V	V_{LV} = 5.5 V [5]

1) The short-term frequency deviation refers to a timeframe of a few hours and is measured relative to the current frequency at the beginning of the respective timeframe. This parameter is useful to determine a time span for re-triggering a LIN synchronization.

1) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF}. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1}.
2) Overload conditions must not occur on pin XTAL1.

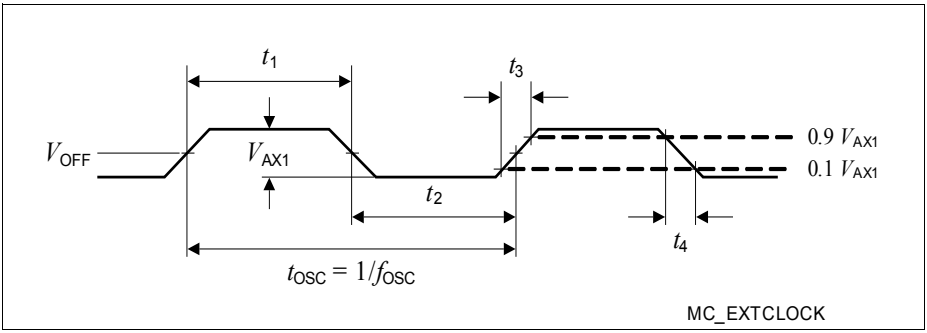

Figure 21 External Clock Drive XTAL1

Note: For crystal or ceramic resonator operation, it is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for oscillator operation.
The manufacturers of crystals and ceramic resonators offer an oscillator evaluation service. This evaluation checks the crystal/resonator specification limits to ensure a reliable oscillator operation.

Table 28 Standard Pad Parameters for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	37 + 0.65 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Medium
		–	–	24 + 0.3 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Medium
		–	–	6.2 + 0.24 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Sharp
		–	–	34 + 0.3 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Slow
		–	–	500 + 2.5 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Weak

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and Σ-I_{OH}) must remain below 50 mA.

Table 39 JTAG Interface Timing for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK low time	t_3 SR	16	–	–	ns	
TCK clock rise time	t_4 SR	–	–	8	ns	
TCK clock fall time	t_5 SR	–	–	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid from TCK falling edge (propagation delay)[2]	t_8 CC	–	25	29	ns	
TDO high impedance to valid output from TCK falling edge[3][2]	t_9 CC	–	25	29	ns	
TDO valid output to high impedance from TCK falling edge[2]	t_{10} CC	–	25	29	ns	
TDO hold after TCK falling edge[2]	t_{18} CC	5	–	–	ns	

1) Under typical conditions, the JTAG interface can operate at transfer rates up to 20 MHz.
2) The falling edge on TCK is used to generate the TDO timing.
3) The setup time for TDO is given implicitly by the TCK cycle time.

Table 40 is valid under the following conditions: C_L= 20 pF; voltage_range= lower

Table 40 JTAG Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50	–	–	ns	
TCK high time	t_2 SR	16	–	–	ns	
TCK low time	t_3 SR	16	–	–	ns	
TCK clock rise time	t_4 SR	–	–	8	ns	
TCK clock fall time	t_5 SR	–	–	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	

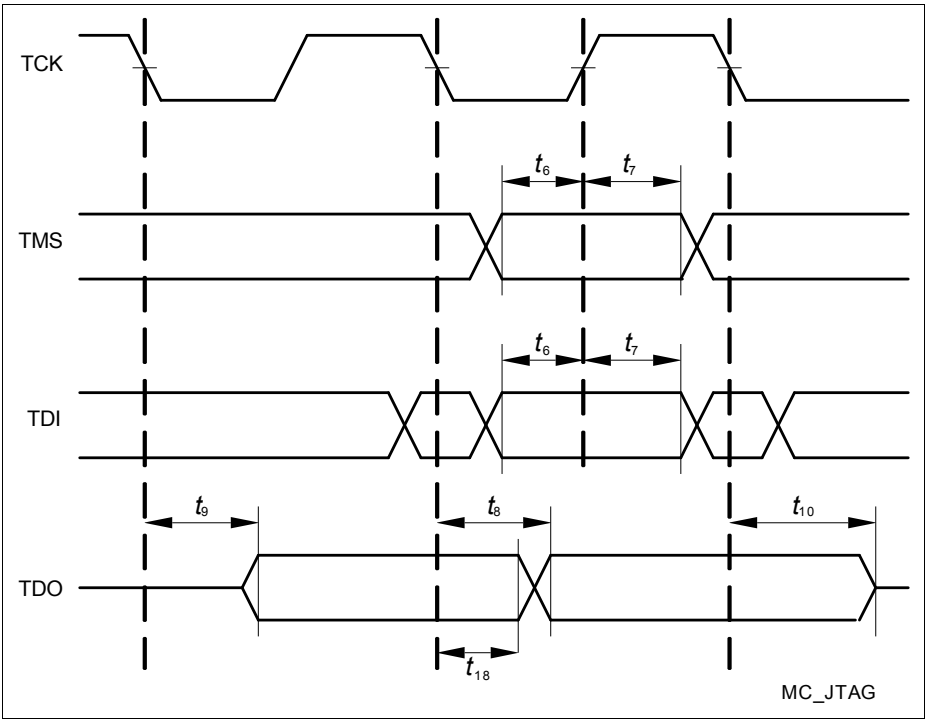

Figure 31 JTAG Timing