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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Obsolete
Core Processor	C1665V2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xe164gn-40f80l-aa
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Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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General Device Information

Tabl	able 5 Pin Definitions and Functions (cont'd)						
Pin	Symbol	Ctrl.	Туре	Function			
39	P2.0	O0 / I	St/B	Bit 0 of Port 2, General Purpose Input/Output			
	AD13	OH / IH	St/B	External Bus Interface Address/Data Line 13			
	RxDC0C	I	St/B	CAN Node 0 Receive Data Input			
	T5INB	I	St/B	GPT12E Timer T5 Count/Gate Input			
40	P2.1	O0 / I	St/B	Bit 1 of Port 2, General Purpose Input/Output			
	TxDC0	01	St/B	CAN Node 0 Transmit Data Output			
	AD14	OH / IH	St/B	External Bus Interface Address/Data Line 14			
	T5EUDB	I	St/B	GPT12E Timer T5 External Up/Down Control Input			
	ESR1_5	I	St/B	ESR1 Trigger Input 5			
41	P2.2	O0 / I	St/B	Bit 2 of Port 2, General Purpose Input/Output			
	TxDC1	01	St/B	CAN Node 1 Transmit Data Output			
	AD15	OH / IH	St/B	External Bus Interface Address/Data Line 15			
	ESR2_5	I	St/B	ESR2 Trigger Input 5			
42	P4.0	O0 / I	St/B	Bit 0 of Port 4, General Purpose Input/Output			
	CC2_CC24	O3 / I	St/B	CAPCOM2 CC24IO Capture Inp./ Compare Out.			
	CS0	OH	St/B	External Bus Interface Chip Select 0 Output			
43	P2.3	O0 / I	St/B	Bit 3 of Port 2, General Purpose Input/Output			
	U0C0_DOUT	01	St/B	USIC0 Channel 0 Shift Data Output			
	CC2_CC16	O3 / I	St/B	CAPCOM2 CC16IO Capture Inp./ Compare Out.			
	A16	ОН	St/B	External Bus Interface Address Line 16			
	ESR2_0	I	St/B	ESR2 Trigger Input 0			
	U0C0_DX0E	I	St/B	USIC0 Channel 0 Shift Data Input			
	U0C1_DX0D	I	St/B	USIC0 Channel 1 Shift Data Input			
	RxDC0A	I	St/B	CAN Node 0 Receive Data Input			



General Device Information

Tabl	able 5Pin Definitions and Functions (cont'd)					
Pin	Symbol	Ctrl.	Туре	Function		
44	P4.1	O0 / I	St/B	Bit 1 of Port 4, General Purpose Input/Output		
	CC2_CC25	O3 / I	St/B	CAPCOM2 CC25IO Capture Inp./ Compare Out.		
	CS1	OH	St/B	External Bus Interface Chip Select 1 Output		
	T4EUDB	I	St/B	GPT12E Timer T4 External Up/Down Control Input		
	ESR1_8	I	St/B	ESR1 Trigger Input 8		
45	P2.4	O0 / I	St/B	Bit 4 of Port 2, General Purpose Input/Output		
	U0C1_DOUT	01	St/B	USIC0 Channel 1 Shift Data Output		
	TxDC0	02	St/B	CAN Node 0 Transmit Data Output		
	CC2_CC17	O3 / I	St/B	CAPCOM2 CC17IO Capture Inp./ Compare Out.		
	A17	OH	St/B	External Bus Interface Address Line 17		
	ESR1_0	I	St/B	ESR1 Trigger Input 0		
	U0C0_DX0F	I	St/B	USIC0 Channel 0 Shift Data Input		
	RxDC1A	I	St/B	CAN Node 1 Receive Data Input		
46	P2.5	O0 / I	St/B	Bit 5 of Port 2, General Purpose Input/Output		
	U0C0_SCLK OUT	01	St/B	USIC0 Channel 0 Shift Clock Output		
	TxDC0	02	St/B	CAN Node 0 Transmit Data Output		
	CC2_CC18	O3 / I	St/B	CAPCOM2 CC18IO Capture Inp./ Compare Out.		
	A18	ОН	St/B	External Bus Interface Address Line 18		
	U0C0_DX1D	I	St/B	USIC0 Channel 0 Shift Clock Input		
	ESR1_10	I	St/B	ESR1 Trigger Input 10		
47	P4.2	O0 / I	St/B	Bit 2 of Port 4, General Purpose Input/Output		
	CC2_CC26	O3 / I	St/B	CAPCOM2 CC26IO Capture Inp./ Compare Out.		
	CS2	OH	St/B	External Bus Interface Chip Select 2 Output		
	T2INA	I	St/B	GPT12E Timer T2 Count/Gate Input		



General Device Information

Table	Pin Definitions and Functions (cont'd)					
Pin	Symbol	Ctrl.	Туре	Function		
59	P10.0	O0 / I	St/B	Bit 0 of Port 10, General Purpose Input/Output		
	U0C1_DOUT	01	St/B	USIC0 Channel 1 Shift Data Output		
	CCU60_CC6 0	02	St/B	CCU60 Channel 0 Output		
	AD0	OH / IH	St/B	External Bus Interface Address/Data Line 0		
	CCU60_CC6 0INA	I	St/B	CCU60 Channel 0 Input		
	ESR1_2	I	St/B	ESR1 Trigger Input 2		
	U0C0_DX0A	I	St/B	USIC0 Channel 0 Shift Data Input		
	U0C1_DX0A	I	St/B	USIC0 Channel 1 Shift Data Input		
60	P10.1	O0 / I	St/B	Bit 1 of Port 10, General Purpose Input/Output		
	U0C0_DOUT	01	St/B	USIC0 Channel 0 Shift Data Output		
	CCU60_CC6 1	02	St/B	CCU60 Channel 1 Output		
	AD1	OH / IH	St/B	External Bus Interface Address/Data Line 1		
	CCU60_CC6 1INA	I	St/B	CCU60 Channel 1 Input		
	U0C0_DX1A	Ι	St/B	USIC0 Channel 0 Shift Clock Input		
	U0C0_DX0B	I	St/B	USIC0 Channel 0 Shift Data Input		
61	P0.3	O0 / I	St/B	Bit 3 of Port 0, General Purpose Input/Output		
	U1C0_SELO 0	01	St/B	USIC1 Channel 0 Select/Control 0 Output		
	U1C1_SELO 1	O2	St/B	USIC1 Channel 1 Select/Control 1 Output		
	CCU61_COU T60	O3	St/B	CCU61 Channel 0 Output		
	A3	ОН	St/B	External Bus Interface Address Line 3		
	U1C0_DX2A	I	St/B	USIC1 Channel 0 Shift Control Input		
	RxDC0B	I	St/B	CAN Node 0 Receive Data Input		



General Device Information

Table	Table 5Pin Definitions and Functions (cont'd)						
Pin	Symbol	Ctrl.	Туре	Function			
67	P10.3	O0 / I	St/B	Bit 3 of Port 10, General Purpose Input/Output			
	CCU60_COU T60	02	St/B	CCU60 Channel 0 Output			
	AD3	OH / IH	St/B	External Bus Interface Address/Data Line 3			
	U0C0_DX2A	I	St/B	USIC0 Channel 0 Shift Control Input			
	U0C1_DX2A	I	St/B	USIC0 Channel 1 Shift Control Input			
68	P0.5	O0 / I	St/B	Bit 5 of Port 0, General Purpose Input/Output			
	U1C1_SCLK OUT	01	St/B	USIC1 Channel 1 Shift Clock Output			
	U1C0_SELO 2	02	St/B	USIC1 Channel 0 Select/Control 2 Output			
	CCU61_COU T62	O3	St/B	CCU61 Channel 2 Output			
	A5	OH	St/B	External Bus Interface Address Line 5			
	U1C1_DX1A	I	St/B	USIC1 Channel 1 Shift Clock Input			
	U1C0_DX1C	I	St/B	USIC1 Channel 0 Shift Clock Input			
69	P10.4	O0 / I	St/B	Bit 4 of Port 10, General Purpose Input/Output			
	U0C0_SELO 3	01	St/B	USIC0 Channel 0 Select/Control 3 Output			
	CCU60_COU T61	02	St/B	CCU60 Channel 1 Output			
	AD4	OH / IH	St/B	External Bus Interface Address/Data Line 4			
	U0C0_DX2B	I	St/B	USIC0 Channel 0 Shift Control Input			
	U0C1_DX2B	I	St/B	USIC0 Channel 1 Shift Control Input			
	ESR1_9	I	St/B	ESR1 Trigger Input 9			



Functional Description

3 Functional Description

The architecture of the XE164xN combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources. This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XE164xN.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XE164xN.



Figure 4 Block Diagram



Functional Description



Figure 6 CAPCOM Unit Block Diagram



Functional Description

3.9 Capture/Compare Units CCU6x

The XE164xN types feature the CCU60, CCU61 unit(s).

CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for highside and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- · Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

Timer 13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- · Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

Additional Features

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal (CTRAP)
- · Control modes for multi-channel AC drives
- · Output levels can be selected and adapted to the power stage



Functional Description



Figure 7 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.



Functional Description

3.10 General Purpose Timer (GPT12E) Unit

The GPT12E unit is a very flexible multifunctional timer/counter structure which can be used for many different timing tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers organized in two separate modules, GPT1 and GPT2. Each timer in each module may either operate independently in a number of different modes or be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation: Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock and divided by a programmable prescaler. Counter Mode allows timer clocking in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes each timer has one associated port pin (TxIN) which serves as a gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The counting direction (up/down) for each timer can be programmed by software or altered dynamically by an external signal on a port pin (TxEUD), e.g. to facilitate position tracking.

In Incremental Interface Mode the GPT1 timers can be directly connected to the incremental position sensor signals A and B through their respective inputs TxIN and TxEUD. Direction and counting signals are internally derived from these two input signals, so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to the basic operating modes, T2 and T4 may be configured as reload or capture register for timer T3. A timer used as capture or reload register is stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at the associated input pin (TxIN). Timer T3 is reloaded with the contents of T2 or T4, triggered either by an external signal or a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be continuously generated without software intervention.



Functional Description







Functional Description

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD¹). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XE164xN to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

¹⁾ Exception: T5EUD is not connected to a pin.



Functional Description

Table 10 Instr	uction Set Summary (cont'd)			
Mnemonic	Description	Bytes		
ROL/ROR	Rotate left/right direct word GPR	2		
ASHR	Arithmetic (sign bit) shift right direct word GPR	2		
MOV(B)	Nove word (byte) data			
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2/4		
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4		
JMPS	Jump absolute to a code segment	4		
JB(C)	Jump relative if direct bit is set (and clear bit)	4		
JNB(S)	Jump relative if direct bit is not set (and set bit)	4		
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4		
CALLS	Call absolute subroutine in any code segment	4		
PCALL Push direct word register onto system stack and call absolute subroutine				
RAP Call interrupt service routine via immediate trap number		2		
PUSH/POP	Push/pop direct word register onto/from system stack	2		
SCXT	Push direct word register onto system stack and update register with word operand			
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)			
RETS	Return from inter-segment subroutine	2		
RETI	Return from interrupt service subroutine	2		
SBRK	Software Break	2		
SRST	Software Reset	4		
IDLE	Enter Idle Mode	4		
PWRDN	Unused instruction ¹⁾	4		
SRVWDT	Service Watchdog Timer	4		
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4		
EINIT	End-of-Initialization Register Lock	4		
ATOMIC	Begin ATOMIC sequence	2		
EXTR	Begin EXTended Register sequence	2		
EXTP(R)	Begin EXTended Page (and Register) sequence	2/4		
EXTS(R)	Begin EXTended Segment (and Register) sequence	2/4		



Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.	-	Test Condition
Output High voltage ⁷⁾	V _{OH} CC	V _{DDP} - 1.0	-	-	V	$I_{\rm OH} \ge I_{\rm OHmax}$
		V _{DDP} - 0.4	-	-	V	$I_{\text{OH}} \ge I_{\text{OHnom}}^{8}$
Output Low Voltage ⁷⁾	V _{OL} CC	-	-	0.4	V	$I_{\rm OL} \le I_{\rm OLnom}$ ⁸⁾
		-	-	1.0	V	$I_{\rm OL} \leq I_{\rm OLmax}$

Table 15 DC Characteristics for Upper Voltage Range (cont'd)

1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.

 Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

- 3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{\rm IN} < V_{\rm SS}$) or supply ripple ($V_{\rm IN} > V_{\rm DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current ($I_{\rm INJ}$) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor $K_{\rm CV}$.
- 4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature (*T*_J = junction temperature [°C]): *I*_{OZ} = 0.05 x e^(1.5 + 0.028 x T,J>) [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = *V*_{DDP} *V*_{PIN} [V]): *I*_{OZ} = *I*_{OZtempmax} (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.
- Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device.
- 6) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level.
- 7) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
- 8) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL} -> V_{SS} , V_{OH} -> V_{DDP}). However, only the levels for nominal output currents are verified.



Sample time and conversion time of the XE164xN's A/D converters are programmable. The timing above can be calculated using Table 20.

The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

GLOBCTR.5-0	A/D Converter	INPCRx.7-0	Sample Time ¹⁾
000000 _B	f _{sys}	00 _H	$t_{ADCI} \times 2$
000001 _B	f _{SYS} / 2	01 _H	$t_{ADCI} \times 3$
000010 _B	<i>f</i> _{SYS} / 3	02 _H	$t_{ADCI} \times 4$
:	$f_{\rm SYS}$ / (DIVA+1)	:	$t_{ADCI} \times (STC+2)$
111110 _B	f _{SYS} / 63	FE _H	$t_{ADCI} imes 256$
111111 _B	f _{SYS} / 64	FF _H	$t_{ADCI} imes 257$

 Table 20
 A/D Converter Computation Table

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

Converter Timing Example A:

Assumptions:	$f_{\rm SYS}$	= 80 MHz (i.e. t_{SYS} = 12.5 ns), DIVA = 03 _H , STC = 00 _H
Analog clock	$f_{\sf ADCI}$	$= f_{SYS} / 4 = 20 \text{ MHz}$, i.e. $t_{ADCI} = 50 \text{ ns}$
Sample time	t _S	$= t_{ADCI} \times 2 = 100 \text{ ns}$
Conversion 10	-bit:	
	<i>t</i> _{C10}	= $13 \times t_{ADCI}$ + $2 \times t_{SYS}$ = 13×50 ns + 2×12.5 ns = 0.675 μ s
Conversion 8-I	oit:	
	t _{C8}	= $11 \times t_{ADCI}$ + 2 × t_{SYS} = 11 × 50 ns + 2 × 12.5 ns = 0.575 µs

Converter Timing Example B:

Assumptions:	$f_{\rm SYS}$	= 40 MHz (i.e. t_{SYS} = 25 ns), DIVA = 02 _H , STC = 03 _H
Analog clock	$f_{\sf ADCI}$	$= f_{SYS} / 3 = 13.3 \text{ MHz}$, i.e. $t_{ADCI} = 75 \text{ ns}$
Sample time	t _S	$= t_{ADCI} \times 5 = 375 \text{ ns}$
Conversion 10-	bit:	
	<i>t</i> _{C10}	= $16 \times t_{ADCI}$ + 2 × t_{SYS} = 16 × 75 ns + 2 × 25 ns = 1.25 µs
Conversion 8-b	oit:	
	t _{C8}	= $14 \times t_{ADCI}$ + $2 \times t_{SYS}$ = 14×75 ns + 2×25 ns = 1.10 μ s



Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Maximum output driver current (absolute value) ¹⁾	I _{Omax} CC	-	-	2.5	mA	Driver_Strength = Medium
		_	-	10	mA	Driver_Strength = Strong
		_	-	0.5	mA	Driver_Strength = Weak
Nominal output driver current (absolute value)	I _{Onom} CC	_	-	1.0	mA	Driver_Strength = Medium
		_	-	2.5	mA	Driver_Strength = Strong
		_	-	0.1	mA	Driver_Strength = Weak

Table 28 Standard Pad Parameters for Lower Voltage Range



4.7.5 External Bus Timing

The following parameters specify the behavior of the XE164xN bus interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 29 Parameters

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
CLKOUT Cycle Time ¹⁾	t ₅ CC	-	$1/f_{\rm SYS}$	-	ns	
CLKOUT high time	t ₆ CC	3	-	-		
CLKOUT low time	t ₇ CC	3	_	-		
CLKOUT rise time	t ₈ CC	-	-	3	ns	
CLKOUT fall time	t ₉ CC	-	-	3		

1) The CLKOUT cycle time is influenced by PLL jitter. For longer periods the relative deviation decreases (see PLL deviation formula).



Figure 22 CLKOUT Signal Timing

Note: The term CLKOUT refers to the reference clock output signal which is generated by selecting f_{SYS} as the source signal for the clock output signal EXTCLK on pin P2.8 and by enabling the high-speed clock driver on this pin.



Variable Memory Cycles

External bus cycles of the XE164xN are executed in five consecutive cycle phases (AB, C, D, E, F). The duration of each cycle phase is programmable (via the TCONCSx registers) to adapt the external bus cycles to the respective external module (memory, peripheral, etc.).

The duration of the access phase can optionally be controlled by the external module using the READY handshake input.

This table provides a summary of the phases and the ranges for their length.

Table 30	Programmable Bus	Cycle Phases	(see timing diagram	s)

Bus Cycle Phase	Parameter	Valid Values	Unit
Address setup phase, the standard duration of this phase (1 2 TCS) can be extended by 0 3 TCS if the address window is changed	tpAB	1 2 (5)	TCS
Command delay phase	tpC	03	TCS
Write Data setup/MUX Tristate phase	tpD	0 1	TCS
Access phase	tpE	1 32	TCS
Address/Write Data hold phase	tpF	03	TCS

Note: The bandwidth of a parameter (from minimum to maximum value) covers the whole operating range (temperature, voltage) as well as process variations. Within a given device, however, this bandwidth is smaller than the specified range. This is also due to interdependencies between certain parameters. Some of these interdependencies are described in additional notes (see standard timing).

Note: Operating Conditions apply.

Table 31 is valid under the following conditions: C_L = 20 pF; voltage_range= upper; voltage_range= upper

Table 31	External Bus	Timing for	Upper ¹	Voltage Range
	External Das	r mining i vi	Opper	Voltage Range

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Output valid delay for \overline{RD} , $\overline{WR}(L/\overline{H})$	<i>t</i> ₁₀ CC	-	7	13	ns	
Output valid delay for BHE, ALE	<i>t</i> ₁₁ CC	-	7	14	ns	
Address output valid delay for A23 A0	<i>t</i> ₁₂ CC	-	8	14	ns	



Note: If the READY input is sampled inactive at the indicated sampling point ("Not Rdy") a READY-controlled waitstate is inserted (tpRDY),

sampling the READY input active at the indicated sampling point ("Ready") terminates the currently running bus cycle.

Note the different sampling points for synchronous and asynchronous READY. This example uses one mandatory waitstate (see tpE) before the READY input value is used.



4.7.7 Debug Interface Timing

The debugger can communicate with the XE164xN either via the 2-pin DAP interface or via the standard JTAG interface.

Debug via DAP

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 37 is valid under the following conditions: $C_1 = 20 \text{ pF}$; voltage_range= upper

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
DAP0 clock period ¹⁾	<i>t</i> ₁₁ SR	25	-	-	ns	
DAP0 high time	<i>t</i> ₁₂ SR	8	-	_	ns	
DAP0 low time ¹⁾	t ₁₃ SR	8	-	-	ns	
DAP0 clock rise time	<i>t</i> ₁₄ SR	-	-	4	ns	
DAP0 clock fall time	t ₁₅ SR	-	-	4	ns	
DAP1 setup to DAP0 rising edge	<i>t</i> ₁₆ SR	6	-	-	ns	
DAP1 hold after DAP0 rising edge	<i>t</i> ₁₇ SR	6	-	-	ns	
DAP1 valid per DAP0 clock period ²⁾	<i>t</i> ₁₉ CC	17	20	-	ns	

 Table 37
 DAP Interface Timing for Upper Voltage Range

1) See the DAP chapter for clock rate restrictions in the Active::IDLE protocol state.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

Table 38 is valid under the following conditions: C_{L} = 20 pF; voltage_range = lower