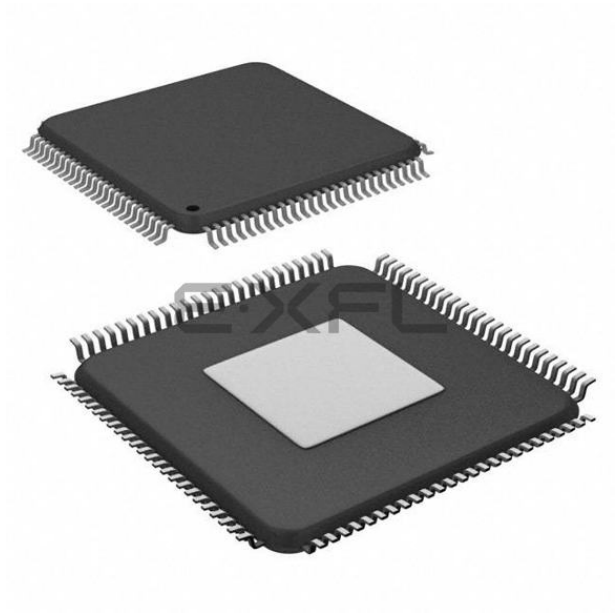
Infineon Technologies - SAK-XE164HN-16F80L AA Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	18K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xe164hn-16f80l-aa

XE164xN Data Sheet
Revision History: V1.4 2013-02

Previous Versions:
V1.3, 2011-07
V1.2, 2010-04
V1.1, 2009-07
V1.0, 2009-03 Preliminary

Page	Subjects (major changes since last revision)
36	Added AB step marking.
87	Errata SWD_X.P002 implemented: V_{SWD} tolerance boundaries for 5.5 V are changed.
89	Clarified “Coding of bit fields LEVxV” descriptions. Matched with Operating Conditions: marked some coding values “out of valid operation range”.
90	Errata FLASH_X.P001 implemented: Test Condition for Flash parameter N_{ER} corrected

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Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
31	P5.9	I	In/A	**Bit 9 of Port 5, General Purpose Input**
	ADC0_CH9	I	In/A	**Analog Input Channel 9 for ADC0**
	ADC1_CH9	I	In/A	**Analog Input Channel 9 for ADC1**
	CC2_T7IN	I	In/A	**CAPCOM2 Timer T7 Count Input**
32	P5.10	I	In/A	**Bit 10 of Port 5, General Purpose Input**
	ADC0_CH10	I	In/A	**Analog Input Channel 10 for ADC0**
	ADC1_CH10	I	In/A	**Analog Input Channel 10 for ADC1**
	$\overline{\text{BRKIN\_A}}$	I	In/A	**OCDS Break Signal Input**
	U2C1_DX0F	I	In/A	**USIC2 Channel 1 Shift Data Input**
	CCU61_T13HRA	I	In/A	**External Run Control Input for T13 of CCU61**
33	P5.11	I	In/A	**Bit 11 of Port 5, General Purpose Input**
	ADC0_CH11	I	In/A	**Analog Input Channel 11 for ADC0**
	ADC1_CH11	I	In/A	**Analog Input Channel 11 for ADC1**
34	P5.13	I	In/A	**Bit 13 of Port 5, General Purpose Input**
	ADC0_CH13	I	In/A	**Analog Input Channel 13 for ADC0**
35	P5.15	I	In/A	**Bit 15 of Port 5, General Purpose Input**
	ADC0_CH15	I	In/A	**Analog Input Channel 15 for ADC0**
36	P2.12	O0 / I	St/B	**Bit 12 of Port 2, General Purpose Input/Output**
	U0C0_SELO4	O1	St/B	**USIC0 Channel 0 Select/Control 4 Output**
	U0C1_SELO3	O2	St/B	**USIC0 Channel 1 Select/Control 3 Output**
	READY	IH	St/B	**External Bus Interface READY Input**
37	P2.11	O0 / I	St/B	**Bit 11 of Port 2, General Purpose Input/Output**
	U0C0_SELO2	O1	St/B	**USIC0 Channel 0 Select/Control 2 Output**
	U0C1_SELO2	O2	St/B	**USIC0 Channel 1 Select/Control 2 Output**
	$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	OH	St/B	**External Bus Interf. High-Byte Control Output** Can operate either as Byte High Enable ($\overline{\text{BHE}}$) or as Write strobe for High Byte ($\overline{\text{WRH}}$).

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
48	P2.6	O0 / I	St/B	**Bit 6 of Port 2, General Purpose Input/Output**
	U0C0_SELO 0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	U0C1_SELO 1	O2	St/B	**USIC0 Channel 1 Select/Control 1 Output**
	CC2_CC19	O3 / I	St/B	**CAPCOM2 CC19IO Capture Inp./ Compare Out.**
	A19	OH	St/B	**External Bus Interface Address Line 19**
	U0C0_DX2D	I	St/B	**USIC0 Channel 0 Shift Control Input**
	RxDC0D	I	St/B	**CAN Node 0 Receive Data Input**
	ESR2_6	I	St/B	**ESR2 Trigger Input 6**
49	P4.3	O0 / I	St/B	**Bit 3 of Port 4, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CC2_CC27	O3 / I	St/B	**CAPCOM2 CC27IO Capture Inp./ Compare Out.**
	$\overline{CS3}$	OH	St/B	**External Bus Interface Chip Select 3 Output**
	T2EUDA	I	St/B	**GPT12E Timer T2 External Up/Down Control Input**
53	P0.0	O0 / I	St/B	**Bit 0 of Port 0, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	CCU61_CC6 0	O3	St/B	**CCU61 Channel 0 IOutput**
	A0	OH	St/B	**External Bus Interface Address Line 0**
	U1C0_DX0A	I	St/B	**USIC1 Channel 0 Shift Data Input**
	CCU61_CC6 0INA	I	St/B	**CCU61 Channel 0 Input**
	ESR1_11	I	St/B	**ESR1 Trigger Input 11**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
67	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COUT60	O2	St/B	**CCU60 Channel 0 Output**
	AD3	OH / IH	St/B	**External Bus Interface Address/Data Line 3**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
68	P0.5	O0 / I	St/B	**Bit 5 of Port 0, General Purpose Input/Output**
	U1C1_SCLKOUT	O1	St/B	**USIC1 Channel 1 Shift Clock Output**
	U1C0_SELO2	O2	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	CCU61_COUT62	O3	St/B	**CCU61 Channel 2 Output**
	A5	OH	St/B	**External Bus Interface Address Line 5**
	U1C1_DX1A	I	St/B	**USIC1 Channel 1 Shift Clock Input**
	U1C0_DX1C	I	St/B	**USIC1 Channel 0 Shift Clock Input**
69	P10.4	O0 / I	St/B	**Bit 4 of Port 10, General Purpose Input/Output**
	U0C0_SELO3	O1	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CCU60_COUT61	O2	St/B	**CCU60 Channel 1 Output**
	AD4	OH / IH	St/B	**External Bus Interface Address/Data Line 4**
	U0C0_DX2B	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2B	I	St/B	**USIC0 Channel 1 Shift Control Input**
	ESR1_9	I	St/B	**ESR1 Trigger Input 9**

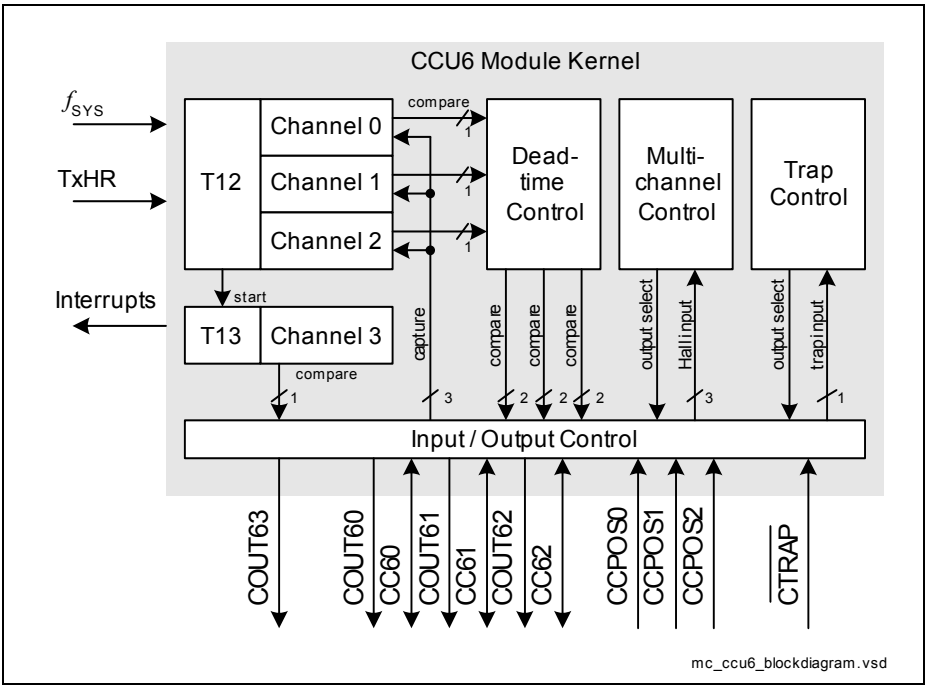

Figure 7 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

3.10 General Purpose Timer (GPT12E) Unit

The GPT12E unit is a very flexible multifunctional timer/counter structure which can be used for many different timing tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers organized in two separate modules, GPT1 and GPT2. Each timer in each module may either operate independently in a number of different modes or be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation: Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock and divided by a programmable prescaler. Counter Mode allows timer clocking in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes each timer has one associated port pin (TxIN) which serves as a gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The counting direction (up/down) for each timer can be programmed by software or altered dynamically by an external signal on a port pin (TxEUD), e.g. to facilitate position tracking.

In Incremental Interface Mode the GPT1 timers can be directly connected to the incremental position sensor signals A and B through their respective inputs TxIN and TxEUD. Direction and counting signals are internally derived from these two input signals, so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to the basic operating modes, T2 and T4 may be configured as reload or capture register for timer T3. A timer used as capture or reload register is stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at the associated input pin (TxIN). Timer T3 is reloaded with the contents of T2 or T4, triggered either by an external signal or a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be continuously generated without software intervention.

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time-based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long-term measurements
- Alarm interrupt at a defined time

3.13 Universal Serial Interface Channel Modules (USIC)

The XE164xN features the USIC modules USIC0, USIC1, USIC2. Each module provides two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.

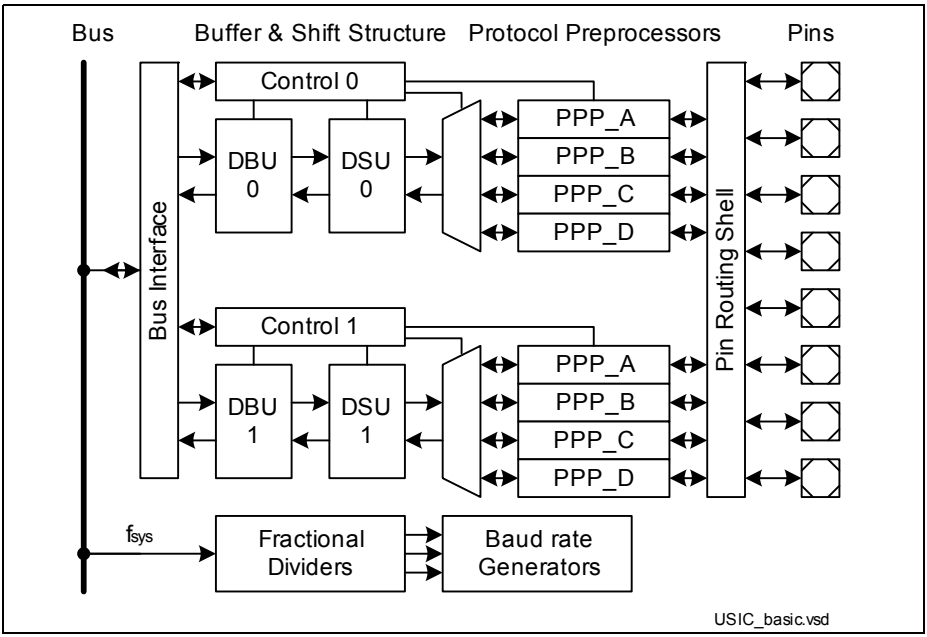

Figure 11 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

3.14 MultiCAN Module

The MultiCAN module contains independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames using a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

Note: The number of CAN nodes and message objects depends on the selected device type.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

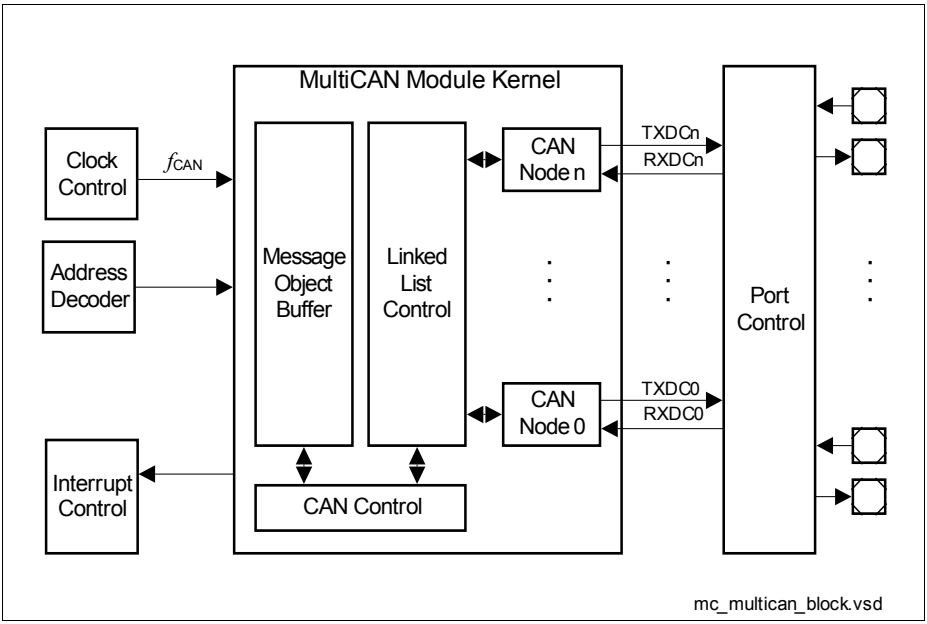

Figure 12 Block Diagram of MultiCAN Module

Table 12 Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload current coupling factor for digital I/O pins	K_{OVD} CC	–	1.0 x 10^{-2}	3.0 x 10^{-2}	-	I_{OV}< 0 mA; not subject to production test
		–	1.0 x 10^{-4}	5.0 x 10^{-3}	-	I_{OV}> 0 mA; not subject to production test
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$ SR	–	–	50	mA	not subject to production test
Digital core supply voltage for domain M[8)]	V_{DDIM} CC	–	1.5	–		
Digital core supply voltage for domain 1[8)]	V_{DDI1} CC	–	1.5	–		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	3.0	–	5.5	V	
Digital ground voltage	V_{SS} SR	–	0	–	V	

1) To ensure the stability of the voltage regulators the EVRs must be buffered with ceramic capacitors. Separate buffer capacitors with the recomended values shall be connected as close as possible to each V_{DDIM} and V_{DDI1} pin to keep the resistance of the board tracks below 2 Ohm. Connect all V_{DDI1} pins together. The minimum capacitance value is required for proper operation under all conditions (e.g. temperature). Higher values slightly increase the startup time.

2) Use one Capacitor for each pin.

3) This is the reference load. For bigger capacitive loads, use the derating factors listed in the pad properties section.

4) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).

5) The operating frequency range may be reduced for specific device types. This is indicated in the device designation (...FxxL). 80 MHz devices are marked ...F80L.

6) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{IHmax}$ ($I_{OV} > 0$) or $V_{OV} < V_{ILmin}$ (($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed 50 mA. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application. Overload conditions must not occur on pin XTAL1 (powered by V_{DDIM}).

4.3.1 DC Parameters for Upper Voltage Area

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Note: Operating Conditions apply.

Table 15 is valid under the following conditions: $V_{DDP} \leq$ 5.5 V; V_{DDP}typ. 5 V; $V_{DDP} \geq$ 4.5 V

Table 15 DC Characteristics for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs). To be doubled for double bond pins.[1)]	C_{IO} CC	–	–	10	pF	not subject to production test
Input Hysteresis[2)]	HYS CC	0.11 x V_{DDP}	–	–	V	R_S= 0 Ohm
Absolute input leakage current on pins of analog ports[3)]	$\|I_{OZ1}\|$ CC	–	10	200	nA	$V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Absolute input leakage current for all other pins. To be doubled for double bond pins.[3)1)4)]	$\|I_{OZ2}\|$ CC	–	0.2	5	µA	$T_J \leq$ 110 °C; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
		–	0.2	15	µA	$T_J \leq$ 150 °C; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Pull Level Force Current[5)]	$\|I_{PLF}\|$ SR	250	–	–	µA	$V_{IN} \geq V_{IHmin}$*(pull down_enabled)*; $V_{IN} \leq V_{ILmax}$*(pull up_enabled)*
Pull Level Keep Current[6)]	$\|I_{PLK}\|$ SR	–	–	30	µA	$V_{IN} \geq V_{IHmin}$*(pull up_enabled)*; $V_{IN} \leq V_{ILmax}$*(pull down_enabled)*
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	–	0.3 x V_{DDP}	V	

4.3.3 Power Consumption

The power consumed by the XE164xN depends on several factors such as supply voltage, operating frequency, active circuits, and operating temperature. The power consumption specified here consists of two components:

- The switching current I_S depends on the device activity
- The leakage current I_{LK} depends on the device temperature

To determine the actual power consumption, always both components, switching current I_S and leakage current I_{LK} must be added:

$I_{DDP} = I_S + I_{LK}$.

Note: The power consumption values are not subject to production test. They are verified by design/characterization.
To determine the total power consumption for dimensioning the external power supply, also the pad driver currents must be considered.

The given power consumption parameters and their values refer to specific operating conditions:

- **Active mode**:
  Regular operation, i.e. peripherals are active, code execution out of Flash.
- **Stopover mode**:
  Crystal oscillator and PLL stopped, Flash switched off, clock in domain DMP_1 stopped.

Note: The maximum values cover the complete specified operating range of all manufactured devices.
The typical values refer to average devices under typical conditions, such as nominal supply voltage, room temperature, application-oriented activity.
After a power reset, the decoupling capacitors for V_{DDIM} and V_{DDI1} are charged with the maximum possible current.

For additional information, please refer to **Section 5.2, Thermal Considerations**.

Note: Operating Conditions apply.

Table 19 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Broken wire detection delay against VAGND[2]	t_{BWG} CC	–	–	50[3]		
Broken wire detection delay against VAREF[2]	t_{BWR} CC	–	–	50[4]		
Conversion time for 8-bit result[2]	t_{c8} CC	(11+STC) x t_{ADCI} + 2 x t_{SYS}	–	–		
Conversion time for 10-bit result[2]	t_{c10} CC	(13+STC) x t_{ADCI} + 2 x t_{SYS}	–	–		
Total Unadjusted Error	|TUE| CC	–	1	2	LSB	[5]
Wakeup time from analog powerdown, fast mode	t_{WAF} CC	–	–	4	µs	
Wakeup time from analog powerdown, slow mode	t_{WAS} CC	–	–	15	µs	
Analog reference ground	V_{AGND} SR	V_{SS} - 0.05	–	1.5	V	
Analog input voltage range	V_{AIN} SR	V_{AGND}	–	V_{AREF}	V	[6]
Analog reference voltage	V_{AREF} SR	V_{AGND} + 1.0	–	V_{DDPA} + 0.05	V	

1) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used: $C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 5 pF, R_{AINtyp} = 1.0 kOhm, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 10 pF, $R_{AREFtyp}$ = 1.0 kOhm.

2) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result. Values for the basic clock t_{ADCI} depend on programming.

3) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 µs. Result below 10% (66_H)

Table 27 Standard Pad Parameters for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	23 + 0.6 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Medium
		–	–	11.6 + 0.22 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Medium
		–	–	4.2 + 0.14 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Sharp
		–	–	20.6 + 0.22 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Slow
		–	–	212 + 1.9 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Weak

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and Σ-I_{OH}) must remain below 50 mA.

Table 28 Standard Pad Parameters for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	37 + 0.65 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Medium
		–	–	24 + 0.3 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Medium
		–	–	6.2 + 0.24 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Sharp
		–	–	34 + 0.3 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Slow
		–	–	500 + 2.5 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Weak

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and Σ-I_{OH}) must remain below 50 mA.

4.7.5 External Bus Timing

The following parameters specify the behavior of the XE164xN bus interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 29 Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CLKOUT Cycle Time[1)]	t_5 CC	–	1 / f_{SYS}	–	ns	
CLKOUT high time	t_6 CC	3	–	–		
CLKOUT low time	t_7 CC	3	–	–		
CLKOUT rise time	t_8 CC	–	–	3	ns	
CLKOUT fall time	t_9 CC	–	–	3		

1) The CLKOUT cycle time is influenced by PLL jitter. For longer periods the relative deviation decreases (see PLL deviation formula).

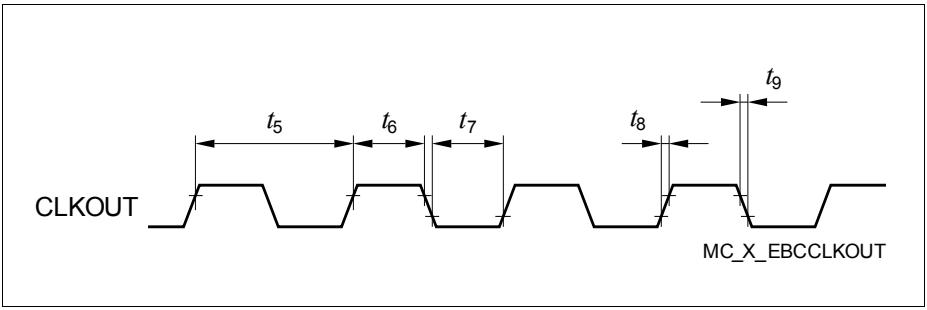

Figure 22 CLKOUT Signal Timing

Note: The term CLKOUT refers to the reference clock output signal which is generated by selecting f_{SYS} as the source signal for the clock output signal EXTCLK on pin P2.8 and by enabling the high-speed clock driver on this pin.

duration of an asynchronous READY signal for safe synchronization is one CLKOUT period plus the input setup time.

An active READY signal can be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{RD}$ or $\overline{WR}$).

If the next bus cycle is controlled by READY, an active READY signal must be disabled before the first valid sample point in the next bus cycle. This sample point depends on the programmed phases of the next cycle.

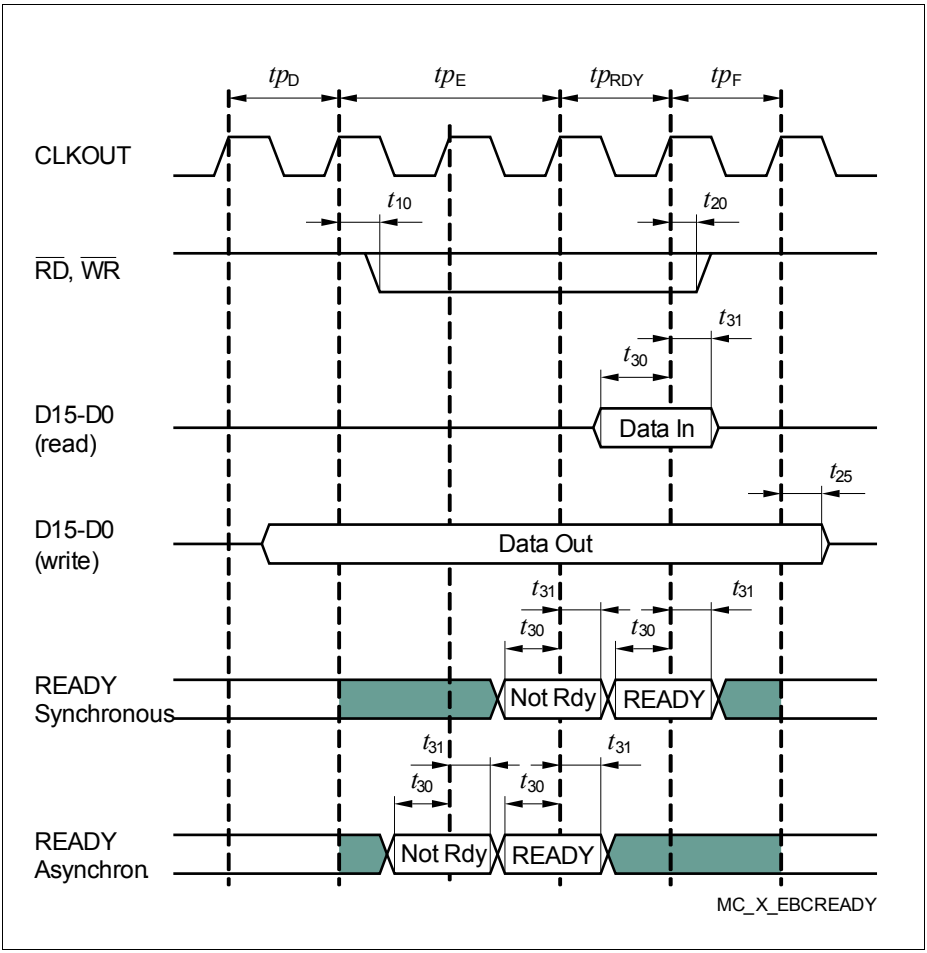

Figure 25 READY Timing

Table 35 USIC SSC Slave Mode Timing for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data input DX0 hold time from clock input DX1 receive edge[1)]	t_{13} SR	5	–	–	ns	
Data output DOUT valid time	t_{14} CC	7	–	33	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

Table 36 is valid under the following conditions: C_L= 20 pF; SSC= slave ; voltage_range= lower

Table 36 USIC SSC Slave Mode Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10} SR	7	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11} SR	7	–	–	ns	
Receive data input setup time to shift clock receive edge[1)]	t_{12} SR	7	–	–	ns	
Data input DX0 hold time from clock input DX1 receive edge[1)]	t_{13} SR	5	–	–	ns	
Data output DOUT valid time	t_{14} CC	8	–	41	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

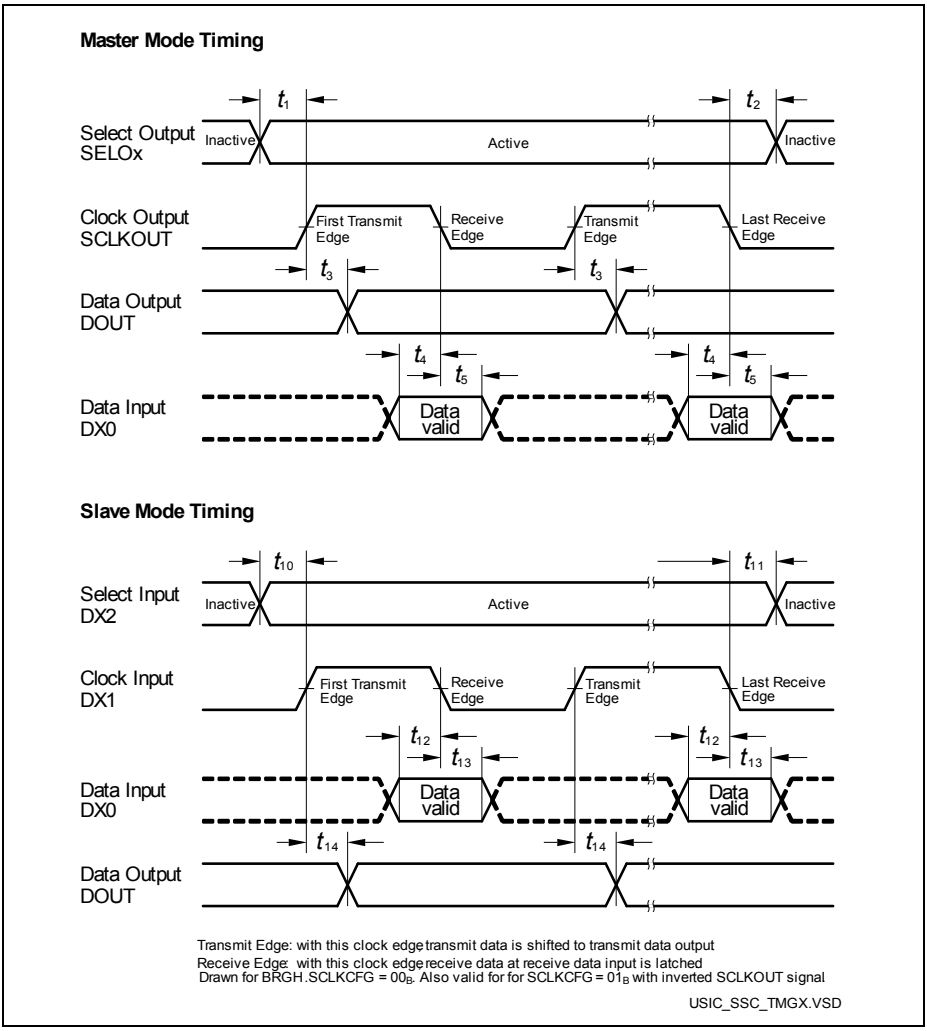

Figure 26 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.

Table 39 JTAG Interface Timing for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK low time	t_3 SR	16	–	–	ns	
TCK clock rise time	t_4 SR	–	–	8	ns	
TCK clock fall time	t_5 SR	–	–	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid from TCK falling edge (propagation delay)[2]	t_8 CC	–	25	29	ns	
TDO high impedance to valid output from TCK falling edge[3][2]	t_9 CC	–	25	29	ns	
TDO valid output to high impedance from TCK falling edge[2]	t_{10} CC	–	25	29	ns	
TDO hold after TCK falling edge[2]	t_{18} CC	5	–	–	ns	

1) Under typical conditions, the JTAG interface can operate at transfer rates up to 20 MHz.
2) The falling edge on TCK is used to generate the TDO timing.
3) The setup time for TDO is given implicitly by the TCK cycle time.

Table 40 is valid under the following conditions: C_L= 20 pF; voltage_range= lower

Table 40 JTAG Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50	–	–	ns	
TCK high time	t_2 SR	16	–	–	ns	
TCK low time	t_3 SR	16	–	–	ns	
TCK clock rise time	t_4 SR	–	–	8	ns	
TCK clock fall time	t_5 SR	–	–	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	