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Details

E·XFI

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34К х 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xe164hn-40f80l-aa

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Tabl	able 5 Pin Definitions and Functions (cont'd)								
Pin	Symbol	Ctrl.	Туре	Function					
39	P2.0	O0 / I	St/B	Bit 0 of Port 2, General Purpose Input/Output					
	AD13	OH / IH	St/B	External Bus Interface Address/Data Line 13					
	RxDC0C	I	St/B	CAN Node 0 Receive Data Input					
	T5INB	I	St/B	GPT12E Timer T5 Count/Gate Input					
40	P2.1	O0 / I	St/B	Bit 1 of Port 2, General Purpose Input/Output					
	TxDC0	01	St/B	CAN Node 0 Transmit Data Output					
	AD14	OH / IH	St/B	External Bus Interface Address/Data Line 14					
	T5EUDB	I	St/B	GPT12E Timer T5 External Up/Down Control Input					
	ESR1_5	I	St/B	ESR1 Trigger Input 5					
41	P2.2	O0 / I	St/B	Bit 2 of Port 2, General Purpose Input/Output					
	TxDC1	01	St/B	CAN Node 1 Transmit Data Output					
	AD15	OH / IH	St/B	External Bus Interface Address/Data Line 15					
	ESR2_5	I	St/B	ESR2 Trigger Input 5					
42	P4.0	O0 / I	St/B	Bit 0 of Port 4, General Purpose Input/Output					
	CC2_CC24	O3 / I	St/B	CAPCOM2 CC24IO Capture Inp./ Compare Out.					
	CS0	OH	St/B	External Bus Interface Chip Select 0 Output					
43	P2.3	O0 / I	St/B	Bit 3 of Port 2, General Purpose Input/Output					
	U0C0_DOUT	01	St/B	USIC0 Channel 0 Shift Data Output					
	CC2_CC16	O3 / I	St/B	CAPCOM2 CC16IO Capture Inp./ Compare Out.					
	A16	ОН	St/B	External Bus Interface Address Line 16					
	ESR2_0	I	St/B	ESR2 Trigger Input 0					
	U0C0_DX0E	I	St/B	USIC0 Channel 0 Shift Data Input					
	U0C1_DX0D	I	St/B	USIC0 Channel 1 Shift Data Input					
	RxDC0A	I	St/B	CAN Node 0 Receive Data Input					



Tabl	Fable 5 Pin Definitions and Functions (cont'd)						
Pin	Symbol	Ctrl.	Туре	Function			
44	P4.1	O0 / I	St/B	Bit 1 of Port 4, General Purpose Input/Output			
	CC2_CC25	O3 / I	St/B	CAPCOM2 CC25IO Capture Inp./ Compare Out.			
	CS1	OH	St/B	External Bus Interface Chip Select 1 Output			
	T4EUDB	I	St/B	GPT12E Timer T4 External Up/Down Control Input			
	ESR1_8	I	St/B	ESR1 Trigger Input 8			
45	P2.4	O0 / I	St/B	Bit 4 of Port 2, General Purpose Input/Output			
	U0C1_DOUT	01	St/B	USIC0 Channel 1 Shift Data Output			
	TxDC0	02	St/B	CAN Node 0 Transmit Data Output			
	CC2_CC17	O3 / I	St/B	CAPCOM2 CC17IO Capture Inp./ Compare Out.			
	A17	OH	St/B	External Bus Interface Address Line 17			
	ESR1_0	I	St/B	ESR1 Trigger Input 0			
	U0C0_DX0F	I	St/B	USIC0 Channel 0 Shift Data Input			
	RxDC1A	I	St/B	CAN Node 1 Receive Data Input			
46	P2.5	O0 / I	St/B	Bit 5 of Port 2, General Purpose Input/Output			
	U0C0_SCLK OUT	01	St/B	USIC0 Channel 0 Shift Clock Output			
	TxDC0	02	St/B	CAN Node 0 Transmit Data Output			
	CC2_CC18	O3 / I	St/B	CAPCOM2 CC18IO Capture Inp./ Compare Out.			
	A18	ОН	St/B	External Bus Interface Address Line 18			
	U0C0_DX1D	I	St/B	USIC0 Channel 0 Shift Clock Input			
	ESR1_10	I	St/B	ESR1 Trigger Input 10			
47	P4.2	O0 / I	St/B	Bit 2 of Port 4, General Purpose Input/Output			
	CC2_CC26	O3 / I	St/B	CAPCOM2 CC26IO Capture Inp./ Compare Out.			
	CS2	OH	St/B	External Bus Interface Chip Select 2 Output			
	T2INA	I	St/B	GPT12E Timer T2 Count/Gate Input			



Table	bit able 5 Pin Definitions and Functions (cont'd)						
Pin	Symbol	Ctrl.	Туре	Function			
62	P10.2	O0 / I	St/B	Bit 2 of Port 10, General Purpose Input/Output			
	U0C0_SCLK OUT	01	St/B	USIC0 Channel 0 Shift Clock Output			
	CCU60_CC6 2	O2	St/B	CCU60 Channel 2 Output			
	AD2	OH / IH	St/B	External Bus Interface Address/Data Line 2			
	CCU60_CC6 2INA	I	St/B	CCU60 Channel 2 Input			
	U0C0_DX1B	I	St/B	USIC0 Channel 0 Shift Clock Input			
63	P0.4	O0 / I	St/B	Bit 4 of Port 0, General Purpose Input/Output			
	U1C1_SELO 0	01	St/B	USIC1 Channel 1 Select/Control 0 Output			
	U1C0_SELO 1	O2	St/B	USIC1 Channel 0 Select/Control 1 Output			
	CCU61_COU T61	O3	St/B	CCU61 Channel 1 Output			
	A4	OH	St/B	External Bus Interface Address Line 4			
	U1C1_DX2A	I	St/B	USIC1 Channel 1 Shift Control Input			
	RxDC1B	I	St/B	CAN Node 1 Receive Data Input			
	ESR2_8	I	St/B	ESR2 Trigger Input 8			
65	P2.13	00 / 1	St/B	Bit 13 of Port 2, General Purpose Input/Output			
	U2C1_SELO 2	01	St/B	USIC2 Channel 1 Select/Control 2 Output			
66	P2.10	00 / 1	St/B	Bit 10 of Port 2, General Purpose Input/Output			
	U0C1_DOUT	01	St/B	USIC0 Channel 1 Shift Data Output			
	U0C0_SELO 3	O2	St/B	USIC0 Channel 0 Select/Control 3 Output			
	CC2_CC23	O3 / I	St/B	CAPCOM2 CC23IO Capture Inp./ Compare Out.			
	A23	OH	St/B	External Bus Interface Address Line 23			
	U0C1_DX0E	I	St/B	USIC0 Channel 1 Shift Data Input			
	CAPINA	I	St/B	GPT12E Register CAPREL Capture Input			



XE164FN, XE164GN, XE164HN, XE164KN XE166 Family / Value Line

General Device Information

Tabl	Table 5 Pin Definitions and Functions (cont'd)								
Pin	Symbol	Ctrl.	Туре	Function					
92	P1.5	O0 / I	St/B	Bit 5 of Port 1, General Purpose Input/Output					
	U1C1_SELO 3	O2	St/B	USIC1 Channel 1 Select/Control 3 Output					
	BRKOUT	O3	St/B	OCDS Break Signal Output					
	A13	OH	St/B	External Bus Interface Address Line 13					
	U2C0_DX0C	I	St/B	USIC2 Channel 0 Shift Data Input					
93	P1.6	O0 / I	St/B	Bit 6 of Port 1, General Purpose Input/Output					
	U1C1_SELO 2	O2	St/B	USIC1 Channel 1 Select/Control 2 Output					
	U2C0_DOUT	O3	St/B	USIC2 Channel 0 Shift Data Output					
	A14	OH	St/B	External Bus Interface Address Line 14					
	U2C0_DX0D	I	St/B	USIC2 Channel 0 Shift Data Input					
94	P1.7	O0 / I	St/B	Bit 7 of Port 1, General Purpose Input/Output					
	U1C1_MCLK OUT	O2	St/B	USIC1 Channel 1 Master Clock Output					
	U2C0_SCLK OUT	O3	St/B	USIC2 Channel 0 Shift Clock Output					
	A15	OH	St/B	External Bus Interface Address Line 15					
	U2C0_DX1C	I	St/B	USIC2 Channel 0 Shift Clock Input					
95	XTAL2	0	Sp/M	Crystal Oscillator Amplifier Output					
96	XTAL1	I	Sp/M	Crystal Oscillator Amplifier Input To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Voltages on XTAL1 must comply to the core supply voltage V_{DDIM} .					
	ESR2_9	I	St/B	ESR2 Trigger Input 9					
97	PORST	1	In/B	Power On Reset Input A low level at this pin resets the XE164xN completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pull-up device will hold this pin high when nothing is driving it.					



Table 5 Pin Definitions and Functions (cont'd)							
Pin	Symbol	Ctrl.	Туре	Function			
98	ESR1	00 / 1	St/B	External Service Request 1 After power-up, an internal weak pull-up device holds this pin high when nothing is driving it.			
	RxDC0E	I	St/B	CAN Node 0 Receive Data Input			
	U1C0_DX0F	I	St/B	USIC1 Channel 0 Shift Data Input			
	U1C0_DX2C	I	St/B	USIC1 Channel 0 Shift Control Input			
	U1C1_DX0C	I	St/B	USIC1 Channel 1 Shift Data Input			
	U1C1_DX2B	I	St/B	USIC1 Channel 1 Shift Control Input			
	U2C1_DX2C	I	St/B	USIC2 Channel 1 Shift Control Input			
99	ESR0	O0 / I	St/B	External Service Request 0 After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.			
	U1C0_DX0E	I	St/B	USIC1 Channel 0 Shift Data Input			
	U1C0_DX2B	I	St/B	USIC1 Channel 0 Shift Control Input			
10	V _{DDIM}	-	PS/M	Digital Core Supply Voltage for Domain M Decouple with a ceramic capacitor, see Data Sheet for details.			
38, 64, 88	V _{DDI1}	-	PS/1	Digital Core Supply Voltage for Domain 1 Decouple with a ceramic capacitor, see Data Sheet for details. All V_{DDI1} pins must be connected to each other.			
14	V _{DDPA}	-	PS/A	Digital Pad Supply Voltage for Domain A Connect decoupling capacitors to adjacent $V_{\text{DDP}}/V_{\text{SS}}$ pin pairs as close as possible to the pins. Note: The A/D_Converters and ports P5, P6 and P15 are fed from supply voltage V_{DDPA} .			



Table 5

XE164FN, XE164GN, XE164HN, XE164KN XE166 Family / Value Line

General Device Information

Pin	Symbol	Ctrl.	Туре	Function					
2, 25, 27, 50	V _{DDPB}	-	PS/B	Digital Pad Supply Voltage for Domain B Connect decoupling capacitors to adjacent $V_{\text{DDP}}/V_{\text{SS}}$ pin pairs as close as possible to the pins.					
52, 75, 77, 100				Note: The on-chip voltage regulators and all ports except P5, P6 and P15 are fed from supply voltage V _{DDPB} .					
1, 26, 51,	V _{SS}	-	PS/	Digital Ground All V_{SS} pins must be connected to the ground-line or ground-plane.					
76			Note: Also the exposed pad is connected internally to V_{SS} . To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground. For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.						

Pin Definitions and Functions (cont'd)

 To generate the reference clock output for bus timing measurement, f_{SYS} must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.



3.3 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instructionfetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.



Figure 5 CPU Block Diagram



Functional Description



Figure 6 CAPCOM Unit Block Diagram



3.9 Capture/Compare Units CCU6x

The XE164xN types feature the CCU60, CCU61 unit(s).

CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for highside and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- · Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

Timer 13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- · Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

Additional Features

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal (CTRAP)
- · Control modes for multi-channel AC drives
- · Output levels can be selected and adapted to the power stage



3.11 Real Time Clock

The Real Time Clock (RTC) module of the XE164xN can be clocked with a clock signal selected from internal sources or external sources (pins).

The RTC basically consists of a chain of divider blocks:

- Selectable 32:1 and 8:1 dividers (on off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL) consisting of: – a reloadable 10-bit timer
 - a reloadable 6-bit timer
 - a reloadable 6-bit timer
 - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.



Figure 10 RTC Block Diagram

Note: The registers associated with the RTC are only affected by a power reset.



3.18 Parallel Ports

The XE164xN provides up to 76 I/O lines which are organized into 7 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in Table 9.

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

Port	Width	I/O	Connected Modules
P0	8	I/O	EBC (A7A0), CCU6, USIC, CAN
P1	8	I/O	EBC (A15A8), CCU6, USIC
P2	14	I/O	EBC (READY, BHE, A23A16, AD15AD13, D15D13), CAN, CC2, GPT12E, USIC, DAP/JTAG
P4	4	I/O	EBC (CS3CS0), CC2, CAN, GPT12E, USIC
P5	11	I	Analog Inputs, CCU6, DAP/JTAG, GPT12E, CAN
P6	3	I/O	ADC, CAN, GPT12E
P7	5	I/O	CAN, GPT12E, SCU, DAP/JTAG, CCU6, ADC, USIC
P10	16	I/O	EBC (ALE, RD, WR, AD12AD0, D12D0), CCU6, USIC, DAP/JTAG, CAN
P15	5	Ι	Analog Inputs, GPT12E

Table 9Summary of the XE164xN's Ports



4.1.1 Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XE164xN. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Note: Typical parameter values refer to room temperature and nominal supply voltage, minimum/maximum parameter values also include conditions of minimum/maximum temperature and minimum/maximum supply voltage. Additional details are described where applicable.

Parameter	Symbol		Values		Unit	Note /
		Min.	Тур.	Max.		Test Condition
Voltage Regulator Buffer Capacitance for DMP_M	$\begin{array}{c} C_{\rm EVRM} \\ {\rm SR} \end{array}$	1.0	-	4.7	μF	1)
Voltage Regulator Buffer Capacitance for DMP_1	$C_{\rm EVR1}$ SR	0.47	-	2.2	μF	2)1)
External Load Capacitance	$C_{L} \operatorname{SR}$	-	20 ³⁾	-	pF	pin out driver= default 4)
System frequency	$f_{\rm SYS}{ m SR}$	-	-	80	MHz	5)
Overload current for analog inputs ⁶⁾	$I_{\rm OVA}{\rm SR}$	-2	-	5	mA	not subject to production test
Overload current for digital inputs ⁶⁾	$I_{\rm OVD}{\rm SR}$	-5	-	5	mA	not subject to production test
Overload current coupling factor for analog inputs ⁷⁾	K _{OVA} CC	-	2.5 x 10 ⁻⁴	1.5 x 10 ⁻³	-	<i>I</i> _{OV} < 0 mA; not subject to production test
		_	1.0 x 10 ⁻⁶	1.0 x 10 ⁻⁴	-	<i>I</i> _{OV} > 0 mA; not subject to production test

Table 12 Operating Conditions



Pullup/Pulldown Device Behavior

Most pins of the XE164xN feature pullup or pulldown devices. For some special pins these are fixed; for the port pins they can be selected by the application.

The specified current values indicate how to load the respective pin depending on the intended signal level. **Figure 13** shows the current paths.

The shaded resistors shown in the figure may be required to compensate system pull currents that do not match the given limit values.



Figure 13 Pullup/Pulldown Current Definition



Table 19ADC Parameters (cont'd)

Parameter	Symbol		Values	;	Unit	Note / Test Condition
		Min.	Тур.	Max.		
Broken wire detection delay against VAGND ²⁾	t _{BWG} CC	-	-	50 ³⁾		
Broken wire detection delay against VAREF ²⁾	t _{BWR} CC	-	-	50 ⁴⁾		
Conversion time for 8-bit result ²⁾	t _{c8} CC	$(11+S)$ $TC) \times$ $t_{ADCI} +$ $2 \times$ t_{SVS}	_	-		
Conversion time for 10-bit result ²⁾	<i>t</i> _{c10} CC	$(13+S)$ $TC) \times$ $t_{ADCI} +$ $2 \times$ t_{SYS}	-	-		
Total Unadjusted Error	TUE CC	_	1	2	LSB	5)
Wakeup time from analog powerdown, fast mode	t _{WAF} CC	-	-	4	μS	
Wakeup time from analog powerdown, slow mode	t _{WAS} CC	-	-	15	μS	
Analog reference ground	V_{AGND} SR	V _{SS} - 0.05	-	1.5	V	
Analog input voltage range	$V_{\rm AIN}{ m SR}$	V_{AGND}	-	V_{AREF}	V	6)
Analog reference voltage	V _{AREF} SR	V _{AGND} + 1.0	-	V _{DDPA} + 0.05	V	

 These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used: C_{AINTtyp} = 12 pF, C_{AINStyp} = 5 pF, R_{AINtyp} = 1.0 kOhm, C_{AREFTtyp} = 15 pF, C_{AREFStyp} = 10 pF, R_{AREFStyp} = 1.0 kOhm.

2) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result. Values for the basic clock t_{ADCI} depend on programming.

3) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 μ s. Result below 10% (66_H)



- This parameter is tested for the fastest and the slowest selection. The medium selections are not subject to production test - verified by design/characterization
- 3) f_{WU} in MHz
- 4) This value includes a hysteresis of approximately 50 mV for rising voltage.
- 5) $V_{\rm LV}$ = selected SWD voltage level
- 6) The limit V_{LV} 0.10 V is valid for the OK1 level. The limit for the OK2 level is V_{LV} 0.15 V.

Conditions for t_{SPO} Timing Measurement

The time required for the transition from **Power-on** to **Base** mode is called t_{SPO} . It is measured under the following conditions:

Precondition: The pad supply is valid, i.e. V_{DDPB} is above 3.0V and remains above 3.0V even though the XE164xN is starting up. No debugger is attached.

Start condition: Power-on reset is removed ($\overline{PORST} = 1$).

End condition: External pin toggle caused by first user instruction executed from FLASH after startup.

Conditions for t_{SSO} Timing Measurement

The time required for the transition from **Stopover** to **Stopover Waked-Up** mode is called t_{SSO} . It is measured under the following conditions:

Precondition: The **Stopover** mode has been entered using the procedure defined in the Programmer's Guide.

Start condition: Pin toggle on ESR pin triggering the startup sequence.

End condition: External pin toggle caused by first user instruction executed from PSRAM after startup.



4.7.2 Definition of Internal Timing

The internal operation of the XE164xN is controlled by the internal system clock f_{SYS} .

Because the system clock signal $f_{\rm SYS}$ can be generated from a number of internal and external sources using different mechanisms, the duration of the system clock periods (TCSs) and their variation (as well as the derived external timing) depend on the mechanism used to generate $f_{\rm SYS}$. This must be considered when calculating the timing for the XE164xN.



Figure 19 Generation Mechanisms for the System Clock

Note: The example of PLL operation shown in **Figure 19** uses a PLL factor of 1:4; the example of prescaler operation uses a divider factor of 2:1.

The specification of the external timing (AC Characteristics) depends on the period of the system clock (TCS).



Direct Drive

When direct drive operation is selected (SYSCON0.CLKSEL = 11_B), the system clock is derived directly from the input clock signal CLKIN1:

 $f_{\text{SYS}} = f_{\text{IN}}.$

The frequency of f_{SYS} is the same as the frequency of f_{IN} . In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{IN} .

Selecting Bypass Operation from the XTAL1¹⁾ input and using a divider factor of 1 results in a similar configuration.

Prescaler Operation

When prescaler operation is selected (SYSCON0.CLKSEL = 10_B , PLLCON0.VCOBY = 1_B), the system clock is derived either from the crystal oscillator (input clock signal XTAL1) or from the internal clock source through the output prescaler K1 (= K1DIV+1):

 $f_{\text{SYS}} = f_{\text{OSC}} / \text{K1}.$

If a divider factor of 1 is selected, the frequency of $f_{\rm SYS}$ equals the frequency of $f_{\rm OSC}$. In this case the high and low times of $f_{\rm SYS}$ are determined by the duty cycle of the input clock $f_{\rm OSC}$ (external or internal).

The lowest system clock frequency results from selecting the maximum value for the divider factor K1:

 $f_{\rm SYS} = f_{\rm OSC} / 1024.$

4.7.2.1 Phase Locked Loop (PLL)

When PLL operation is selected (SYSCON0.CLKSEL = 10_B , PLLCON0.VCOBY = 0_B), the on-chip phase locked loop is enabled and provides the system clock. The PLL multiplies the input frequency by the factor **F** ($f_{SYS} = f_{IN} \times F$).

F is calculated from the input divider P (= PDIV+1), the multiplication factor N (= NDIV+1), and the output divider K2 (= K2DIV+1):

 $(F = N / (P \times K2)).$

The input clock can be derived either from an external source at XTAL1 or from the onchip clock source.

The PLL circuit synchronizes the system clock to the input clock. This synchronization is performed smoothly so that the system clock frequency does not change abruptly.

Adjustment to the input clock continuously changes the frequency of f_{SYS} so that it is locked to f_{IN} . The slight variation causes a jitter of f_{SYS} which in turn affects the duration of individual TCSs.

¹⁾ Voltages on XTAL1 must comply to the core supply voltage V_{DDIM} .



Parameter	Symbol		Value	S	Unit	Note /
	-	Min.	Тур.	Max.	_	Test Condition
DAP0 clock period ¹⁾	<i>t</i> ₁₁ SR	25	-	-	ns	
DAP0 high time	t ₁₂ SR	8	-	-	ns	
DAP0 low time ¹⁾	t ₁₃ SR	8	-	-	ns	
DAP0 clock rise time	t ₁₄ SR	-	-	4	ns	
DAP0 clock fall time	t ₁₅ SR	-	-	4	ns	
DAP1 setup to DAP0 rising edge	<i>t</i> ₁₆ SR	6	-	-	ns	
DAP1 hold after DAP0 rising edge	<i>t</i> ₁₇ SR	6	-	-	ns	
DAP1 valid per DAP0 clock period ²⁾	<i>t</i> ₁₉ CC	12	17	-	ns	

Table 38 DAP Interface Timing for Lower Voltage Range

1) See the DAP chapter for clock rate restrictions in the Active::IDLE protocol state.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.



Figure 27 Test Clock Timing (DAP0)



Package and Reliability

5.2 Thermal Considerations

When operating the XE164xN in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The "Thermal resistance $R_{\Theta JA}$ " quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta,IA}$

The internal power consumption is defined as

 $P_{\text{INT}} = V_{\text{DDP}} \times I_{\text{DDP}}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as $P_{\text{IOSTAT}} = \Sigma((V_{\text{DDP}}-V_{\text{OH}}) \times I_{\text{OH}}) + \Sigma(V_{\text{OL}} \times I_{\text{OL}})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP} , if possible in the system
- · Reduce the system frequency
- · Reduce the number of output pins
- Reduce the load on active output drivers



Package and Reliability

5.3 Quality Declarations

The operation lifetime of the XE164xN depends on the operating temperature. The life time decreases with increasing temperature as shown in **Table 43**.

Table 42 Quality Parameters

Parameter	Symbol		Values		Unit	Note /
		Min.	Тур.	Max.		Test Condition
Operation lifetime	t _{OP} CC	-	-	20	а	See Table 43
ESD susceptibility according to Human Body Model (HBM)	$V_{\rm HBM}$ SR	-	-	2 000	V	EIA/JESD22- A114-B
Moisture sensitivity level	MSL CC	-	-	3	_	JEDEC J-STD-020C

Table 43 Lifetime dependency from Temperature

Operating Time	Operating Temperature
20 a	$T_{\rm J} \leq 110^{\circ}{\rm C}$
95 500 h	<i>T</i> _J = 120°C
68 500 h	$T_{\rm J} = 125^{\circ}{\rm C}$
49 500 h	$T_{\rm J} = 130^{\circ}{\rm C}$
26 400 h	$T_{\rm J} = 140^{\circ}{\rm C}$
14 500 h	$T_{\rm J} = 150^{\circ}{\rm C}$