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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	18K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xe164kn-16f80l-aa

Summary of Features

The XE164xN types are offered with several SRAM memory sizes. **Figure 1** shows the allocation rules for PSRAM and DSRAM. Note that the rules differ:

- PSRAM allocation starts from the **lower** address
- DSRAM allocation starts from the **higher** address

For example 8 Kbytes of PSRAM will be allocated at E0'0000h-E0'1FFFh and 8 Kbytes of DSRAM will be at 00'C000h-00'DFFFh.

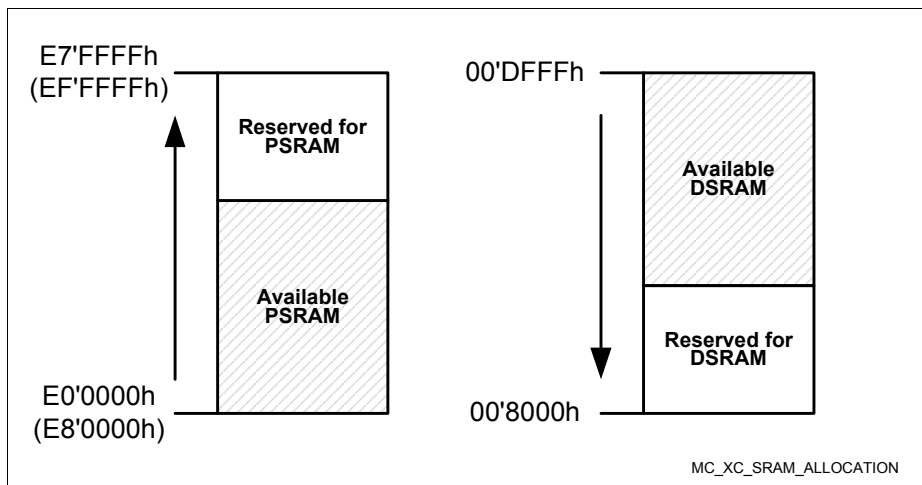


Figure 1 **SRAM Allocation**

Key to Pin Definitions

- **Ctrl.:** The output signal for a port pin is selected by bit field PC in the associated register Px_IOCry. Output O0 is selected by setting the respective bit field PC to 1x00_B, output O1 is selected by 1x01_B, etc.
Output signal OH is controlled by hardware.
- **Type:** Indicates the pad type and its power supply domain (A, B, M, 1).
 - St: Standard pad
 - Sp: Special pad e.g. XTALx
 - DP: Double pad - can be used as standard or high speed pad
 - In: Input only pad
 - PS: Power supply pad

Table 5 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
3	$\overline{\text{TESTM}}$	I	In/B	Testmode Enable Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pull-up device will hold this pin high when nothing is driving it.
4	P7.2	O0 / I	St/B	Bit 2 of Port 7, General Purpose Input/Output
	EMUX0	O1	St/B	External Analog MUX Control Output 0 (ADC1)
	TDI_C	IH	St/B	JTAG Test Data Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
5	$\overline{\text{TRST}}$	I	In/B	Test-System Reset Input For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XE164xN's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pull-down device will hold this pin low when nothing is driving it.

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
6	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output
	T3OUT	O1	St/B	GPT12E Timer T3 Toggle Latch Output
	T6OUT	O2	St/B	GPT12E Timer T6 Toggle Latch Output
	TDO_A	OH / IH	St/B	JTAG Test Data Output / DAP1 Input/Output If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	ESR2_1	I	St/B	ESR2 Trigger Input 1
7	P7.3	O0 / I	St/B	Bit 3 of Port 7, General Purpose Input/Output
	EMUX1	O1	St/B	External Analog MUX Control Output 1 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_DOUT	O3	St/B	USIC0 Channel 0 Shift Data Output
	TMS_C	IH	St/B	JTAG Test Mode Selection Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	U0C1_DX0F	I	St/B	USIC0 Channel 1 Shift Data Input
8	P7.1	O0 / I	St/B	Bit 1 of Port 7, General Purpose Input/Output
	EXTCLK	O1	St/B	Programmable Clock Signal Output
	BRKIN_C	I	St/B	OCDS Break Signal Input
9	P7.4	O0 / I	St/B	Bit 4 of Port 7, General Purpose Input/Output
	EMUX2	O1	St/B	External Analog MUX Control Output 2 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C1_SCLK OUT	O3	St/B	USIC0 Channel 1 Shift Clock Output
	TCK_C	IH	St/B	DAP0/JTAG Clock Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	U0C0_DX0D	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX1E	I	St/B	USIC0 Channel 1 Shift Clock Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
79	P10.8	O0 / I	St/B	Bit 8 of Port 10, General Purpose Input/Output
	U0C0_MCLK OUT	O1	St/B	USIC0 Channel 0 Master Clock Output
	U0C1_SELO 0	O2	St/B	USIC0 Channel 1 Select/Control 0 Output
	U2C1_DOUT	O3	St/B	USIC2 Channel 1 Shift Data Output
	AD8	OH / IH	St/B	External Bus Interface Address/Data Line 8
	CCU60_CCP OS1A	I	St/B	CCU60 Position Input 1
	U0C0_DX1C	I	St/B	USIC0 Channel 0 Shift Clock Input
	BRKIN_B	I	St/B	OCDS Break Signal Input
80	T3EUDB	I	St/B	GPT12E Timer T3 External Up/Down Control Input
	P10.9	O0 / I	St/B	Bit 9 of Port 10, General Purpose Input/Output
	U0C0_SELO 4	O1	St/B	USIC0 Channel 0 Select/Control 4 Output
	U0C1_MCLK OUT	O2	St/B	USIC0 Channel 1 Master Clock Output
	AD9	OH / IH	St/B	External Bus Interface Address/Data Line 9
	CCU60_CCP OS2A	I	St/B	CCU60 Position Input 2
	TCK_B	I/H	St/B	DAP0/JTAG Clock Input If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	T3INB	I	St/B	GPT12E Timer T3 Count/Gate Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
98	ESR1	O0 / I	St/B	External Service Request 1 After power-up, an internal weak pull-up device holds this pin high when nothing is driving it.
	RxDC0E	I	St/B	CAN Node 0 Receive Data Input
	U1C0_DX0F	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX2C	I	St/B	USIC1 Channel 0 Shift Control Input
	U1C1_DX0C	I	St/B	USIC1 Channel 1 Shift Data Input
	U1C1_DX2B	I	St/B	USIC1 Channel 1 Shift Control Input
	U2C1_DX2C	I	St/B	USIC2 Channel 1 Shift Control Input
99	ESR0	O0 / I	St/B	External Service Request 0 After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.
	U1C0_DX0E	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX2B	I	St/B	USIC1 Channel 0 Shift Control Input
10	V_{DDIM}	-	PS/M	Digital Core Supply Voltage for Domain M Decouple with a ceramic capacitor, see Data Sheet for details.
38, 64, 88	V_{DDI1}	-	PS/1	Digital Core Supply Voltage for Domain 1 Decouple with a ceramic capacitor, see Data Sheet for details. All V_{DDI1} pins must be connected to each other.
14	V_{DDPA}	-	PS/A	Digital Pad Supply Voltage for Domain A Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. <i>Note: The A/D Converters and ports P5, P6 and P15 are fed from supply voltage V_{DDPA}.</i>

Functional Description

Up to 16 Kbytes of on-chip Data SRAM (DSRAM) are used for storage of general user data. The DSRAM is accessed via a separate interface and is optimized for data access.

Note: The actual size of the DSRAM depends on the quoted device type.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, ..., RL7, RH7) General Purpose Registers (GPRs).

The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

8 Kbytes of on-chip Stand-By SRAM (SBRAM) provide storage for system-relevant user data that must be preserved while the major part of the device is powered down. The SBRAM is accessed via a specific interface and is powered in domain M.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XE166 Family. In order to ensure upward compatibility they should either not be accessed or written with zeros.

In order to meet the requirements of designs where more memory is required than is available on chip, up to 12 Mbytes (approximately, see [Table 7](#)) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

The on-chip Flash memory stores code, constant data, and control data. The 320 Kbytes of on-chip Flash memory consist of 1 module of 64 Kbytes (preferably for data storage) and 1 module of 256 Kbytes. Each module is organized in 4-Kbyte sectors. The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

Note: The actual size of the Flash memory depends on the chosen device type.

Each sector can be separately write protected¹⁾, erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.

For Flash parameters, please see [Section 4.6](#).

¹⁾ To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

3.3 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.

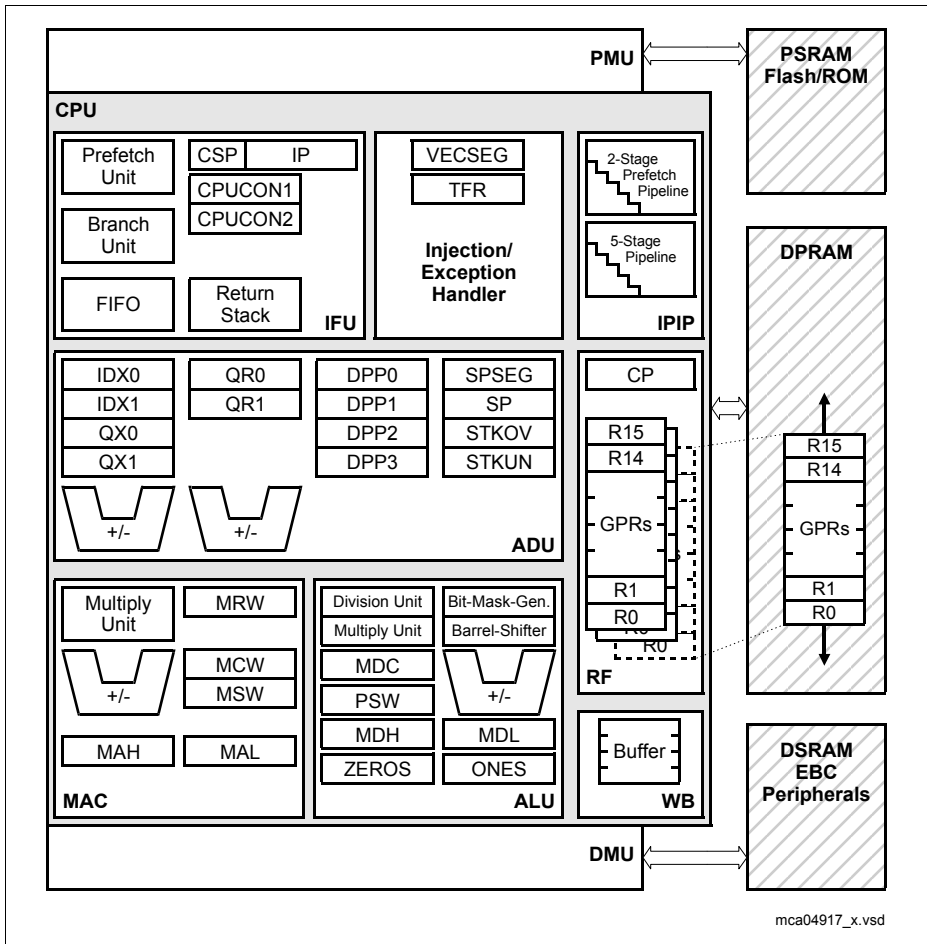


Figure 5 CPU Block Diagram

3.4 Memory Protection Unit (MPU)

The XE164xN's Memory Protection Unit (MPU) protects user-specified memory areas from unauthorized read, write, or instruction fetch accesses. The MPU can protect the whole address space including the peripheral area. This completes established mechanisms such as the register security mechanism or stack overrun/underrun detection.

Four Protection Levels support flexible system programming where operating system, low level drivers, and applications run on separate levels. Each protection level permits different access restrictions for instructions and/or data.

Every access is checked (if the MPU is enabled) and an access violating the permission rules will be marked as invalid and leads to a protection trap.

A set of protection registers for each protection level specifies the address ranges and the access permissions. Applications requiring more than 4 protection levels can dynamically re-program the protection registers.

3.5 Memory Checker Module (MCHK)

The XE164xN's Memory Checker Module calculates a checksum (fractional polynomial division) on a block of data, often called Cyclic Redundancy Code (CRC). It is based on a 32-bit linear feedback shift register and may, therefore, also be used to generate pseudo-random numbers.

The Memory Checker Module is a 16-bit parallel input signature compression circuitry which enables error detection within a block of data stored in memory, registers, or communicated e.g. via serial communication lines. It reduces the probability of error masking due to repeated error patterns by calculating the signature of blocks of data.

The polynomial used for operation is configurable, so most of the commonly used polynomials may be used. Also, the block size for generating a CRC result is configurable via a local counter. An interrupt may be generated if testing the current data block reveals an error.

An autonomous CRC compare circuitry is included to enable redundant error detection, e.g. to enable higher safety integrity levels.

The Memory Checker Module provides enhanced fault detection (beyond parity or ECC) for data and instructions in volatile and non volatile memories. This is especially important for the safety and reliability of embedded systems.

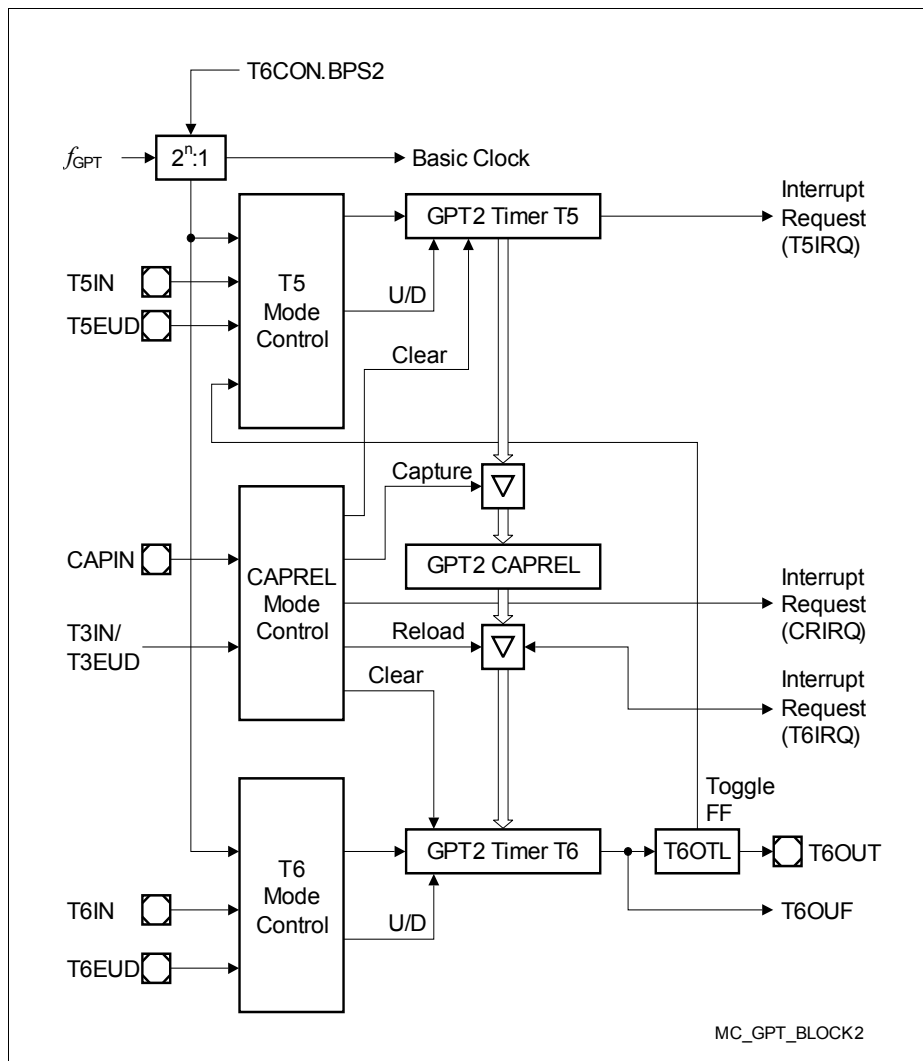


Figure 9 Block Diagram of GPT2

3.18 Parallel Ports

The XE164xN provides up to 76 I/O lines which are organized into 7 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in [Table 9](#).

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

Table 9 Summary of the XE164xN's Ports

Port	Width	I/O	Connected Modules
P0	8	I/O	EBC (A7...A0), CCU6, USIC, CAN
P1	8	I/O	EBC (A15...A8), CCU6, USIC
P2	14	I/O	EBC (READY, $\overline{\text{BHE}}$, A23...A16, AD15...AD13, D15...D13), CAN, CC2, GPT12E, USIC, DAP/JTAG
P4	4	I/O	EBC ($\overline{\text{CS3}}$... $\overline{\text{CS0}}$), CC2, CAN, GPT12E, USIC
P5	11	I	Analog Inputs, CCU6, DAP/JTAG, GPT12E, CAN
P6	3	I/O	ADC, CAN, GPT12E
P7	5	I/O	CAN, GPT12E, SCU, DAP/JTAG, CCU6, ADC, USIC
P10	16	I/O	EBC (ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, AD12...AD0, D12...D0), CCU6, USIC, DAP/JTAG, CAN
P15	5	I	Analog Inputs, GPT12E

4.1.1 Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XE164xN. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Note: Typical parameter values refer to room temperature and nominal supply voltage, minimum/maximum parameter values also include conditions of minimum/maximum temperature and minimum/maximum supply voltage. Additional details are described where applicable.

Table 12 Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage Regulator Buffer Capacitance for DMP_M	C_{EVRM} SR	1.0	—	4.7	μF	¹⁾
Voltage Regulator Buffer Capacitance for DMP_1	C_{EVR1} SR	0.47	—	2.2	μF	²⁾¹⁾
External Load Capacitance	C_L SR	—	20 ³⁾	—	pF	pin out driver= default ⁴⁾
System frequency	f_{SYS} SR	—	—	80	MHz	⁵⁾
Overload current for analog inputs ⁶⁾	I_{OVA} SR	-2	—	5	mA	not subject to production test
Overload current for digital inputs ⁶⁾	I_{OVD} SR	-5	—	5	mA	not subject to production test
Overload current coupling factor for analog inputs ⁷⁾	K_{OVA} CC	—	2.5×10^{-4}	1.5×10^{-3}	—	$I_{OV} < 0$ mA; not subject to production test
		—	1.0×10^{-6}	1.0×10^{-4}	—	$I_{OV} > 0$ mA; not subject to production test

4.3 DC Parameters

These parameters are static or average values that may be exceeded during switching transitions (e.g. output current).

The XE164xN can operate within a wide supply voltage range from 3.0 V to 5.5 V. However, during operation this supply voltage must remain within 10 percent of the selected nominal supply voltage. It cannot vary across the full operating voltage range.

Because of the supply voltage restriction and because electrical behavior depends on the supply voltage, the parameters are specified separately for the upper and the lower voltage range.

During operation, the supply voltages may only change with a maximum speed of $dV/dt < 1 \text{ V/ms}$.

Leakage current is strongly dependent on the operating temperature and the voltage level at the respective pin. The maximum values in the following tables apply under worst case conditions, i.e. maximum temperature and an input level equal to the supply voltage.

The value for the leakage current in an application can be determined by using the respective leakage derating formula (see tables) with values from that application.

The pads of the XE164xN are designed to operate in various driver modes. The DC parameter specifications refer to the pad current limits specified in [Section 4.7.4](#).

Electrical Parameters

4.3.1 DC Parameters for Upper Voltage Area

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV} .

Note: Operating Conditions apply.

Table 15 is valid under the following conditions: $V_{DDP} \leq 5.5 \text{ V}$; $V_{DDP} \text{ typ. } 5 \text{ V}$; $V_{DDP} \geq 4.5 \text{ V}$

Table 15 DC Characteristics for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs). To be doubled for double bond pins. ¹⁾	$C_{IO} \text{ CC}$	–	–	10	pF	not subject to production test
Input Hysteresis ²⁾	$HYS \text{ CC}$	$0.11 \times V_{DDP}$	–	–	V	$R_S = 0 \text{ Ohm}$
Absolute input leakage current on pins of analog ports ³⁾	$ I_{OZ1} \text{ CC}$	–	10	200	nA	$V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Absolute input leakage current for all other pins. To be doubled for double bond pins. ³⁾¹⁾⁴⁾	$ I_{OZ2} \text{ CC}$	–	0.2	5	μA	$T_J \leq 110 \text{ }^\circ\text{C}$; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
		–	0.2	15	μA	$T_J \leq 150 \text{ }^\circ\text{C}$; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Pull Level Force Current ⁵⁾	$ I_{PLF} \text{ SR}$	250	–	–	μA	$V_{IN} \geq V_{IHmin}(\text{pull down_enabled})$; $V_{IN} \leq \bar{V}_{ILmax}(\text{pull up_enabled})$
Pull Level Keep Current ⁶⁾	$ I_{PLK} \text{ SR}$	–	–	30	μA	$V_{IN} \geq V_{IHmin}(\text{pull up_enabled})$; $V_{IN} \leq V_{ILmax}(\text{pull down_enabled})$
Input high voltage (all except XTAL1)	$V_{IH} \text{ SR}$	$0.7 \times V_{DDP}$	–	$V_{DDP} + 0.3$	V	
Input low voltage (all except XTAL1)	$V_{IL} \text{ SR}$	-0.3	–	$0.3 \times V_{DDP}$	V	

Electrical Parameters

Table 19 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Broken wire detection delay against VAGND ²⁾	t_{BWG} CC	—	—	50 ³⁾		
Broken wire detection delay against VAREF ²⁾	t_{BWR} CC	—	—	50 ⁴⁾		
Conversion time for 8-bit result ²⁾	t_{c8} CC	$(11+S \cdot TC) \times t_{ADCI} + 2 \times t_{SYS}$	—	—		
Conversion time for 10-bit result ²⁾	t_{c10} CC	$(13+S \cdot TC) \times t_{ADCI} + 2 \times t_{SYS}$	—	—		
Total Unadjusted Error	TUE CC	—	1	2	LSB	⁵⁾
Wakeup time from analog powerdown, fast mode	t_{WAF} CC	—	—	4	μs	
Wakeup time from analog powerdown, slow mode	t_{WAS} CC	—	—	15	μs	
Analog reference ground	V_{AGND} SR	$V_{SS} - 0.05$	—	1.5	V	
Analog input voltage range	V_{AIN} SR	V_{AGND}	—	V_{AREF}	V	⁶⁾
Analog reference voltage	V_{AREF} SR	$V_{AGND} + 1.0$	—	$V_{DDPA} + 0.05$	V	

1) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used: $C_{AINTyp} = 12$ pF, $C_{AINStyp} = 5$ pF, $R_{AINTyp} = 1.0$ kOhm, $C_{AREFTyp} = 15$ pF, $C_{AREFStyp} = 10$ pF, $R_{AREFTyp} = 1.0$ kOhm.

2) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result. Values for the basic clock t_{ADCI} depend on programming.

3) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 μs. Result below 10% (66μ)

4.5 System Parameters

The following parameters specify several aspects which are important when integrating the XE164xN into an application system.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 21 Various System Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Short-term deviation of internal clock source frequency ¹⁾	Δf_{INT} CC	-1	—	1	%	$\Delta T_J \leq 10^\circ\text{C}$
Internal clock source frequency	f_{INT} CC	4.8	5.0	5.2	MHz	
Wakeup clock source frequency ²⁾	f_{WU} CC	400	—	700	kHz	FREQSEL= 00
		210	—	390	kHz	FREQSEL= 01
		140	—	260	kHz	FREQSEL= 10
		110	—	200	kHz	FREQSEL= 11
Startup time from power-on with code execution from Flash	t_{SPO} CC	1.5	2.0	2.4	ms	$f_{\text{WU}} = 500 \text{ kHz}$
Startup time from stopover mode with code execution from PSRAM	t_{SSO} CC	11 / $f_{\text{WU}}^{3)}$	—	12 / $f_{\text{WU}}^{3)}$	μs	
Core voltage (PVC) supervision level	V_{PVC} CC	$V_{\text{LV}} - 0.03$	V_{LV}	$V_{\text{LV}} + 0.07^{4)}$	V	⁵⁾
Supply watchdog (SWD) supervision level	V_{SWD} CC	$V_{\text{LV}} - 0.10^{6)}$	V_{LV}	$V_{\text{LV}} + 0.15$	V	voltage_range= lower ⁵⁾
		$V_{\text{LV}} - 0.15$	V_{LV}	$V_{\text{LV}} + 0.15$	V	voltage_range= upper ⁵⁾
		$V_{\text{LV}} - 0.30$	V_{LV}	$V_{\text{LV}} + 0.30$	V	$V_{\text{LV}} = 5.5 \text{ V}^{5)}$

1) The short-term frequency deviation refers to a timeframe of a few hours and is measured relative to the current frequency at the beginning of the respective timeframe. This parameter is useful to determine a time span for re-triggering a LIN synchronization.

Electrical Parameters

- 2) Flash module 1 can be erased/programmed while code is executed and/or data is read from Flash module 0.
- 3) Value of IMB_IMBCTRL.WSFLASH.
- 4) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticeably only at extremely low system clock frequencies.

Access to the XE164xN Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

Electrical Parameters

- 1) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF} . This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1} .
- 2) Overload conditions must not occur on pin XTAL1.

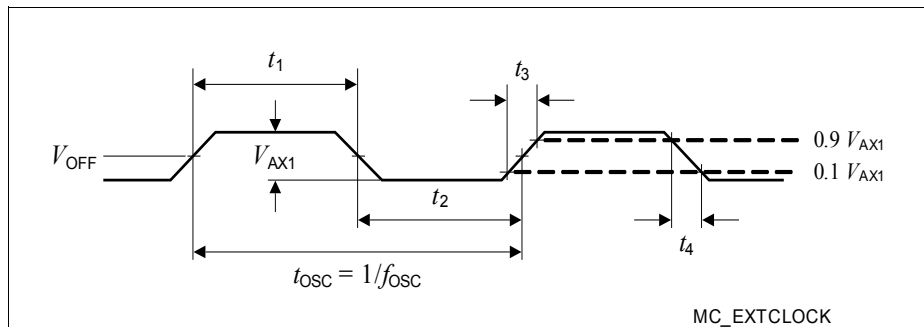


Figure 21 External Clock Drive XTAL1

Note: For crystal or ceramic resonator operation, it is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for oscillator operation.

The manufacturers of crystals and ceramic resonators offer an oscillator evaluation service. This evaluation checks the crystal/resonator specification limits to ensure a reliable oscillator operation.

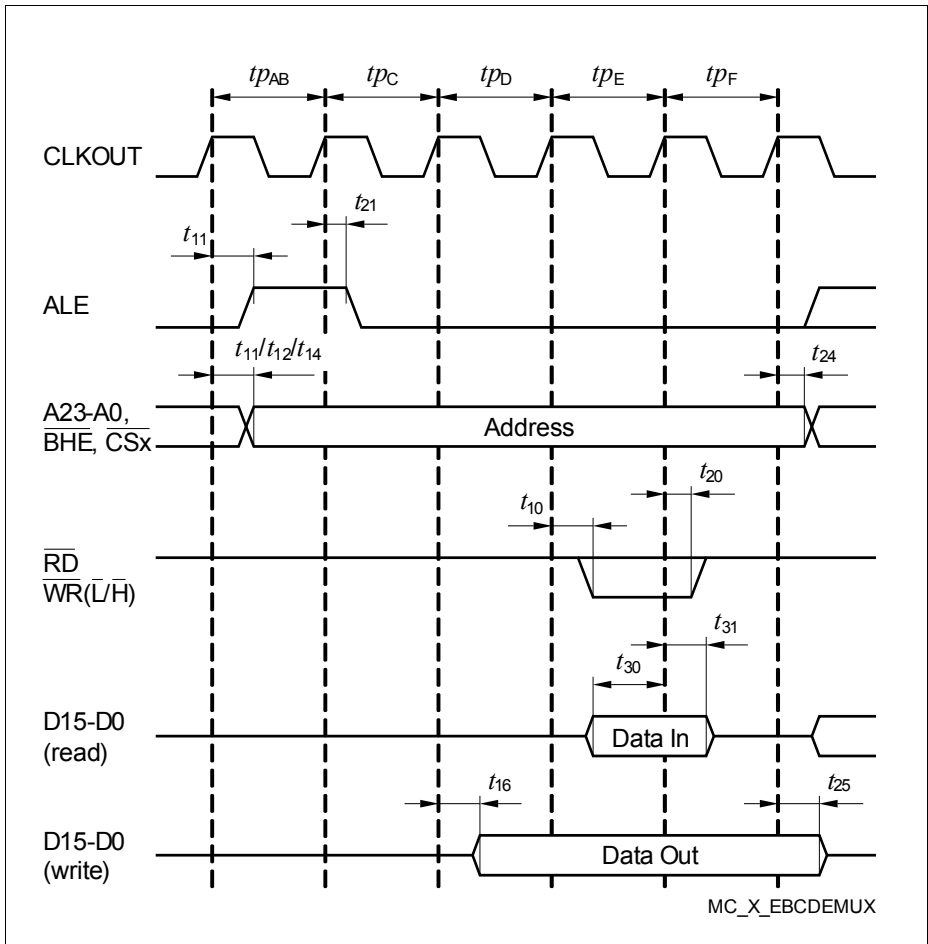


Figure 24 Demultiplexed Bus Cycle

4.7.5.1 Bus Cycle Control with the READY Input

The duration of an external bus cycle can be controlled by the external circuit using the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

An asynchronous READY signal puts no timing constraints on the input signal but incurs a minimum of one waitstate due to the additional synchronization stage. The minimum

Table 34 USIC SSC Master Mode Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	$t_{\text{SYS}} - 10^{1)}$	—	—	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	$t_{\text{SYS}} - 9^{1)}$	—	—	ns	
Data output DOUT valid time	t_3 CC	-7	—	11	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	40	—	—	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-5	—	—	ns	

1) $t_{\text{SYS}} = 1 / f_{\text{SYS}}$

Table 35 is valid under the following conditions: $C_L = 20$ pF; SSC= slave ; voltage_range= upper

Table 35 USIC SSC Slave Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge ¹⁾	t_{10} SR	7	—	—	ns	
Select input DX2 hold after last clock input DX1 receive edge ¹⁾	t_{11} SR	7	—	—	ns	
Receive data input setup time to shift clock receive edge ¹⁾	t_{12} SR	7	—	—	ns	

Electrical Parameters

Table 35 USIC SSC Slave Mode Timing for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data input DX0 hold time from clock input DX1 receive edge ¹⁾	t_{13} SR	5	—	—	ns	
Data output DOUT valid time	t_{14} CC	7	—	33	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

Table 36 is valid under the following conditions: $C_L = 20$ pF; SSC= slave ; voltage_range= lower

Table 36 USIC SSC Slave Mode Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge ¹⁾	t_{10} SR	7	—	—	ns	
Select input DX2 hold after last clock input DX1 receive edge ¹⁾	t_{11} SR	7	—	—	ns	
Receive data input setup time to shift clock receive edge ¹⁾	t_{12} SR	7	—	—	ns	
Data input DX0 hold time from clock input DX1 receive edge ¹⁾	t_{13} SR	5	—	—	ns	
Data output DOUT valid time	t_{14} CC	8	—	41	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).