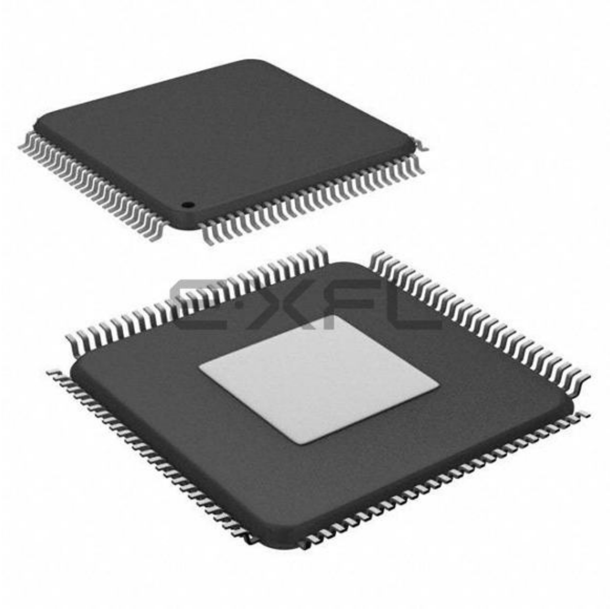

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Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	18K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe164fn16f80laafxuma1

XE164xN Data Sheet
Revision History: V1.4 2013-02

Previous Versions:
V1.3, 2011-07
V1.2, 2010-04
V1.1, 2009-07
V1.0, 2009-03 Preliminary

Page	Subjects (major changes since last revision)
36	Added AB step marking.
87	Errata SWD_X.P002 implemented: V_{SWD} tolerance boundaries for 5.5 V are changed.
89	Clarified “Coding of bit fields LEVxV” descriptions. Matched with Operating Conditions: marked some coding values “out of valid operation range”.
90	Errata FLASH_X.P001 implemented: Test Condition for Flash parameter N_{ER} corrected

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2.1 Pin Configuration and Definition

The pins of the XE164xN are described in detail in **Table 5**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.

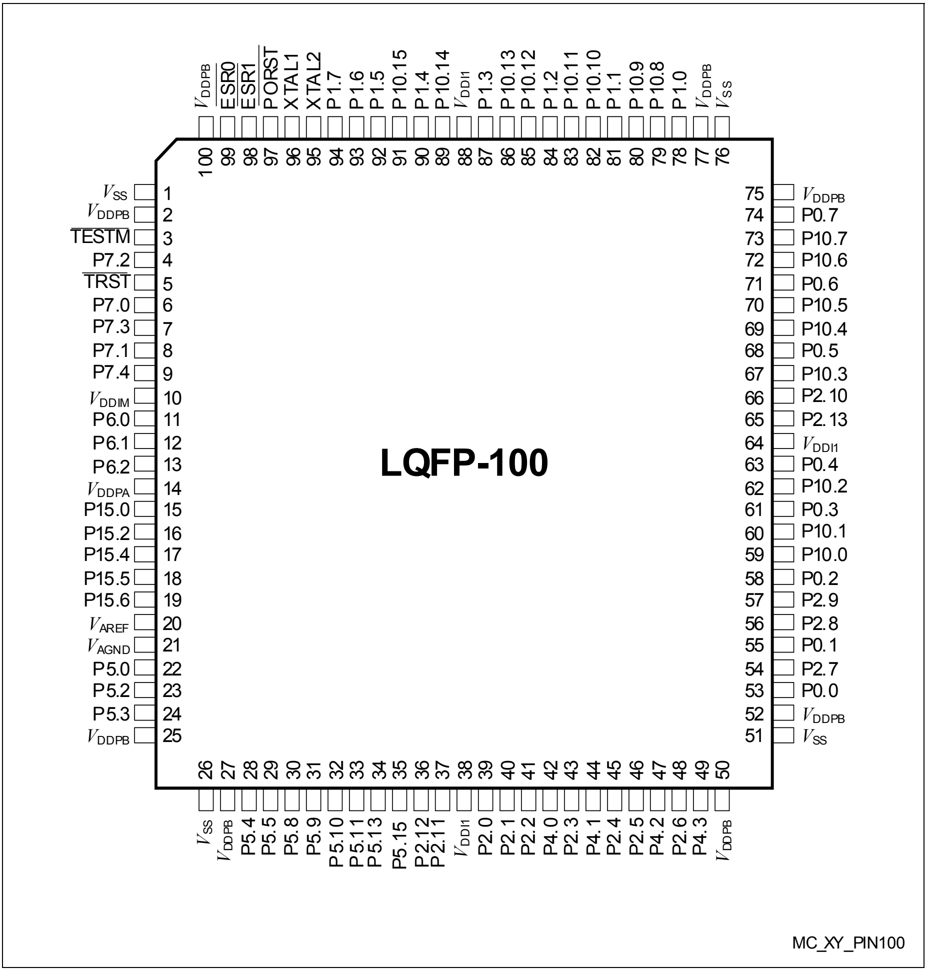

Figure 3 XE164xN Pin Configuration (top view)

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
6	P7.0	O0 / I	St/B	**Bit 0 of Port 7, General Purpose Input/Output**
	T3OUT	O1	St/B	**GPT12E Timer T3 Toggle Latch Output**
	T6OUT	O2	St/B	**GPT12E Timer T6 Toggle Latch Output**
	TDO_A	OH / IH	St/B	**JTAG Test Data Output / DAP1 Input/Output** If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	ESR2_1	I	St/B	**ESR2 Trigger Input 1**
7	P7.3	O0 / I	St/B	**Bit 3 of Port 7, General Purpose Input/Output**
	EMUX1	O1	St/B	**External Analog MUX Control Output 1 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_DOUT	O3	St/B	**USIC0 Channel 0 Shift Data Output**
	TMS_C	IH	St/B	**JTAG Test Mode Selection Input** If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	U0C1_DX0F	I	St/B	**USIC0 Channel 1 Shift Data Input**
8	P7.1	O0 / I	St/B	**Bit 1 of Port 7, General Purpose Input/Output**
	EXTCLK	O1	St/B	**Programmable Clock Signal Output**
	$\overline{\text{BRKIN\_C}}$	I	St/B	**OCDS Break Signal Input**
9	P7.4	O0 / I	St/B	**Bit 4 of Port 7, General Purpose Input/Output**
	EMUX2	O1	St/B	**External Analog MUX Control Output 2 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C1_SCLKOUT	O3	St/B	**USIC0 Channel 1 Shift Clock Output**
	TCK_C	IH	St/B	**DAP0/JTAG Clock Input** If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	U0C0_DX0D	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX1E	I	St/B	**USIC0 Channel 1 Shift Clock Input**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
48	P2.6	O0 / I	St/B	**Bit 6 of Port 2, General Purpose Input/Output**
	U0C0_SELO0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	U0C1_SELO1	O2	St/B	**USIC0 Channel 1 Select/Control 1 Output**
	CC2_CC19	O3 / I	St/B	**CAPCOM2 CC19IO Capture Inp./ Compare Out.**
	A19	OH	St/B	**External Bus Interface Address Line 19**
	U0C0_DX2D	I	St/B	**USIC0 Channel 0 Shift Control Input**
	RxDC0D	I	St/B	**CAN Node 0 Receive Data Input**
	ESR2_6	I	St/B	**ESR2 Trigger Input 6**
49	P4.3	O0 / I	St/B	**Bit 3 of Port 4, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CC2_CC27	O3 / I	St/B	**CAPCOM2 CC27IO Capture Inp./ Compare Out.**
	$\overline{\mathrm{CS3}}$	OH	St/B	**External Bus Interface Chip Select 3 Output**
	T2EUDA	I	St/B	**GPT12E Timer T2 External Up/Down Control Input**
53	P0.0	O0 / I	St/B	**Bit 0 of Port 0, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	CCU61_CC60	O3	St/B	**CCU61 Channel 0 IOutput**
	A0	OH	St/B	**External Bus Interface Address Line 0**
	U1C0_DX0A	I	St/B	**USIC1 Channel 0 Shift Data Input**
	CCU61_CC60INA	I	St/B	**CCU61 Channel 0 Input**
	ESR1_11	I	St/B	**ESR1 Trigger Input 11**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
67	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COUT60	O2	St/B	**CCU60 Channel 0 Output**
	AD3	OH / IH	St/B	**External Bus Interface Address/Data Line 3**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
68	P0.5	O0 / I	St/B	**Bit 5 of Port 0, General Purpose Input/Output**
	U1C1_SCLKOUT	O1	St/B	**USIC1 Channel 1 Shift Clock Output**
	U1C0_SELO2	O2	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	CCU61_COUT62	O3	St/B	**CCU61 Channel 2 Output**
	A5	OH	St/B	**External Bus Interface Address Line 5**
	U1C1_DX1A	I	St/B	**USIC1 Channel 1 Shift Clock Input**
	U1C0_DX1C	I	St/B	**USIC1 Channel 0 Shift Clock Input**
69	P10.4	O0 / I	St/B	**Bit 4 of Port 10, General Purpose Input/Output**
	U0C0_SELO3	O1	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CCU60_COUT61	O2	St/B	**CCU60 Channel 1 Output**
	AD4	OH / IH	St/B	**External Bus Interface Address/Data Line 4**
	U0C0_DX2B	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2B	I	St/B	**USIC0 Channel 1 Shift Control Input**
	ESR1_9	I	St/B	**ESR1 Trigger Input 9**

2.2 Identification Registers

The identification registers describe the current version of the XE164xN and of its modules.

Table 6 XE164xN Identification Registers

Short Name	Value	Address	Notes
SCU_IDMANUF	1820_H	$00'F07E_H$	
SCU_IDCHIP	3001_H	$00'F07C_H$	marking EES-AA or ES-AA
	3002_H	$00'F07C_H$	marking AA, AB
SCU_IDMEM	$304F_H$	$00'F07A_H$	
SCU_IDPROG	1313_H	$00'F078_H$	
JTAG_ID	$0018'B083_H$	---	marking EES-AA or ES-AA
	$1018'B083_H$	---	marking AA, AB

3.1 Memory Subsystem and Organization

The memory space of the XE164xN is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 7 XE164xN Memory Map 1)

Address Area	Start Loc.	End Loc.	Area Size2)	Notes
IMB register space	FF’FF00$_H$	FF’FFFF$_H$	256 Bytes	
Reserved	F0’0000$_H$	FF’FEFF$_H$	< 1 Mbyte	Minus IMB registers
Reserved for EPSRAM	E8’4000$_H$	EF’FFFF$_H$	496 Kbytes	Mirrors EPSRAM
Emulated PSRAM	E8’0000$_H$	E8’3FFF$_H$	up to 16 Kbytes	With Flash timing
Reserved for PSRAM	E0’4000$_H$	E7’FFFF$_H$	496 Kbytes	Mirrors PSRAM
PSRAM	E0’0000$_H$	E0’3FFF$_H$	up to 16 Kbytes	Program SRAM
Reserved for Flash	C5’0000$_H$	DF’FFFF$_H$	1,728 Kbytes	
Flash 1	C4’0000$_H$	C4’FFFF$_H$	64 Kbytes	
Flash 0	C0’0000$_H$	C3’FFFF$_H$	256 Kbytes3)	Minus res. seg.
External memory area	40’0000$_H$	BF’FFFF$_H$	8 Mbytes	
External IO area4)	21’0000$_H$	3F’FFFF$_H$	1,984 Kbytes	
Reserved	20’BC00$_H$	20’FFFF$_H$	17 Kbytes	
USIC0–2 alternate regs.	20’B000$_H$	20’BBFF$_H$	3 Kbytes	Accessed via EBC
MultiCAN alternate regs.	20’8000$_H$	20’AFFF$_H$	12 Kbytes	Accessed via EBC
Reserved	20’5800$_H$	20’7FFF$_H$	10 Kbytes	
USIC0–2 registers	20’4000$_H$	20’57FF$_H$	6 Kbytes	Accessed via EBC
Reserved	20’6800$_H$	20’7FFF$_H$	6 Kbytes	
MultiCAN registers	20’0000$_H$	20’3FFF$_H$	16 Kbytes	Accessed via EBC
External memory area	01’0000$_H$	1F’FFFF$_H$	1984 Kbytes	
SFR area	00’FE00$_H$	00’FFFF$_H$	0.5 Kbytes	
Dualport RAM (DPRAM)	00’F600$_H$	00’FDFF$_H$	2 Kbytes	
Reserved for DPRAM	00’F200$_H$	00’F5FF$_H$	1 Kbytes	
ESFR area	00’F000$_H$	00’F1FF$_H$	0.5 Kbytes	
XSFR area	00’E000$_H$	00’EFFF$_H$	4 Kbytes	
Data SRAM (DSRAM)	00’A000$_H$	00’DFFF$_H$	16 Kbytes	

3.2 External Bus Controller

All external memory access operations are performed by a special on-chip External Bus Controller (EBC). The EBC also controls access to resources connected to the on-chip LXBus (MultiCAN and the USIC modules). The LXBus is an internal representation of the external bus that allows access to integrated peripherals and modules in the same way as to external components.

The EBC can be programmed either to Single Chip Mode, when no external memory is required, or to an external bus mode with the following selections[1]:

- Address Bus Width with a range of 0 … 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

The bus interface uses Port 10 and Port 2 for addresses and data. In the demultiplexed bus modes, the lower addresses are output separately on Port 0 and Port 1. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines shall be assigned to Port 2.

External $\overline{\text{CS}}$ signals (address windows plus default) can be generated and output on Port 4 in order to save external glue logic. External modules can be directly connected to the common address/data bus and their individual select lines.

Important timing characteristics of the external bus interface are programmable (with registers TCONCSx/FCONCSx) to allow the user to adapt it to a wide range of different types of memories and external peripherals.
Access to very slow memories or modules with varying access times is supported by a special ‘Ready’ function. The active level of the control input signal is selectable.

In addition, up to four independent address windows may be defined (using registers ADDRSELx) to control access to resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these four address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is based on the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

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[1] Bus modes are switched dynamically if several address windows with different mode settings are used.

3.3 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.

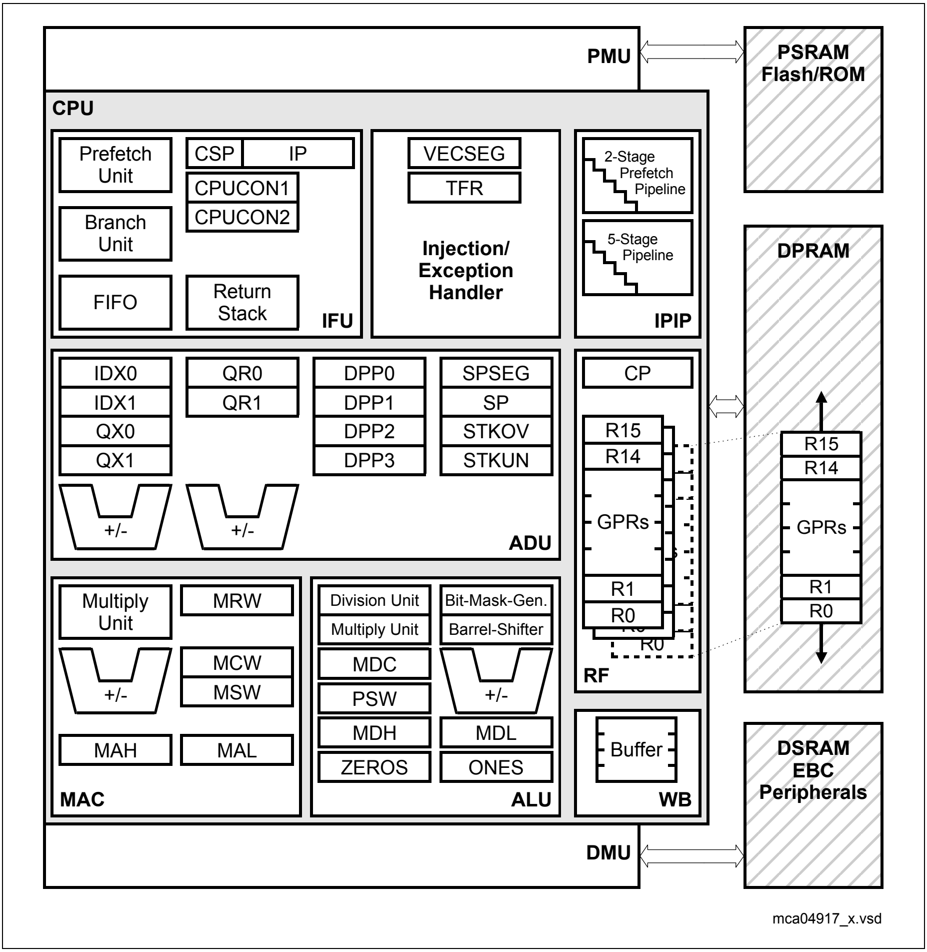

Figure 5 CPU Block Diagram

3.6 Interrupt System

The architecture of the XE164xN supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Using a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed. With the PEC just one cycle is 'stolen' from the current CPU activity to perform the PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XE164xN has eight PEC channels, each with fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11[1] CPU clocks, the XE164xN can react quickly to the occurrence of non-deterministic events.

Interrupt Nodes and Source Selection

The interrupt system provides 96 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

Trap Processing

The XE164xN provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called 'Hardware Traps'. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

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[1] Depending if the jump cache is used or not.

Table 8 Compare Modes (cont'd)

Compare Modes	Function
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the compare mode selected.

MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Independent CAN nodes
- Set of independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.15 System Timer

The System Timer consists of a programmable prescaler and two concatenated timers (10 bits and 6 bits). Both timers can generate interrupt requests. The clock source can be selected and the timers can also run during power reduction modes.

Therefore, the System Timer enables the software to maintain the current time for scheduling functions or for the implementation of a clock.

3.16 Watchdog Timer

The Watchdog Timer is one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after an application reset of the chip. It can be disabled and enabled at any time by executing the instructions DISWDT and ENWDT respectively. The software has to service the Watchdog Timer before it overflows. If this is not the case because of a hardware or software failure, the Watchdog Timer overflows, generating a prewarning interrupt and then a reset request.

The Watchdog Timer is a 16-bit timer clocked with the system clock divided by 16,384 or 256. The Watchdog Timer register is set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the Watchdog Timer is reloaded and the prescaler is cleared.

Time intervals between 3.2 μs and 13.4 s can be monitored (@ 80 MHz).

The default Watchdog Timer interval after power-up is 6.5 ms (@ 10 MHz).

Table 10 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

1) The Enter Power Down Mode instruction is not used in the XE164xN, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

Note: A fraction of the leakage current flows through domain DMP_A (pin V_{DDPA}). This current can be calculated as 7,000 × $e^{-\alpha}$, with α = 5000 / (273 + 1.3 × T_J). For T_J = 150°C, this results in a current of 160 μA.

Leakage Power Consumption Calculation

The leakage power consumption can be calculated according to the following formula:

$I_{LK1} = 530{,}000 \times e^{-\alpha}$ with $\alpha = 5000 / (273 + B \times T_J)$

Parameter B must be replaced by

- 1.0 for typical values
- 1.3 for maximum values

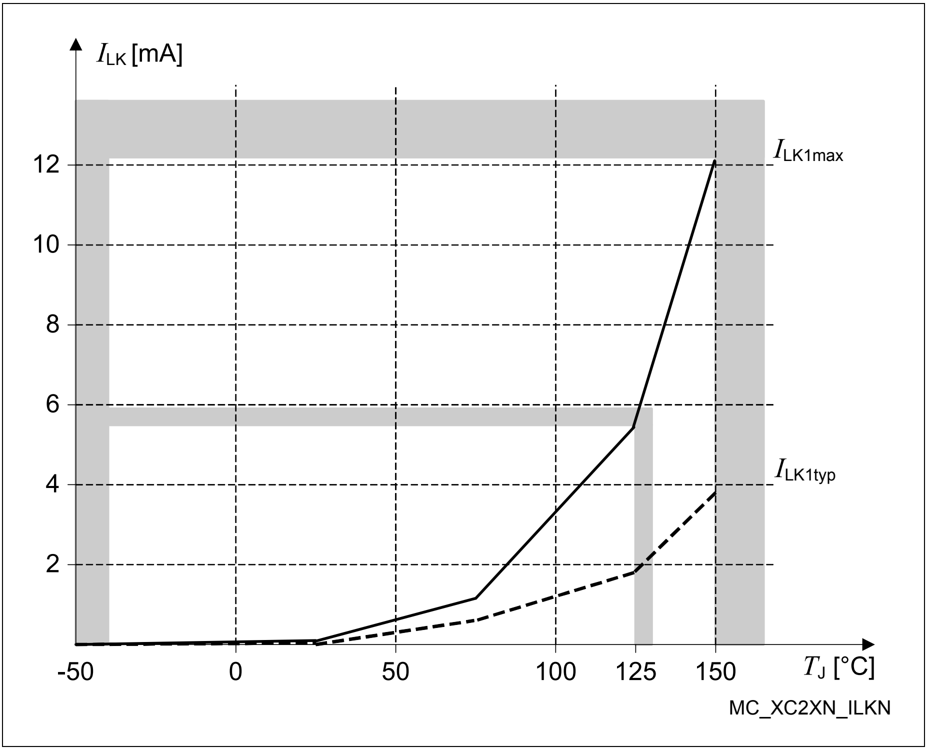


Figure 15 **Leakage Supply Current as a Function of Temperature**

4) The broken wire detection delay against V_{AREF} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 10 µs. This function is influenced by leakage current, in particular at high temperature. Result above 80% (332_H)

5) TUE is tested at $V_{AREF} = V_{DDPA} = 5.0$ V, $V_{AGND} = 0$ V. It is verified by design for all other voltages within the defined voltage range. The specified TUE is valid only if the absolute sum of input overload currents on analog port pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.

6) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

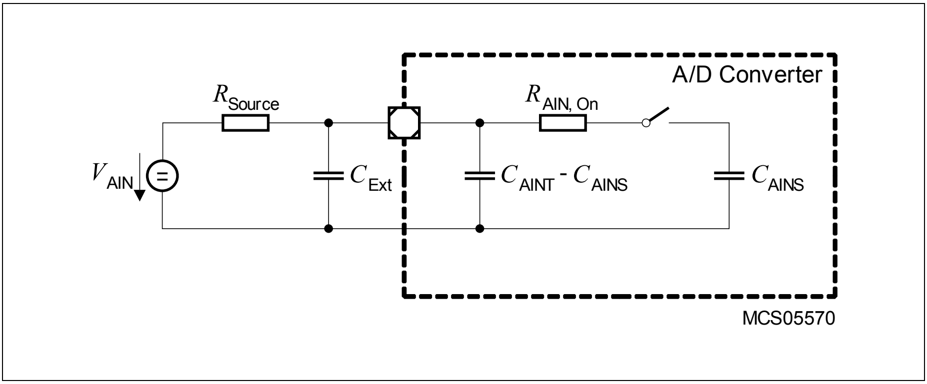


Figure 16 Equivalent Circuitry for Analog Inputs

4.6 Flash Memory Parameters

The XE164xN is delivered with all Flash sectors erased and with no protection installed.

The data retention time of the XE164xN's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 24 Flash Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Parallel Flash module program/erase limit depending on Flash read activity	N_{PP} SR	–	–	2[1]		$N_{\mathrm{FL\_RD}} \leq 1$
		–	–	1[2]		$N_{\mathrm{FL\_RD}} > 1$
Flash erase endurance for security pages	N_{SEC} SR	10	–	–	cycles	$t_{\mathrm{RET}} \geq 20$ years
Flash wait states[3]	N_{WSFLASH} SR	1	–	–		$f_{\mathrm{SYS}} \leq 8$ MHz
		2	–	–		$f_{\mathrm{SYS}} \leq 13$ MHz
		3	–	–		$f_{\mathrm{SYS}} \leq 17$ MHz
		4	–	–		$f_{\mathrm{SYS}} > 17$ MHz
Erase time per sector/page	t_{ER} CC	–	7[4]	8.0	ms	
Programming time per page	t_{PR} CC	–	3[4]	3.5	ms	
Data retention time	t_{RET} CC	20	–	–	years	$N_{\mathrm{ER}} \leq 1{,}000$ cycles
Drain disturb limit	N_{DD} SR	32	–	–	cycles	
Number of erase cycles	N_{ER} SR	–	–	15.000	cycles	$t_{\mathrm{RET}} \geq 5$ years; Valid for Flash module 1 (up to 64 kbytes)
		–	–	1.000	cycles	$t_{\mathrm{RET}} \geq 20$ years

---

[1] The unused Flash module(s) can be erased/programmed while code is executed and/or data is read from only one Flash module or from PSRAM. The Flash module that delivers code/data can, of course, not be erased/programmed.

2) Flash module 1 can be erased/programmed while code is executed and/or data is read from Flash module 0.

3) Value of IMB_IMBCTRL.WSFLASH.

4) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticably only at extremely low system clock frequencies.

Access to the XE164xN Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

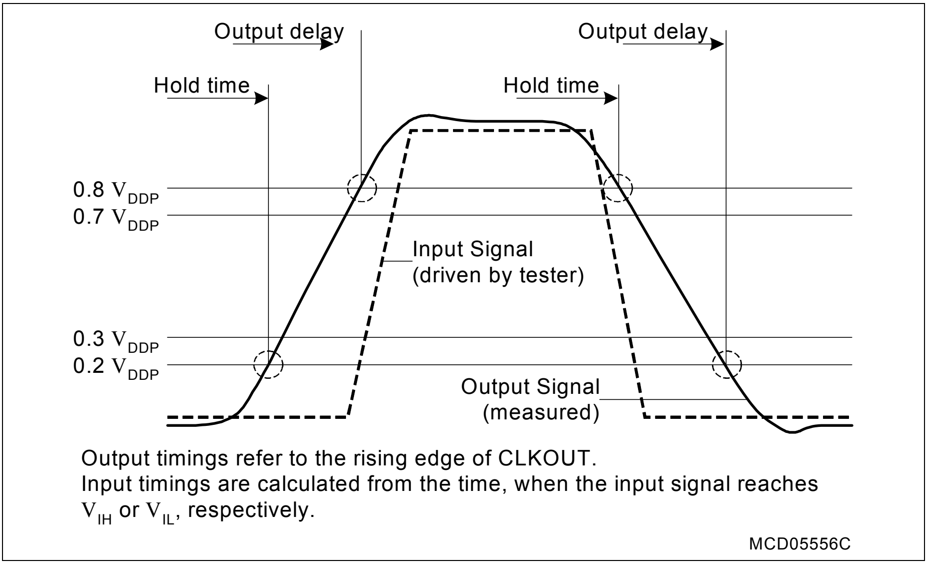
Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

4.7 AC Parameters

These parameters describe the dynamic behavior of the XE164xN.

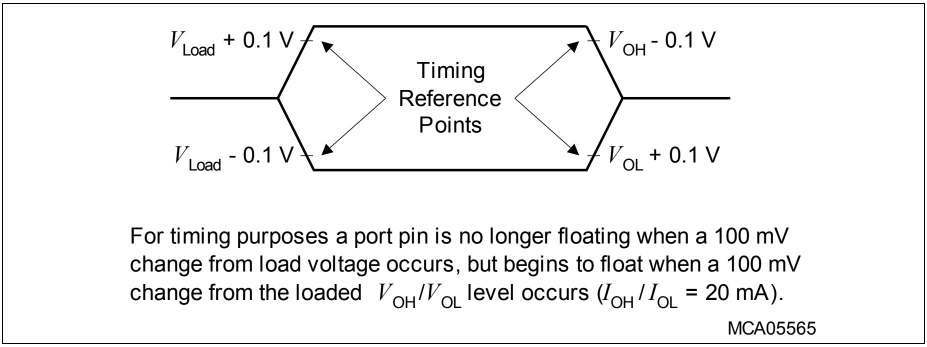
4.7.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).



Output timings refer to the rising edge of CLKOUT.
Input timings are calculated from the time, when the input signal reaches V_{IH} or V_{IL}, respectively.

Figure 17 Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

Figure 18 Floating Waveforms

Table 25 System PLL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCO output frequency	f_{VCO} CC	50	–	110	MHz	*VCOSEL*= 00b; *VCOmode*= controlled
		10	–	40	MHz	*VCOSEL*= 00b; *VCOmode*= free running
		100	–	160	MHz	*VCOSEL*= 01b; *VCOmode*= controlled
		20	–	80	MHz	*VCOSEL*= 01b; *VCOmode*= free running

4.7.2.2 Wakeup Clock

When wakeup operation is selected (SYSCON0.CLKSEL = 00_B), the system clock is derived from the low-frequency wakeup clock source:

$f_{\mathrm{SYS}} = f_{\mathrm{WU}}$.

In this mode, a basic functionality can be maintained without requiring an external clock source and while minimizing the power consumption.

4.7.2.3 Selecting and Changing the Operating Frequency

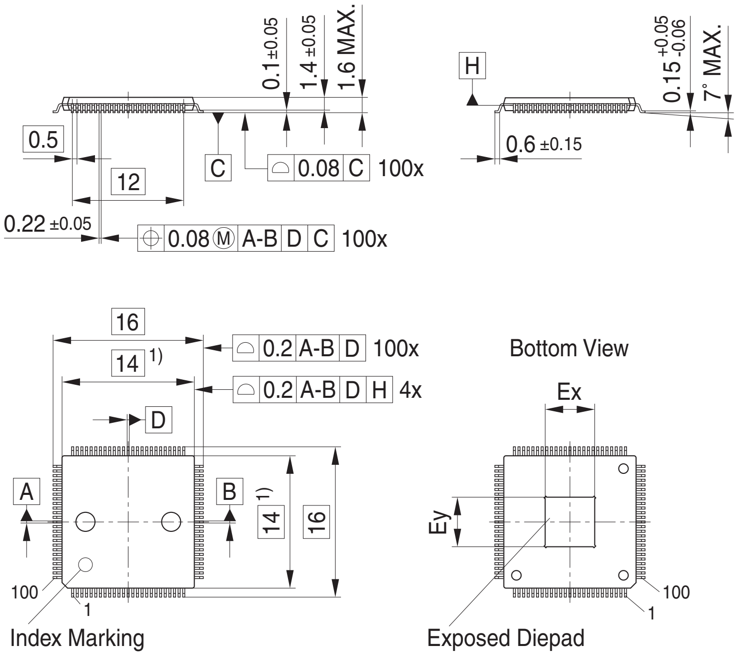
When selecting a clock source and the clock generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock (f_{SYS}) during operation in order to optimize system performance and power consumption. Changing the operating frequency also changes the switching currents, which influences the power supply.

To ensure proper operation of the on-chip EVRs while they generate the core voltage, the operating frequency shall only be changed in certain steps. This prevents overshoots and undershoots of the supply voltage.

To avoid the indicated problems, recommended sequences are provided which ensure the intended operation of the clock system interacting with the power system.
Please refer to the Programmer's Guide.

Package Outlines



1) Does not include plastic or metal protrusion of 0.25 max. per side

Figure 32 **PG-LQFP-100-8** (Plastic Green Thin Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**