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Details

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe164fn40f80laafxuma1

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XE164xN Data Sheet

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V1.1, 2009-07

V1.0, 2009-03 Preliminary

Page	Subjects (major changes since last revision)
36	Added AB step marking.
87	Errata SWD_X.P002 implemented: V_{SWD} tolerance boundaries for 5.5 V are changed.
89	Clarified "Coding of bit fields LEVxV" descriptions. Matched with Operating Conditions: marked some coding values "out of valid operation range".
90	Errata FLASH_X.P001 implemented: Test Condition for Flash parameter N_{ER} corrected

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Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
39	P2.0	O0 / I	St/B	Bit 0 of Port 2, General Purpose Input/Output
	AD13	OH / IH	St/B	External Bus Interface Address/Data Line 13
	RxDC0C	I	St/B	CAN Node 0 Receive Data Input
	T5INB	I	St/B	GPT12E Timer T5 Count/Gate Input
40	P2.1	O0 / I	St/B	Bit 1 of Port 2, General Purpose Input/Output
	TxDC0	O1	St/B	CAN Node 0 Transmit Data Output
	AD14	OH / IH	St/B	External Bus Interface Address/Data Line 14
	T5EUDB	I	St/B	GPT12E Timer T5 External Up/Down Control Input
	ESR1_5	I	St/B	ESR1 Trigger Input 5
41	P2.2	O0 / I	St/B	Bit 2 of Port 2, General Purpose Input/Output
	TxDC1	O1	St/B	CAN Node 1 Transmit Data Output
	AD15	OH / IH	St/B	External Bus Interface Address/Data Line 15
	ESR2_5	I	St/B	ESR2 Trigger Input 5
42	P4.0	O0 / I	St/B	Bit 0 of Port 4, General Purpose Input/Output
	CC2_CC24	O3 / I	St/B	CAPCOM2 CC24IO Capture Inp./ Compare Out.
	CS0	OH	St/B	External Bus Interface Chip Select 0 Output
43	P2.3	O0 / I	St/B	Bit 3 of Port 2, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	CC2_CC16	O3 / I	St/B	CAPCOM2 CC16IO Capture Inp./ Compare Out.
	A16	OH	St/B	External Bus Interface Address Line 16
	ESR2_0	I	St/B	ESR2 Trigger Input 0
	U0C0_DX0E	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX0D	I	St/B	USIC0 Channel 1 Shift Data Input
	RxDC0A	I	St/B	CAN Node 0 Receive Data Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
87	P1.3	O0 / I	St/B	Bit 3 of Port 1, General Purpose Input/Output
	U1C0_SELO 7	O2	St/B	USIC1 Channel 0 Select/Control 7 Output
	U2C0_SELO 4	O3	St/B	USIC2 Channel 0 Select/Control 4 Output
	A11	OH	St/B	External Bus Interface Address Line 11
	ESR2_4	I	St/B	ESR2 Trigger Input 4
89	P10.14	O0 / I	St/B	Bit 14 of Port 10, General Purpose Input/Output
	U1C0_SELO 1	O1	St/B	USIC1 Channel 0 Select/Control 1 Output
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	$\overline{\text{RD}}$	OH	St/B	External Bus Interface Read Strobe Output
	ESR2_2	I	St/B	ESR2 Trigger Input 2
	U0C1_DX0C	I	St/B	USIC0 Channel 1 Shift Data Input
90	P1.4	O0 / I	St/B	Bit 4 of Port 1, General Purpose Input/Output
	U1C1_SELO 4	O2	St/B	USIC1 Channel 1 Select/Control 4 Output
	U2C0_SELO 5	O3	St/B	USIC2 Channel 0 Select/Control 5 Output
	A12	OH	St/B	External Bus Interface Address Line 12
	U2C0_DX2B	I	St/B	USIC2 Channel 0 Shift Control Input
91	P10.15	O0 / I	St/B	Bit 15 of Port 10, General Purpose Input/Output
	U1C0_SELO 2	O1	St/B	USIC1 Channel 0 Select/Control 2 Output
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U1C0_DOUT	O3	St/B	USIC1 Channel 0 Shift Data Output
	ALE	OH	St/B	External Bus Interf. Addr. Latch Enable Output
	U0C1_DX1C	I	St/B	USIC0 Channel 1 Shift Clock Input

Functional Description

Table 7 XE164xN Memory Map (cont'd)¹⁾

Address Area	Start Loc.	End Loc.	Area Size ²⁾	Notes
Reserved for DSRAM	00'8000 _H	00'9FFF _H	8 Kbytes	
External memory area	00'0000 _H	00'7FFF _H	32 Kbytes	

1) Accesses to the shaded areas are reserved. In devices with external bus interface these accesses generate external bus accesses.

2) The areas marked with "<" are slightly smaller than indicated, see column "Notes".

3) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

4) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

This common memory space consists of 16 Mbytes organized as 256 segments of 64 Kbytes; each segment contains four data pages of 16 Kbytes. The entire memory space can be accessed byte-wise or word-wise. Portions of the on-chip DPRAM and the register spaces (ESFR/SFR) additionally are directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls access to the program memories such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls access to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected to the high-speed system bus so that they can exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources. These include peripherals on the LXBus such as USIC or MultiCAN. The system bus allows concurrent two-way communication for maximum transfer performance.

Up to 16 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is optimized for code fetches. A section of the PSRAM with programmable size can be write-protected.

Note: The actual size of the PSRAM depends on the quoted device type.

Functional Description

Up to 16 Kbytes of on-chip Data SRAM (DSRAM) are used for storage of general user data. The DSRAM is accessed via a separate interface and is optimized for data access.

Note: The actual size of the DSRAM depends on the quoted device type.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, ..., RL7, RH7) General Purpose Registers (GPRs).

The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

8 Kbytes of on-chip Stand-By SRAM (SBRAM) provide storage for system-relevant user data that must be preserved while the major part of the device is powered down. The SBRAM is accessed via a specific interface and is powered in domain M.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XE166 Family. In order to ensure upward compatibility they should either not be accessed or written with zeros.

In order to meet the requirements of designs where more memory is required than is available on chip, up to 12 Mbytes (approximately, see [Table 7](#)) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

The on-chip Flash memory stores code, constant data, and control data. The 320 Kbytes of on-chip Flash memory consist of 1 module of 64 Kbytes (preferably for data storage) and 1 module of 256 Kbytes. Each module is organized in 4-Kbyte sectors. The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

Note: The actual size of the Flash memory depends on the chosen device type.

Each sector can be separately write protected¹⁾, erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.

For Flash parameters, please see [Section 4.6](#).

1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

3.3 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.

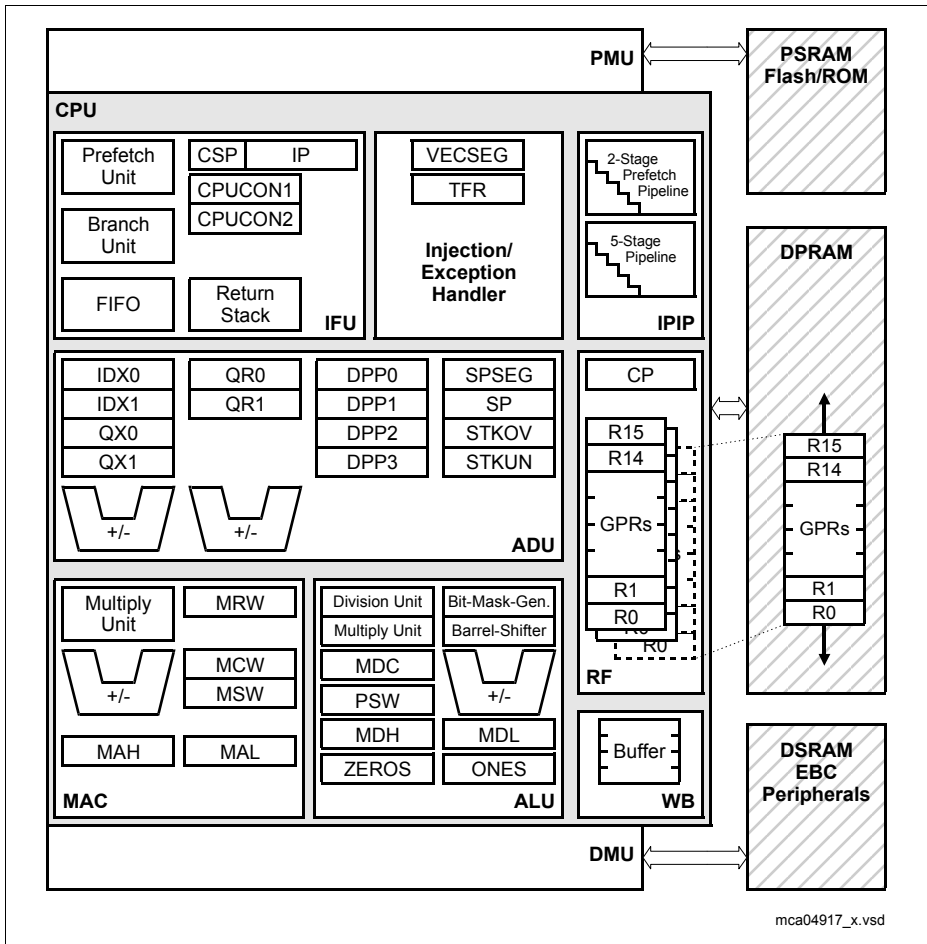


Figure 5 CPU Block Diagram

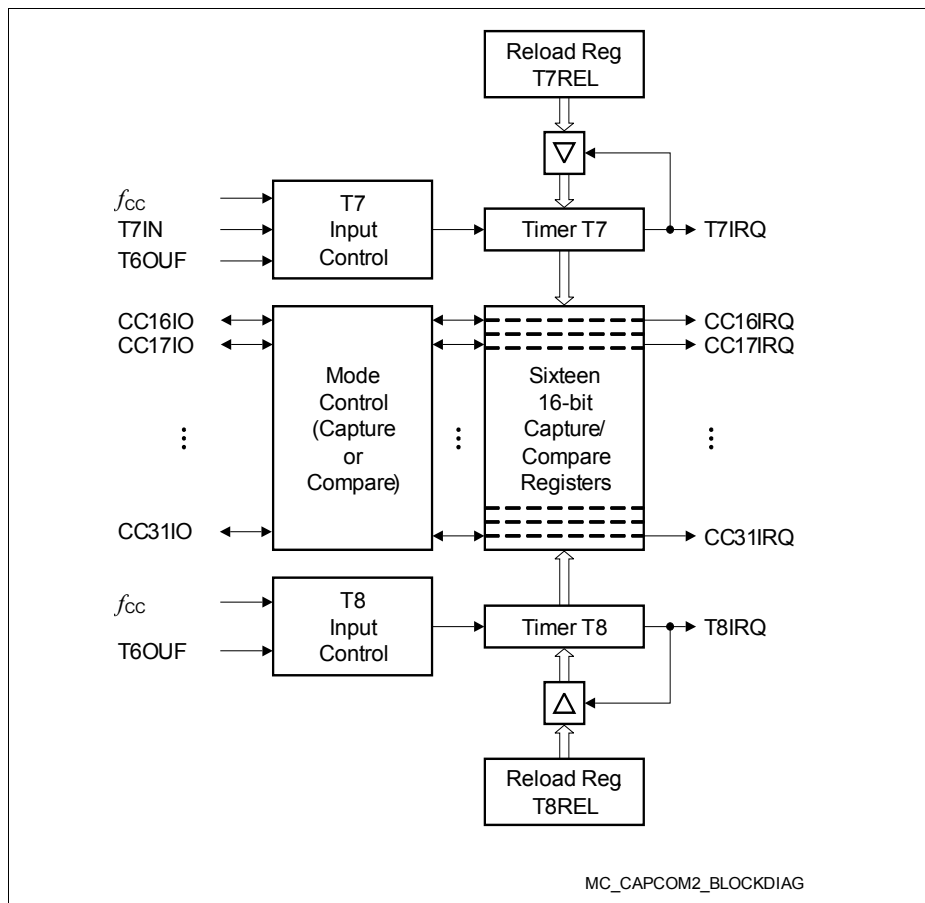


Figure 6 CAPCOM Unit Block Diagram

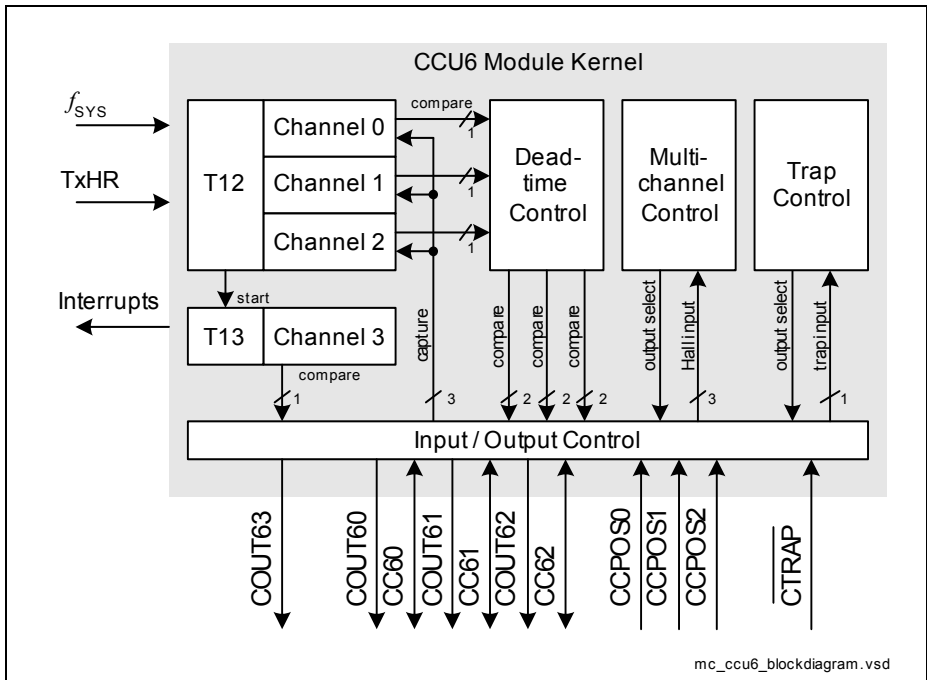


Figure 7 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
 - module capability: maximum baud rate = $f_{\text{SYS}} / 4$
 - data frame length programmable from 1 to 63 bits
 - MSB or LSB first
- **LIN** Support (Local Interconnect Network)
 - module capability: maximum baud rate = $f_{\text{SYS}} / 16$
 - checksum generation under software control
 - baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI** (synchronous serial channel with or without data buffer)
 - module capability: maximum baud rate = $f_{\text{SYS}} / 2$, limited by loop delay
 - number of data bits programmable from 1 to 63, more with explicit stop condition
 - MSB or LSB first
 - optional control of slave select signals
- **IIC** (Inter-IC Bus)
 - supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
 - module capability: maximum baud rate = $f_{\text{SYS}} / 2$

Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum achievable baud rate can be limited. Please note that there may be additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).

3.14 MultiCAN Module

The MultiCAN module contains independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames using a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

Note: The number of CAN nodes and message objects depends on the selected device type.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

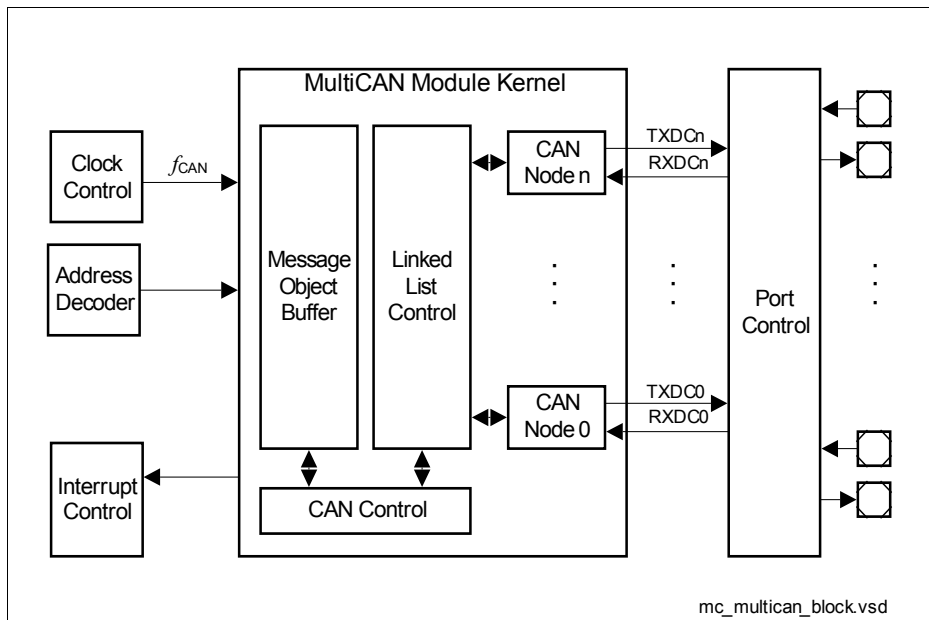


Figure 12 Block Diagram of MultiCAN Module

3.18 Parallel Ports

The XE164xN provides up to 76 I/O lines which are organized into 7 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have alternate input or output functions associated with them. These alternate functions can be programmed to be assigned to various port pins to support the best utilization for a given application. For this reason, certain functions appear several times in [Table 9](#).

All port lines that are not used for alternate functions may be used as general purpose I/O lines.

Table 9 Summary of the XE164xN's Ports

Port	Width	I/O	Connected Modules
P0	8	I/O	EBC (A7...A0), CCU6, USIC, CAN
P1	8	I/O	EBC (A15...A8), CCU6, USIC
P2	14	I/O	EBC (READY, $\overline{\text{BHE}}$, A23...A16, AD15...AD13, D15...D13), CAN, CC2, GPT12E, USIC, DAP/JTAG
P4	4	I/O	EBC ($\overline{\text{CS3}}$... $\overline{\text{CS0}}$), CC2, CAN, GPT12E, USIC
P5	11	I	Analog Inputs, CCU6, DAP/JTAG, GPT12E, CAN
P6	3	I/O	ADC, CAN, GPT12E
P7	5	I/O	CAN, GPT12E, SCU, DAP/JTAG, CCU6, ADC, USIC
P10	16	I/O	EBC (ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, AD12...AD0, D12...D0), CCU6, USIC, DAP/JTAG, CAN
P15	5	I	Analog Inputs, GPT12E

4.7.3 External Clock Input Parameters

These parameters specify the external clock generation for the XE164xN. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2.
- By supplying an **external clock signal**
 - This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain).

If connected to CLKIN1, the input signal must reach the defined input levels V_{IL} and V_{IH} . If connected to XTAL1, a minimum amplitude V_{AX1} (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

Note: The given clock timing parameters ($t_1 \dots t_4$) are only valid for an external clock input signal.

Note: Operating Conditions apply.

Table 26 External Clock Input Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Oscillator frequency	f_{OSC} SR	4	–	40	MHz	Input= Clock Signal
		4	–	16	MHz	Input= Crystal or Ceramic Resonator
XTAL1 input current absolute value	$ I_{IL} $ CC	–	–	20	μA	
Input clock high time	t_1 SR	6	–	–	ns	
Input clock low time	t_2 SR	6	–	–	ns	
Input clock rise time	t_3 SR	–	8	8	ns	
Input clock fall time	t_4 SR	–	8	8	ns	
Input voltage amplitude on XTAL1 ¹⁾	V_{AX1} SR	0.3 x V_{DDIM}	–	–	V	$f_{OSC} \geq 4$ MHz; $f_{OSC} < 16$ MHz
		0.4 x V_{DDIM}	–	–	V	$f_{OSC} \geq 16$ MHz; $f_{OSC} < 25$ MHz
		0.5 x V_{DDIM}	–	–	V	$f_{OSC} \geq 25$ MHz; $f_{OSC} \leq 40$ MHz
Input voltage range limits for signal on XTAL1	V_{IX1} SR	-1.7 + V_{DDIM}	–	1.7	V	²⁾

Table 28 Standard Pad Parameters for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value) ¹⁾	I_{Omax} CC	–	–	2.5	mA	Driver_Strength = Medium
		–	–	10	mA	Driver_Strength = Strong
		–	–	0.5	mA	Driver_Strength = Weak
Nominal output driver current (absolute value)	I_{Onom} CC	–	–	1.0	mA	Driver_Strength = Medium
		–	–	2.5	mA	Driver_Strength = Strong
		–	–	0.1	mA	Driver_Strength = Weak

Electrical Parameters
Table 31 External Bus Timing for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Address output valid delay for AD15 ... AD0 (MUX mode)	t_{13} CC	–	8	15	ns	
Output valid delay for \overline{CS}	t_{14} CC	–	7	13	ns	
Data output valid delay for AD15 ... AD0 (write data, MUX mode)	t_{15} CC	–	8	15	ns	
Data output valid delay for D15 ... D0 (write data, DEMUX mode)	t_{16} CC	–	8	15	ns	
Output hold time for \overline{RD} , \overline{WR} (L/H)	t_{20} CC	-2	6	8	ns	
Output hold time for \overline{BHE} , ALE	t_{21} CC	-2	6	10	ns	
Address output hold time for AD15 ... AD0	t_{23} CC	-3	6	8	ns	
Output hold time for \overline{CS}	t_{24} CC	-3	6	11	ns	
Data output hold time for D15 ... D0 and AD15 ... AD0	t_{25} CC	-3	6	8	ns	
Input setup time for READY, D15 ... D0, AD15 ... AD0	t_{30} SR	25	15	–	ns	
Input hold time READY, D15 ... D0, AD15 ... AD0 ¹⁾	t_{31} SR	0	-7	–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of \overline{RD} . Address changes before the end of \overline{RD} have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of \overline{RD} .

Table 32 is valid under the following conditions: $C_L = 20$ pF; voltage_range= lower ; voltage_range= lower

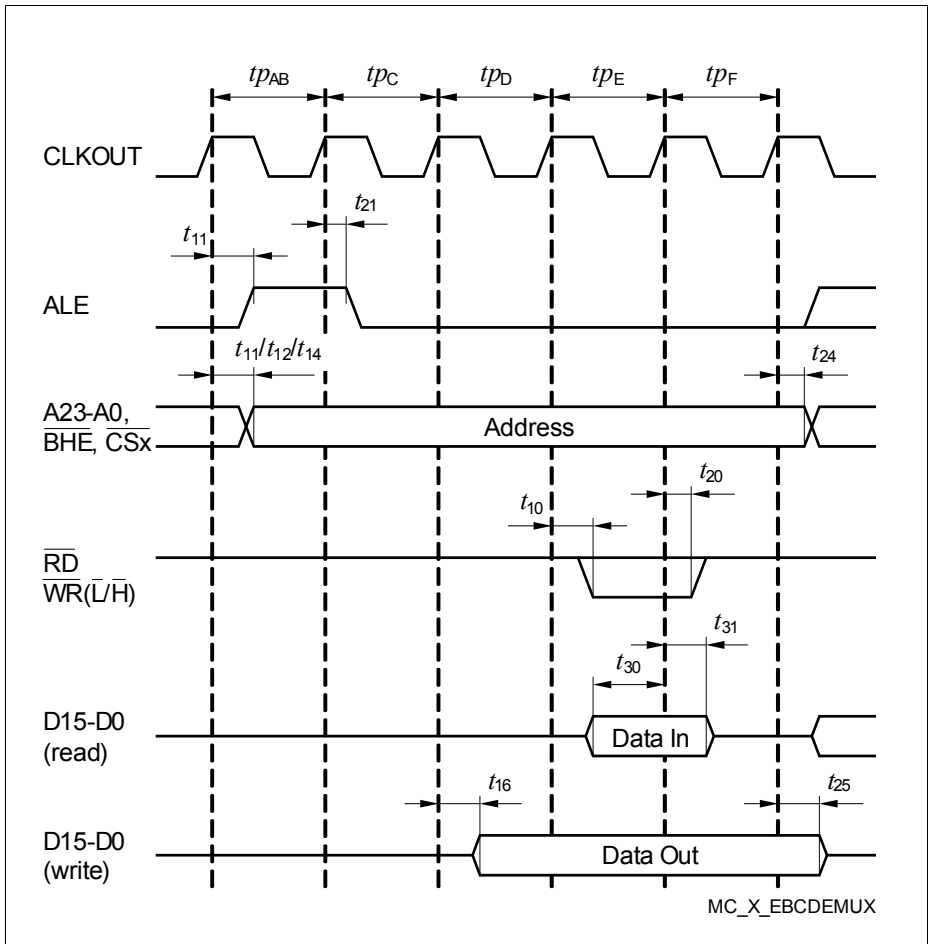


Figure 24 Demultiplexed Bus Cycle

4.7.5.1 Bus Cycle Control with the READY Input

The duration of an external bus cycle can be controlled by the external circuit using the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

An asynchronous READY signal puts no timing constraints on the input signal but incurs a minimum of one waitstate due to the additional synchronization stage. The minimum

Electrical Parameters

Table 40 JTAG Interface Timing for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TDI/TMS hold after TCK rising edge	t_7 SR	6	—	—	ns	
TDO valid from TCK falling edge (propagation delay) ¹⁾	t_8 CC	—	32	36	ns	
TDO high impedance to valid output from TCK falling edge ²⁾¹⁾	t_9 CC	—	32	36	ns	
TDO valid output to high impedance from TCK falling edge ¹⁾	t_{10} CC	—	32	36	ns	
TDO hold after TCK falling edge ¹⁾	t_{18} CC	5	—	—	ns	

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

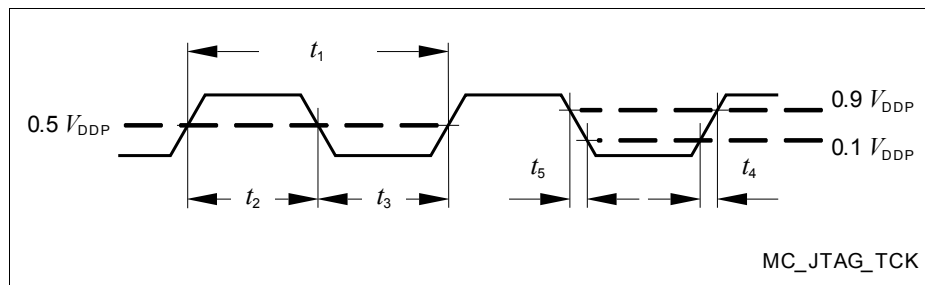


Figure 30 Test Clock Timing (TCK)

5 Package and Reliability

The XE166 Family devices use the package type PG-LQFP (Plastic Green - Low Profile Quad Flat Package). The following specifications must be regarded to ensure proper integration of the XE164xN in its target environment.

5.1 Packaging

These parameters specify the packaging rather than the silicon.

Table 41 Package Parameters (PG-LQFP-100-8)

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Exposed Pad Dimension	$E_x \times E_y$	–	5.2×5.2	mm	–
Power Dissipation	P_{DISS}	–	0.8	W	–
Thermal resistance Junction-Ambient	$R_{\Theta JA}$	–	54	K/W	No thermal via ¹⁾
			49	K/W	4-layer, no pad ²⁾
			27	K/W	4-layer, pad ³⁾

1) Device mounted on a 4-layer board without thermal vias; exposed pad not soldered.

2) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad not soldered.

3) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad soldered to the board.

Note: To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground, independent of the thermal requirements.

Board layout examples are given in an application note.

Package Compatibility Considerations

The XE164xN is a member of the XE166 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Pad (if present) may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

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