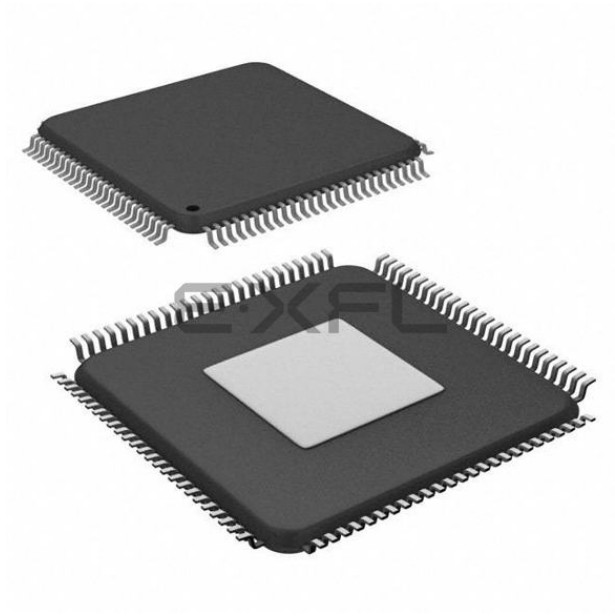
Infineon Technologies - XE164FN40F80LRABKXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe164fn40f80lrabkxuma1

1.2 Definition of Feature Variants

The XE164xN types are offered with several Flash memory sizes. **Table 2** and **Table 3** describe the location of the available Flash memory.

Table 2 Continuous Flash Memory Ranges

Total Flash Size	1st Range[1)]	2nd Range	3rd Range
320 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C4'FFFF_H$	n.a.
192 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C1'FFFF_H$	$C4'0000_H$ … $C4'FFFF_H$
128 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C4'0000_H$ … $C4'FFFF_H$	n.a.

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

Table 3 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0[1)]	Flash 1
320	256	64
192	128	64
128	64	64

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XE164xN types are offered with different interface options. **Table 4** lists the available channels for each option.

Table 4 Interface Channel Association

Total Number	Available Channels / Message Objects
6 ADC0 channels	CH0, CH2 … CH5, CH8
11 ADC0 channels	CH0, CH2 … CH5, CH8 … CH11, CH13, CH15
5 ADC1 channels	CH0, CH2, CH4 … CH6
2 CAN nodes	CAN0, CAN1 64 message objects
4 serial channels	U0C0, U0C1, U1C0, U1C1
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
62	P10.2	O0 / I	St/B	**Bit 2 of Port 10, General Purpose Input/Output**
	U0C0_SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	CCU60_CC62	O2	St/B	**CCU60 Channel 2 Output**
	AD2	OH / IH	St/B	**External Bus Interface Address/Data Line 2**
	CCU60_CC62INA	I	St/B	**CCU60 Channel 2 Input**
	U0C0_DX1B	I	St/B	**USIC0 Channel 0 Shift Clock Input**
63	P0.4	O0 / I	St/B	**Bit 4 of Port 0, General Purpose Input/Output**
	U1C1_SELO0	O1	St/B	**USIC1 Channel 1 Select/Control 0 Output**
	U1C0_SELO1	O2	St/B	**USIC1 Channel 0 Select/Control 1 Output**
	CCU61_COUT61	O3	St/B	**CCU61 Channel 1 Output**
	A4	OH	St/B	**External Bus Interface Address Line 4**
	U1C1_DX2A	I	St/B	**USIC1 Channel 1 Shift Control Input**
	RxDC1B	I	St/B	**CAN Node 1 Receive Data Input**
	ESR2_8	I	St/B	**ESR2 Trigger Input 8**
65	P2.13	O0 / I	St/B	**Bit 13 of Port 2, General Purpose Input/Output**
	U2C1_SELO2	O1	St/B	**USIC2 Channel 1 Select/Control 2 Output**
66	P2.10	O0 / I	St/B	**Bit 10 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_SELO3	O2	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CC2_CC23	O3 / I	St/B	**CAPCOM2 CC23IO Capture Inp./ Compare Out.**
	A23	OH	St/B	**External Bus Interface Address Line 23**
	U0C1_DX0E	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CAPINA	I	St/B	**GPT12E Register CAPREL Capture Input**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
67	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COUT60	O2	St/B	**CCU60 Channel 0 Output**
	AD3	OH / IH	St/B	**External Bus Interface Address/Data Line 3**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
68	P0.5	O0 / I	St/B	**Bit 5 of Port 0, General Purpose Input/Output**
	U1C1_SCLKOUT	O1	St/B	**USIC1 Channel 1 Shift Clock Output**
	U1C0_SELO2	O2	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	CCU61_COUT62	O3	St/B	**CCU61 Channel 2 Output**
	A5	OH	St/B	**External Bus Interface Address Line 5**
	U1C1_DX1A	I	St/B	**USIC1 Channel 1 Shift Clock Input**
	U1C0_DX1C	I	St/B	**USIC1 Channel 0 Shift Clock Input**
69	P10.4	O0 / I	St/B	**Bit 4 of Port 10, General Purpose Input/Output**
	U0C0_SELO3	O1	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CCU60_COUT61	O2	St/B	**CCU60 Channel 1 Output**
	AD4	OH / IH	St/B	**External Bus Interface Address/Data Line 4**
	U0C0_DX2B	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2B	I	St/B	**USIC0 Channel 1 Shift Control Input**
	ESR1_9	I	St/B	**ESR1 Trigger Input 9**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
84	P1.2	O0 / I	St/B	**Bit 2 of Port 1, General Purpose Input/Output**
	U1C0_SELO 6	O2	St/B	**USIC1 Channel 0 Select/Control 6 Output**
	U2C1_SCLK OUT	O3	St/B	**USIC2 Channel 1 Shift Clock Output**
	A10	OH	St/B	**External Bus Interface Address Line 10**
	ESR1_4	I	St/B	**ESR1 Trigger Input 4**
	CCU61_T12 HRB	I	St/B	**External Run Control Input for T12 of CCU61**
	U2C1_DX0D	I	St/B	**USIC2 Channel 1 Shift Data Input**
	U2C1_DX1C	I	St/B	**USIC2 Channel 1 Shift Clock Input**
85	P10.12	O0 / I	St/B	**Bit 12 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TDO_B	OH / IH	St/B	**JTAG Test Data Output / DAP1 Input/Output** If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	AD12	OH / IH	St/B	**External Bus Interface Address/Data Line 12**
	U1C0_DX0C	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX1E	I	St/B	**USIC1 Channel 0 Shift Clock Input**
86	P10.13	O0 / I	St/B	**Bit 13 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	U1C0_SELO 3	O3	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	$\overline{WR}$/$\overline{WRL}$	OH	St/B	**External Bus Interface Write Strobe Output** Active for each external write access, when $\overline{WR}$, active for ext. writes to the low byte, when $\overline{WRL}$.
	U1C0_DX0D	I	St/B	**USIC1 Channel 0 Shift Data Input**

Up to 16 Kbytes of on-chip Data SRAM (DSRAM) are used for storage of general user data. The DSRAM is accessed via a separate interface and is optimized for data access.

Note: The actual size of the DSRAM depends on the quoted device type.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) provide storage for user-defined variables, for the system stack, and for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, …, RL7, RH7) General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

8 Kbytes of on-chip Stand-By SRAM (SBRAM) provide storage for system-relevant user data that must be preserved while the major part of the device is powered down. The SBRAM is accessed via a specific interface and is powered in domain M.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used to control and monitor functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XE166 Family. In order to ensure upward compatibility they should either not be accessed or written with zeros.

In order to meet the requirements of designs where more memory is required than is available on chip, up to 12 Mbytes (approximately, see **Table 7**) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

The on-chip Flash memory stores code, constant data, and control data. The 320 Kbytes of on-chip Flash memory consist of 1 module of 64 Kbytes (preferably for data storage) and 1 module of 256 Kbytes. Each module is organized in 4-Kbyte sectors. The uppermost 4-Kbyte sector of segment 0 (located in Flash module 0) is used internally to store operation control parameters and protection information.

Note: The actual size of the Flash memory depends on the chosen device type.

Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read access with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read access operations. Access to different Flash modules can be executed in parallel.
For Flash parameters, please see **Section 4.6**.

1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

3.6 Interrupt System

The architecture of the XE164xN supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Using a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed. With the PEC just one cycle is 'stolen' from the current CPU activity to perform the PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XE164xN has eight PEC channels, each with fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11[1)] CPU clocks, the XE164xN can react quickly to the occurrence of non-deterministic events.

Interrupt Nodes and Source Selection

The interrupt system provides 96 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

Trap Processing

The XE164xN provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called 'Hardware Traps'. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

1) Depending if the jump cache is used or not.

to a dedicated vector table location). The occurrence of a hardware trap is also indicated by a single bit in the trap flag register (TFR). Unless another higher-priority trap service is in progress, a hardware trap will interrupt any ongoing program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Depending on the package option up to 3 External Service Request (ESR) pins are provided. The ESR unit processes their input values and allows to implement user controlled trap functions (System Requests SR0 and SR1). In this way reset, wakeup and power control can be efficiently realized.

Software interrupts are supported by the 'TRAP' instruction in combination with an individual trap (interrupt) number. Alternatively to emulate an interrupt by software a program can trigger interrupt requests by writing the Interrupt Request (IR) bit of an interrupt control register.

3.7 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system built into the XE164xN provides a broad range of debug and emulation features. User software running on the XE164xN can be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface. This either consists of the 2-pin Device Access Port (DAP) or of the JTAG port conforming to IEEE-1149. The debug interface can be completed with an optional break interface.

The debugger controls the OCDS with a set of dedicated registers accessible via the debug interface (DAP or JTAG). In addition the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported, as is the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing of data can be obtained via the debug interface, or via the external bus interface for increased performance.

Tracing of program execution is supported by the XE166 Family emulation device. With this device the DAP can operate on clock rates of up to 20 MHz.

The DAP interface uses two interface signals, the JTAG interface uses four interface signals, to communicate with external circuitry. The debug interface can be amended with two optional break lines.

3.9 Capture/Compare Units CCU6x

The XE164xN types feature the CCU60, CCU61 unit(s).

CCU6 is a high-resolution capture and compare unit with application-specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features

- Three capture/compare channels, where each channel can be used either as a capture or as a compare channel.
- Supports generation of a three-phase PWM (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on a HW event (T12HR, for synchronization purposes)

Timer 13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period match and compare match
- Single-shot mode supported
- Automatic start on a HW event (T13HR, for synchronization purposes)

Additional Features

- Block commutation for brushless DC drives implemented
- Position detection via Hall sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC drives
- Output levels can be selected and adapted to the power stage

Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
  - module capability: maximum baud rate = f_{SYS} / 4
  - data frame length programmable from 1 to 63 bits
  - MSB or LSB first
- **LIN** Support (Local Interconnect Network)
  - module capability: maximum baud rate = f_{SYS} / 16
  - checksum generation under software control
  - baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI** (synchronous serial channel with or without data buffer)
  - module capability: maximum baud rate = f_{SYS} / 2, limited by loop delay
  - number of data bits programmable from 1 to 63, more with explicit stop condition
  - MSB or LSB first
  - optional control of slave select signals
- **IIC** (Inter-IC Bus)
  - supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
  - module capability: maximum baud rate = f_{SYS} / 2

Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum achievable baud rate can be limited. Please note that there may be additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).

3.17 Clock Generation

The Clock Generation Unit can generate the system clock signal f_{SYS} for the XE164xN from a number of external or internal clock sources:

- External clock signals with pad voltage or core voltage levels
- External crystal or resonator using the on-chip oscillator
- On-chip clock source for operation without crystal/resonator
- Wake-up clock (ultra-low-power) to further reduce power consumption

The programmable on-chip PLL with multiple prescalers generates a clock signal for maximum system performance from standard crystals, a clock input signal, or from the on-chip clock source. See also **Section 4.7.2**.

The Oscillator Watchdog (OWD) generates an interrupt if the crystal oscillator frequency falls below a certain limit or stops completely. In this case, the system can be supplied with an emergency clock to enable operation even after an external clock failure.

All available clock signals can be output on one of two selectable pins.

Table 10 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2 / 4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Unused instruction[1)]	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4

4.3.1 DC Parameters for Upper Voltage Area

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Note: Operating Conditions apply.

Table 15 is valid under the following conditions: $V_{DDP} \leq$ 5.5 V; V_{DDP}typ. 5 V; $V_{DDP} \geq$ 4.5 V

Table 15 DC Characteristics for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs). To be doubled for double bond pins.[1)]	C_{IO} CC	–	–	10	pF	not subject to production test
Input Hysteresis[2)]	HYS CC	0.11 x V_{DDP}	–	–	V	R_S= 0 Ohm
Absolute input leakage current on pins of analog ports[3)]	$\|I_{OZ1}\|$ CC	–	10	200	nA	$V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Absolute input leakage current for all other pins. To be doubled for double bond pins.[3)1)4)]	$\|I_{OZ2}\|$ CC	–	0.2	5	µA	$T_J \leq$ 110 °C; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
		–	0.2	15	µA	$T_J \leq$ 150 °C; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Pull Level Force Current[5)]	$\|I_{PLF}\|$ SR	250	–	–	µA	$V_{IN} \geq V_{IHmin}$*(pull down_enabled)*; $V_{IN} \leq V_{ILmax}$*(pull up_enabled)*
Pull Level Keep Current[6)]	$\|I_{PLK}\|$ SR	–	–	30	µA	$V_{IN} \geq V_{IHmin}$*(pull up_enabled)*; $V_{IN} \leq V_{ILmax}$*(pull down_enabled)*
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	–	0.3 x V_{DDP}	V	

Table 19 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Broken wire detection delay against VAGND[2]	t_{BWG} CC	–	–	50[3]		
Broken wire detection delay against VAREF[2]	t_{BWR} CC	–	–	50[4]		
Conversion time for 8-bit result[2]	t_{c8} CC	(11+STC) x t_{ADCI} + 2 x t_{SYS}	–	–		
Conversion time for 10-bit result[2]	t_{c10} CC	(13+STC) x t_{ADCI} + 2 x t_{SYS}	–	–		
Total Unadjusted Error	|TUE| CC	–	1	2	LSB	[5]
Wakeup time from analog powerdown, fast mode	t_{WAF} CC	–	–	4	µs	
Wakeup time from analog powerdown, slow mode	t_{WAS} CC	–	–	15	µs	
Analog reference ground	V_{AGND} SR	V_{SS} - 0.05	–	1.5	V	
Analog input voltage range	V_{AIN} SR	V_{AGND}	–	V_{AREF}	V	[6]
Analog reference voltage	V_{AREF} SR	V_{AGND} + 1.0	–	V_{DDPA} + 0.05	V	

1) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used: $C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 5 pF, R_{AINtyp} = 1.0 kOhm, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 10 pF, $R_{AREFtyp}$ = 1.0 kOhm.

2) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result. Values for the basic clock t_{ADCI} depend on programming.

3) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 µs. Result below 10% (66_H)

Sample time and conversion time of the XE164xN's A/D converters are programmable. The timing above can be calculated using **Table 20**.
The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

Table 20 A/D Converter Computation Table

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}	INPCRx.7-0 (STC)	Sample Time[1] t_S
000000_B	f_{SYS}	00_H	$t_{ADCI} \times 2$
000001_B	f_{SYS} / 2	01_H	$t_{ADCI} \times 3$
000010_B	f_{SYS} / 3	02_H	$t_{ADCI} \times 4$
:	f_{SYS} / (DIVA+1)	:	$t_{ADCI} \times$ (STC+2)
111110_B	f_{SYS} / 63	FE_H	$t_{ADCI} \times 256$
111111_B	f_{SYS} / 64	FF_H	$t_{ADCI} \times 257$

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

Converter Timing Example A:

Assumptions: f_{SYS} = 80 MHz (i.e. t_{SYS} = 12.5 ns), DIVA = 03_H, STC = 00_H
Analog clock f_{ADCI} = f_{SYS} / 4 = 20 MHz, i.e. t_{ADCI} = 50 ns
Sample time t_S = $t_{ADCI} \times 2$ = 100 ns

Conversion 10-bit:

t_{C10} = $13 \times t_{ADCI} + 2 \times t_{SYS}$ = 13×50 ns + 2×12.5 ns = 0.675 µs

Conversion 8-bit:

t_{C8} = $11 \times t_{ADCI} + 2 \times t_{SYS}$ = 11×50 ns + 2×12.5 ns = 0.575 µs

Converter Timing Example B:

Assumptions: f_{SYS} = 40 MHz (i.e. t_{SYS} = 25 ns), DIVA = 02_H, STC = 03_H
Analog clock f_{ADCI} = f_{SYS} / 3 = 13.3 MHz, i.e. t_{ADCI} = 75 ns
Sample time t_S = $t_{ADCI} \times 5$ = 375 ns

Conversion 10-bit:

t_{C10} = $16 \times t_{ADCI} + 2 \times t_{SYS}$ = 16×75 ns + 2×25 ns = 1.25 µs

Conversion 8-bit:

t_{C8} = $14 \times t_{ADCI} + 2 \times t_{SYS}$ = 14×75 ns + 2×25 ns = 1.10 µs

Coding of bit fields LEVxV in SWD Configuration Registers

After power-on the supply watch dog is preconfigured to operate in the lower voltage range.

Table 22 Coding of bit fields LEVxV in Register SWDCON0

Code	Voltage Level	Notes[1)]
0000_B	-	out of valid operation range
0001_B	3.0 V	LEV1V: reset request
0010_B - 0101_B	3.1 V- 3.4 V	step width is 0.1 V
0110_B	3.6 V	
0111_B	4.0 V	
1000_B	4.2 V	
1001_B	4.5 V	LEV2V: no request
1010_B - 1110_B	4.6 V - 5.0 V	step width is 0.1 V
1111_B	5.5 V	

1) The indicated default levels for LEV1V and LEV2V are selected automatically after a power-on reset.

Coding of bit fields LEVxV in PVC Configuration Registers

The core voltages are controlled internally to the nominal value of 1.5 V; a variation of ±10 % is allowed. These operation conditions limit the possible PVC monitoring values to the predefined reset values shown in **Table 23**.

Table 23 Coding of bit fields LEVxV in Registers PVCyCONz

Code	Voltage Level	Notes[1)]
000_B-011_B	-	out of valid operation range
100_B	1.35 V	LEV1V: reset request
101_B	1.45 V	LEV2V: interrupt request[2)]
110_B - 111_B	-	out of valid operation range

1) The indicated default levels for LEV1V and LEV2V are selected automatically after a power-on reset.

2) Due to variations of the tolerance of both the Embedded Voltage Regulators (EVR) and the PVC levels, this interrupt can be triggered inadvertently, even though the core voltage is within the normal range. It is, therefore, recommended not to use this warning level.

The timing in the AC Characteristics refers to TCSs. Timing must be calculated using the minimum TCS possible under the given circumstances.
The actual minimum value for TCS depends on the jitter of the PLL. Because the PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or oscillator), the accumulated jitter is limited. This means that the relative deviation for periods of more than one TCS is lower than for a single TCS (see formulas and **Figure 20**).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler K2 to generate the system clock signal f_{SYS}. The number of VCO cycles is K2 × **T**, where **T** is the number of consecutive f_{SYS} cycles (TCS).

The maximum accumulated jitter (long-term jitter) D_{Tmax} is defined by:

D_{Tmax} [ns] = $\pm(220 / (K2 \times f_{SYS}) + 4.3)$

This maximum value is applicable, if either the number of clock cycles T > (f_{SYS} / 1.2) or the prescaler value K2 > 17.

In all other cases for a timeframe of **T** × TCS the accumulated jitter D_T is determined by:

D_T [ns] = $D_{Tmax} \times [(1 - 0.058 \times K2) \times (T - 1) / (0.83 \times f_{SYS} - 1) + 0.058 \times K2]$

f_{SYS} in [MHz] in all formulas.

Example, for a period of 3 TCSs @ 33 MHz and K2 = 4:

$D_{max} = \pm(220 / (4 \times 33) + 4.3) = 5.97$ ns (Not applicable directly in this case!)

$D_3 = 5.97 \times [(1 - 0.058 \times 4) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 4]$
$= 5.97 \times [0.768 \times 2 / 26.39 + 0.232]$
$= 1.7$ ns

Example, for a period of 3 TCSs @ 33 MHz and K2 = 2:

$D_{max} = \pm(220 / (2 \times 33) + 4.3) = 7.63$ ns (Not applicable directly in this case!)

$D_3 = 7.63 \times [(1 - 0.058 \times 2) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 2]$
$= 7.63 \times [0.884 \times 2 / 26.39 + 0.116]$
$= 1.4$ ns

4.7.3 External Clock Input Parameters

These parameters specify the external clock generation for the XE164xN. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2.
- By supplying an **external clock signal**
  - This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain).

If connected to CLKIN1, the input signal must reach the defined input levels V_{IL} and V_{IH}. If connected to XTAL1, a minimum amplitude V_{AX1} (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

Note: The given clock timing parameters (t_1 … t_4) are only valid for an external clock input signal.

Note: Operating Conditions apply.

Table 26 External Clock Input Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Oscillator frequency	f_{OSC} SR	4	–	40	MHz	Input= Clock Signal
		4	–	16	MHz	Input= Crystal or Ceramic Resonator
XTAL1 input current absolute value	$\|I_{IL}\|$ CC	–	–	20	µA	
Input clock high time	t_1 SR	6	–	–	ns	
Input clock low time	t_2 SR	6	–	–	ns	
Input clock rise time	t_3 SR	–	8	8	ns	
Input clock fall time	t_4 SR	–	8	8	ns	
Input voltage amplitude on XTAL1[1)]	V_{AX1} SR	0.3 x V_{DDIM}	–	–	V	$f_{OSC} \geq$ 4 MHz; $f_{OSC} <$ 16 MHz
		0.4 x V_{DDIM}	–	–	V	$f_{OSC} \geq$ 16 MHz; $f_{OSC} <$ 25 MHz
		0.5 x V_{DDIM}	–	–	V	$f_{OSC} \geq$ 25 MHz; $f_{OSC} \leq$ 40 MHz
Input voltage range limits for signal on XTAL1	V_{IX1} SR	-1.7 + V_{DDIM}	–	1.7	V	[2)]

Table 27 Standard Pad Parameters for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	23 + 0.6 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Medium
		–	–	11.6 + 0.22 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Medium
		–	–	4.2 + 0.14 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Sharp
		–	–	20.6 + 0.22 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Slow
		–	–	212 + 1.9 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Weak

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and Σ-I_{OH}) must remain below 50 mA.

Table 32 External Bus Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output valid delay for $\overline{RD}$, $\overline{WR}$(L/$\overline{H}$)	t_{10} CC	–	11	20	ns	
Output valid delay for $\overline{BHE}$, ALE	t_{11} CC	–	10	21	ns	
Address output valid delay for A23 ... A0	t_{12} CC	–	11	22	ns	
Address output valid delay for AD15 ... AD0 (MUX mode)	t_{13} CC	–	10	22	ns	
Output valid delay for $\overline{CS}$	t_{14} CC	–	10	13	ns	
Data output valid delay for AD15 ... AD0 (write data, MUX mode)	t_{15} CC	–	10	22	ns	
Data output valid delay for D15 ... D0 (write data, DEMUX mode)	t_{16} CC	–	10	22	ns	
Output hold time for $\overline{RD}$, $\overline{WR}$(L/$\overline{H}$)	t_{20} CC	-2	8	10	ns	
Output hold time for $\overline{BHE}$, ALE	t_{21} CC	-2	8	10	ns	
Address output hold time for AD15 ... AD0	t_{23} CC	-3	8	10	ns	
Output hold time for $\overline{CS}$	t_{24} CC	-3	8	11	ns	
Data output hold time for D15 ... D0 and AD15 ... AD0	t_{25} CC	-3	8	10	ns	
Input setup time for READY, D15 ... D0, AD15 ... AD0	t_{30} SR	29	17	–	ns	
Input hold time READY, D15 ... D0, AD15 ... AD0[1)]	t_{31} SR	0	-9	–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.

Table 38 DAP Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period[1]	t_{11} SR	25	–	–	ns	
DAP0 high time	t_{12} SR	8	–	–	ns	
DAP0 low time[1]	t_{13} SR	8	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	4	ns	
DAP0 clock fall time	t_{15} SR	–	–	4	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6	–	–	ns	
DAP1 hold after DAP0 rising edge	t_{17} SR	6	–	–	ns	
DAP1 valid per DAP0 clock period[2]	t_{19} CC	12	17	–	ns	

1) See the DAP chapter for clock rate restrictions in the Active::IDLE protocol state.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

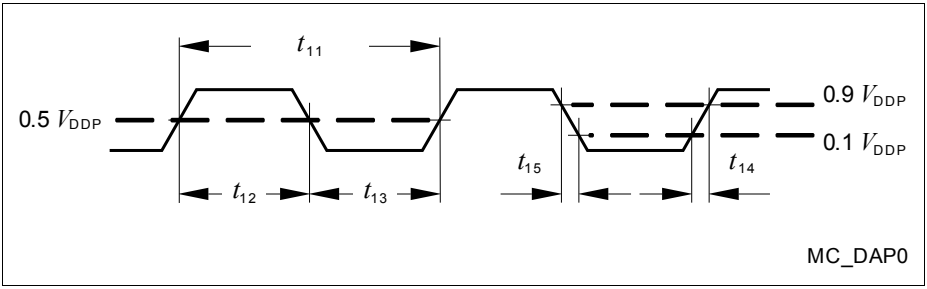

Figure 27 Test Clock Timing (DAP0)