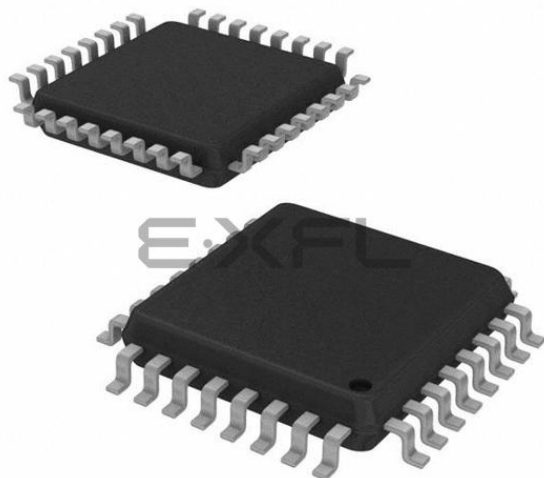




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08rn32w1mlc

- Input/Output
 - Up to 55 GPIOs including one output-only pin
 - Two 8-bit keyboard interrupt modules (KBI)
 - Two true open-drain output pins
 - Eight, ultra-high current sink pins supporting 20 mA source/sink current
- Package options
 - 64-pin LQFP
 - 48-pin LQFP
 - 32-pin LQFP

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2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-6000	+6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 125°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Symbol	Description	Min.	Max.	Unit
V_{DD}	Supply voltage	-0.3	5.8	V
I_{DD}	Maximum current into V_{DD}	—	120	mA

Table continues on the next page...

Symbol	Description	Min.	Max.	Unit
V_{DIO}	Digital input voltage (except RESET, EXTAL, XTAL, or true open drain pin PTA2 and PTA3)	-0.3	$V_{DD} + 0.3$	V
	Digital input voltage (true open drain pin PTA2 and PTA3)	-0.3	6	V
V_{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

1. All digital I/O pins, except open-drain pin PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD} . PTA2 and PTA3 is only clamped to V_{SS} .

5 General

5.1 Nonswitching electrical specifications

5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 2. DC characteristics

Symbol	C	Descriptions			Min	Typical ¹	Max	Unit
—	—	Operating voltage			2.7	—	5.5	V
V_{OH}	C	Output high voltage	All I/O pins, standard-drive strength	5 V, $I_{load} = -5$ mA	$V_{DD} - 0.8$	—	—	V
	C			3 V, $I_{load} = -2.5$ mA	$V_{DD} - 0.8$	—	—	V
	C	High current drive pins, high-drive strength ^{2, 2}		5 V, $I_{load} = -20$ mA	$V_{DD} - 0.8$	—	—	V
	C			3 V, $I_{load} = -10$ mA	$V_{DD} - 0.8$	—	—	V
I_{OHT}	D	Output high current	Max total I_{OH} for all ports	5 V	—	—	-100	mA
				3 V	—	—	-50	
V_{OL}	C	Output low voltage	All I/O pins, standard-drive strength	5 V, $I_{load} = 5$ mA	—	—	0.8	V
	C			3 V, $I_{load} = 2.5$ mA	—	—	0.8	V
	C	High current drive pins, high-drive strength ²		5 V, $I_{load} = 20$ mA	—	—	0.8	V
	C			3 V, $I_{load} = 10$ mA	—	—	0.8	V

Table continues on the next page...

Table 2. DC characteristics (continued)

Symbol	C	Descriptions			Min	Typical ¹	Max	Unit
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	50	
V_{IH}	P	Input high voltage	All digital inputs	$V_{DD} > 4.5V$	$0.70 \times V_{DD}$	—	—	V
	C			$V_{DD} > 2.7V$	$0.75 \times V_{DD}$	—	—	
V_{IL}	P	Input low voltage	All digital inputs	$V_{DD} > 4.5V$	—	—	$0.30 \times V_{DD}$	V
	C			$V_{DD} > 2.7V$	—	—	$0.35 \times V_{DD}$	
V_{hys}	C	Input hysteresis	All digital inputs	—	$0.06 \times V_{DD}$	—	—	mV
I_{In}	P	Input leakage current	All input only pins (per pin)	$V_{IN} = V_{DD}$ or V_{SS}	—	0.1	1	μA
I_{OZ}	P	Hi-Z (off-state) leakage current	All input/output (per pin)	$V_{IN} = V_{DD}$ or V_{SS}	—	0.1	1	μA
I_{OZTOT}	C	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	$V_{IN} = V_{DD}$ or V_{SS}	—	—	2	μA
R_{PU}	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	k Ω
R_{PU}^3	P	Pullup resistors	PTA2 and PTA3 pin	—	30.0	—	60.0	k Ω
I_{IC}	D	DC injection current ^{4, 5, 6}	Single pin limit	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	-0.2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{in}	C	Input capacitance, all pins		—	—	—	7	pF
V_{RAM}	C	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB4, PTB5 support ultra high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD} .
5. Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{IN} > V_{DD}$) is higher than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 3. LVD and POR Specification

Symbol	C	Description	Min	Typ	Max	Unit
V_{POR}	D	POR re-arm voltage ^{1, 2}	1.5	1.75	2.0	V

Table continues on the next page...

Table 3. LVD and POR Specification (continued)

Symbol	C	Description		Min	Typ	Max	Unit
V _{LVDH}	C	Falling low-voltage detect threshold - high range (LVDV = 1) ³		4.2	4.3	4.4	V
V _{LVW1H}	C	Falling low-voltage warning threshold - high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V _{LVW2H}	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V _{LVW3H}	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V _{LVW4H}	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V _{HYSH}	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V _{LVDL}	C	Falling low-voltage detect threshold - low range (LVDV = 0)		2.56	2.61	2.66	V
V _{LVDW1L}	C	Falling low-voltage warning threshold - low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V _{LVDW2L}	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V _{LVDW3L}	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V _{LVDW4L}	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V _{HYSDL}	C	Low range low-voltage detect hysteresis		—	40	—	mV
V _{HYSWL}	C	Low range low-voltage warning hysteresis		—	80	—	mV
V _{BG}	P	Buffered bandgap output ⁴		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. POR ramp time must be longer than 20 μ s/V to get a stable startup.
3. Rising thresholds are falling threshold + hysteresis.
4. Voltage factory trimmed at V_{DD} = 5.0 V, Temp = 125 °C

Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (low drive strength) ($V_{DD} = 5\text{ V}$)

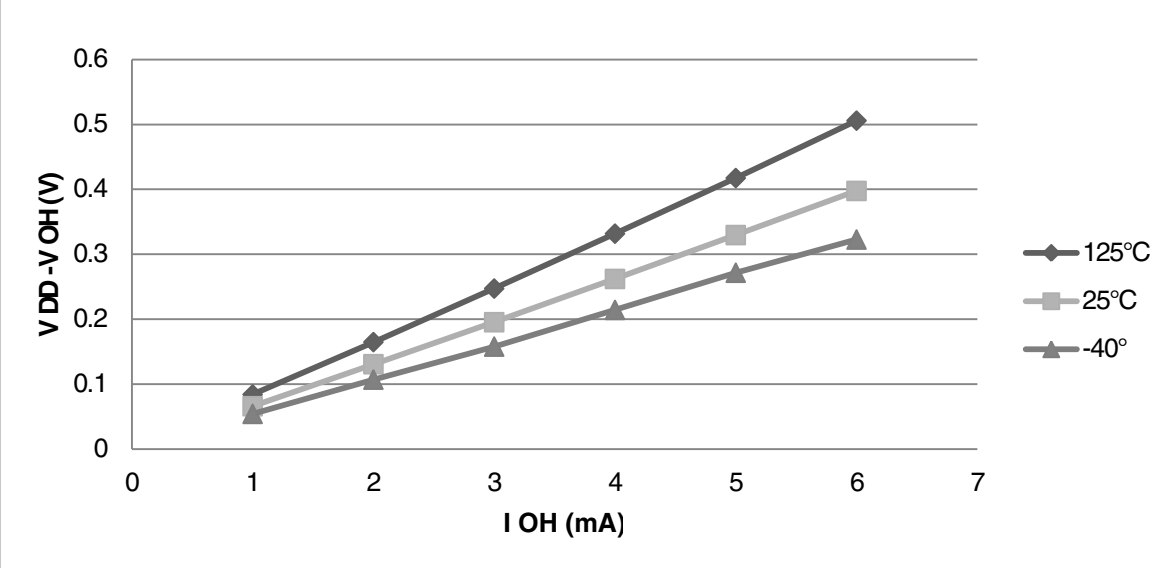


Figure 1. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (standard drive strength) ($V_{DD} = 5\text{ V}$)

Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (low drive strength) ($V_{DD} = 3\text{ V}$)

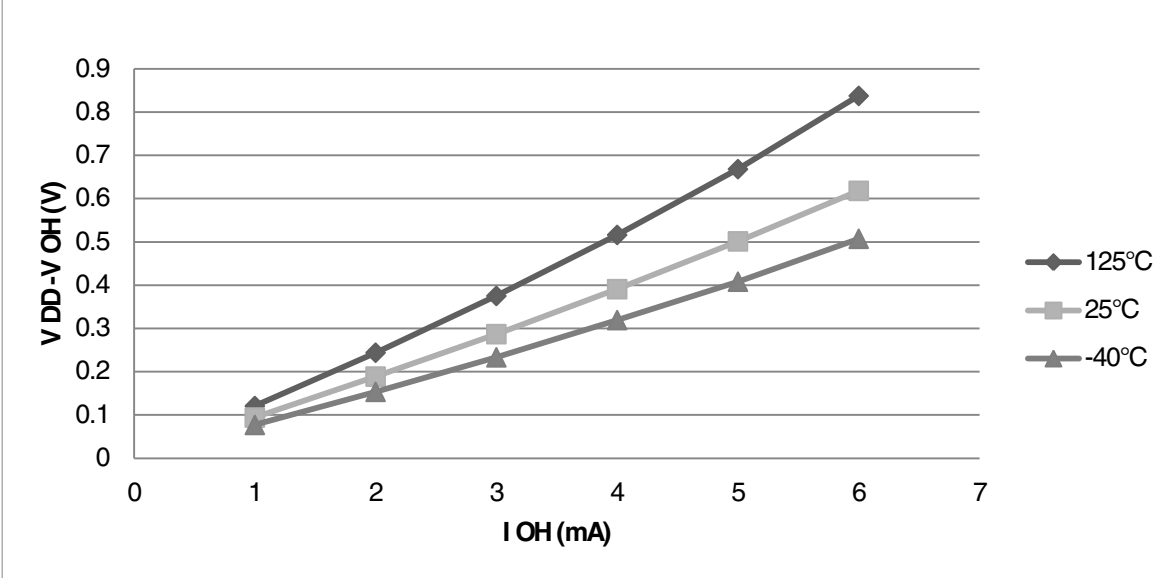


Figure 2. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (standard drive strength) ($V_{DD} = 3\text{ V}$)

Typical I_{OL} Vs. V_{OL} (low drive strength) ($V_{DD} = 5\text{ V}$)

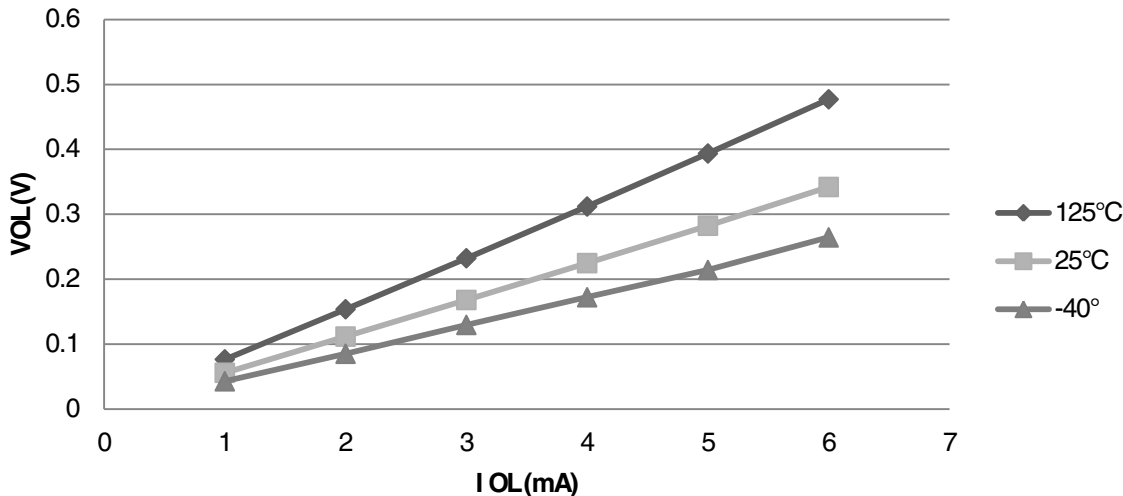


Figure 5. Typical I_{OL} Vs. V_{OL} (standard drive strength) ($V_{DD} = 5\text{ V}$)

Typical I_{OL} Vs. V_{OL} (low drive strength) ($V_{DD} = 3\text{ V}$)

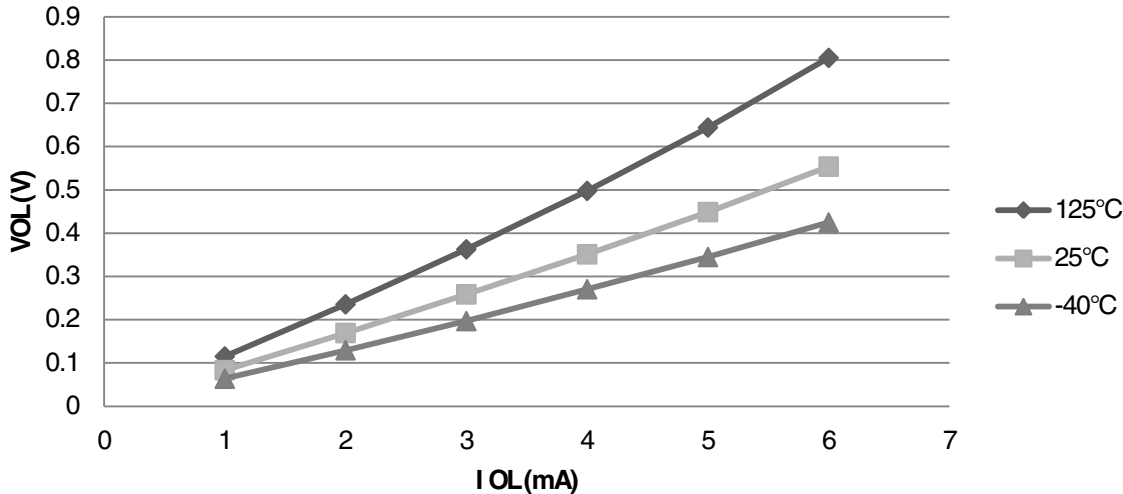


Figure 6. Typical I_{OL} Vs. V_{OL} (standard drive strength) ($V_{DD} = 3\text{ V}$)

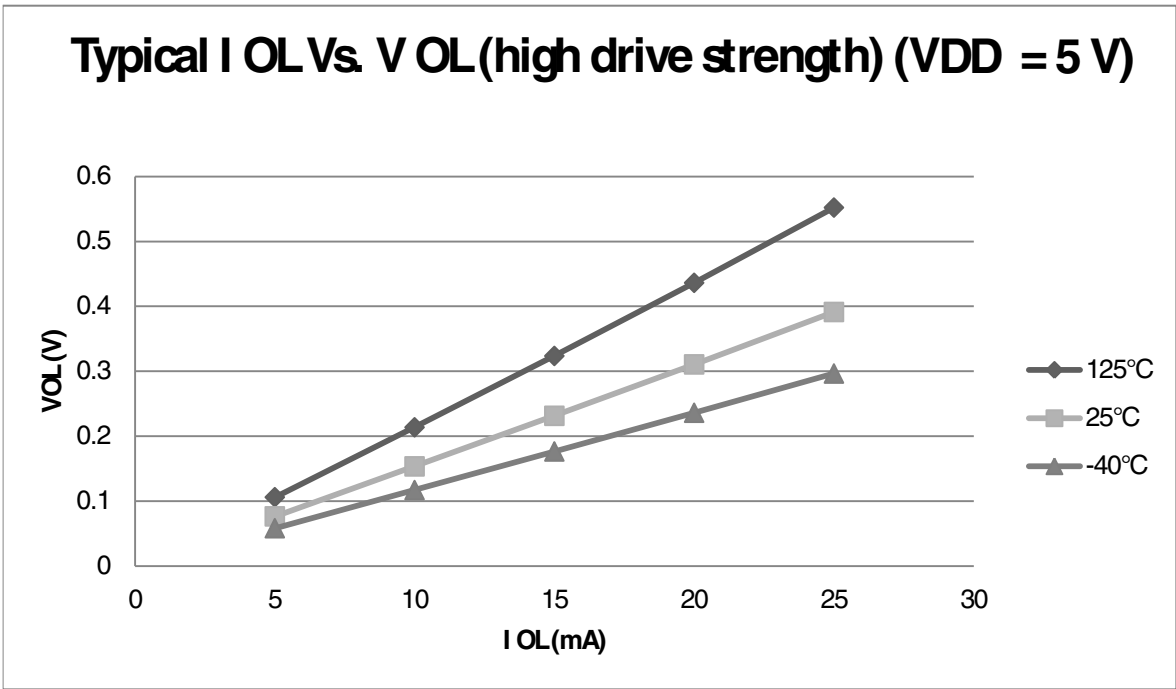


Figure 7. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 5\text{ V}$)

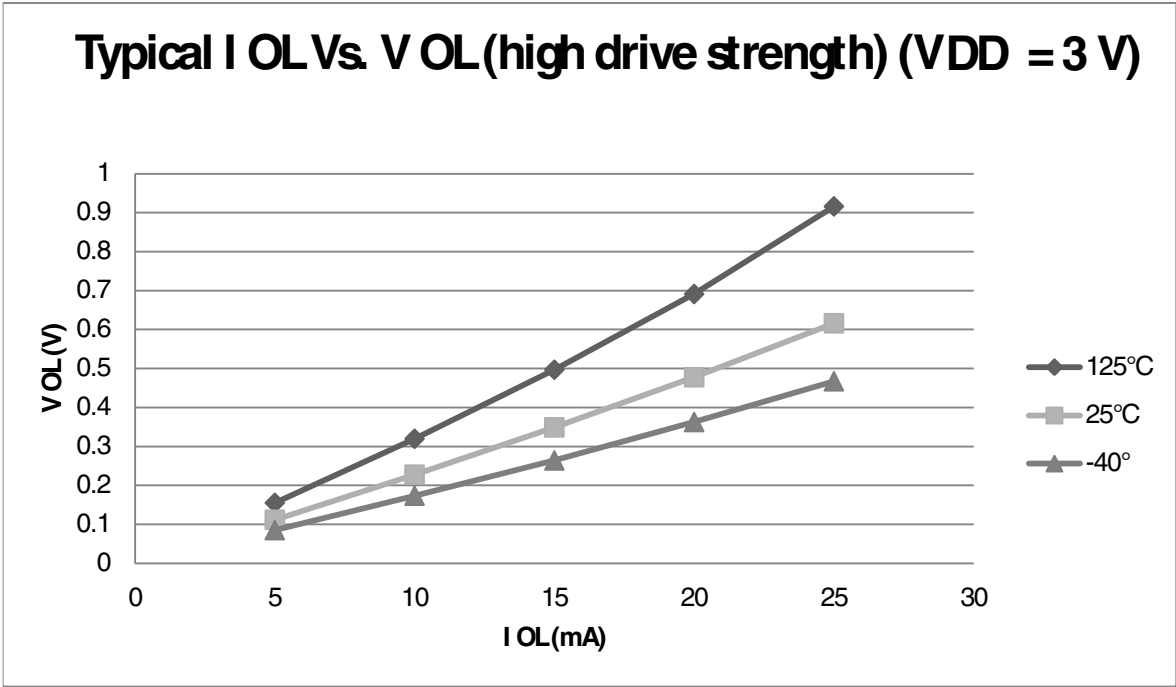


Figure 8. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 3\text{ V}$)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp
1	C	Run supply current FEI mode, all modules on; run from flash	RI _{DD}	20 MHz	5	12.6	—	mA	-40 to 125 °C
	C			10 MHz		7.2	—		
	C			1 MHz		2.4	—		
	C			20 MHz	3	9.6	—		
	C			10 MHz		6.1	—		
	C			1 MHz		2.1	—		
2	C	Run supply current FEI mode, all modules off & gated; run from flash	RI _{DD}	20 MHz	5	10.5	—	mA	-40 to 125 °C
	C			10 MHz		6.2	—		
	C			1 MHz		2.3	—		
	C			20 MHz	3	7.4	—		
	C			10 MHz		5.0	—		
	C			1 MHz		2.0	—		
3	P	Run supply current FBE mode, all modules on; run from RAM	RI _{DD}	20 MHz	5	12.1	14.8	mA	-40 to 125 °C
	C			10 MHz		6.5	—		
	C			1 MHz		1.8	—		
	P			20 MHz	3	9.1	11.8		
	C			10 MHz		5.5	—		
	C			1 MHz		1.5	—		
4	P	Run supply current FBE mode, all modules off & gated; run from RAM	RI _{DD}	20 MHz	5	9.8	12.3	mA	-40 to 125 °C
	C			10 MHz		5.4	—		
	C			1 MHz		1.6	—		
	P			20 MHz	3	6.9	9.2		
	C			10 MHz		4.4	—		
	C			1 MHz		1.4	—		
5	C	Wait mode current FEI mode, all modules on	WI _{DD}	20 MHz	5	7.8	—	mA	-40 to 125 °C
	C			10 MHz		4.5	—		
	C			1 MHz		1.3	—		
	C			20 MHz	3	5.1	—		
	C			10 MHz		3.5	—		
	C			1 MHz		1.2	—		
6	C	Stop3 mode supply current no clocks active (except 1 kHz LPO clock) ^{2,3}	S3I _{DD}	—	5	3.8	—	μA	-40 to 125 °C
	C			—	3	3	—		-40 to 125 °C

Table continues on the next page...

5.2.2 Debug trace timing specifications

Table 6. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
t_{cyc}	Clock period	Frequency dependent		MHz
t_{wl}	Low pulse width	2	—	ns
t_{wh}	High pulse width	2	—	ns
t_r	Clock and data rise time	—	3	ns
t_f	Clock and data fall time	—	3	ns
t_s	Data setup	3	—	ns
t_h	Data hold	2	—	ns

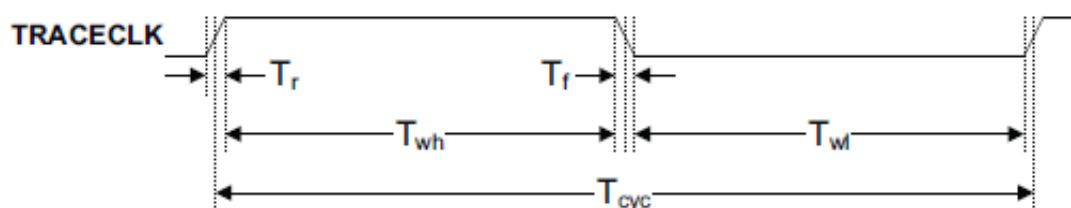


Figure 11. TRACE_CLKOUT specifications

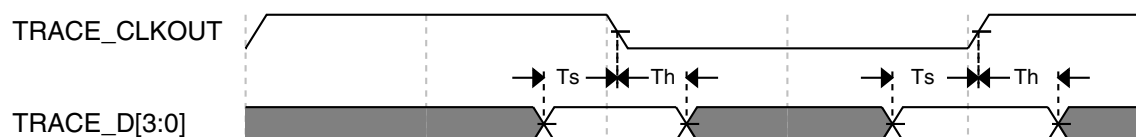


Figure 12. Trace data specifications

5.2.3 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 7. FTM input timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz

Table continues on the next page...

Table 8. Thermal characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H -40 to 125	$^{\circ}\text{C}$
Junction temperature range	T_J	-40 to 135	$^{\circ}\text{C}$
Thermal resistance single-layer board			
64-pin LQFP	θ_{JA}	71	$^{\circ}\text{C}/\text{W}$
48-pin LQFP	θ_{JA}	81	$^{\circ}\text{C}/\text{W}$
32-pin LQFP	θ_{JA}	86	$^{\circ}\text{C}/\text{W}$
Thermal resistance four-layer board			
64-pin LQFP	θ_{JA}	53	$^{\circ}\text{C}/\text{W}$
48-pin LQFP	θ_{JA}	57	$^{\circ}\text{C}/\text{W}$
32-pin LQFP	θ_{JA}	57	$^{\circ}\text{C}/\text{W}$

The average chip-junction temperature (T_J) in $^{\circ}\text{C}$ can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

T_A = Ambient temperature, $^{\circ}\text{C}$

θ_{JA} = Package thermal resistance, junction-to-ambient, $^{\circ}\text{C}/\text{W}$

$$P_D = P_{\text{int}} + P_{\text{I/O}}$$

$P_{\text{int}} = I_{\text{DD}} \times V_{\text{DD}}$, Watts - chip internal power

$P_{\text{I/O}}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{\text{I/O}} \ll P_{\text{int}}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{\text{I/O}}$ is neglected) is:

$$P_D = K \div (T_J + 273 \text{ }^{\circ}\text{C})$$

Solving the equations above for K gives:

$$K = P_D \times (T_A + 273 \text{ }^{\circ}\text{C}) + \theta_{JA} \times (P_D)^2$$

where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A .

6 Peripheral operating requirements and behaviors

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

6.3 Analog

6.3.1 ADC characteristics

Table 11. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} ($V_{DD}-V_{DDAD}$)	ΔV_{DDA}	-100	0	+100	mV	
Ground voltage	Delta to V_{SS} ($V_{SS}-V_{SSA}$) ²	ΔV_{SSA}	-100	0	+100	mV	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	k Ω	—
Analog source resistance	12-bit mode	R_{AS}	—	—	2	k Ω	External to MCU
	• $f_{ADCK} > 4$ MHz		—	—	5		
	• $f_{ADCK} < 4$ MHz		—	—	5		
	10-bit mode		—	—	5		
	• $f_{ADCK} > 4$ MHz		—	—	10		
	• $f_{ADCK} < 4$ MHz		—	—	10		
	8-bit mode		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK}=1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.

Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error ^{2, 2}	12-bit mode	T	E_{TUE}	—	±5.0	—	LSB ^{3, 3}
	10-bit mode	P		—	±1.5	±2.0	
	8-bit mode	P		—	±0.7	±1.0	
Differential Non-Linearity	12-bit mode	T	DNL	—	±1.0	—	LSB ³
	10-bit mode ^{4, 4}	P		—	±0.25	±0.5	
	8-bit mode ⁴	P		—	±0.15	±0.25	
Integral Non-Linearity	12-bit mode	T	INL	—	±1.0	—	LSB ³
	10-bit mode	T		—	±0.3	±0.5	
	8-bit mode	T		—	±0.15	±0.25	
Zero-scale error ^{5, 5}	12-bit mode	C	E_{ZS}	—	±2.0	—	LSB ³
	10-bit mode	P		—	±0.25	±1.0	
	8-bit mode	P		—	±0.65	±1.0	
Full-scale error ⁶	12-bit mode	T	E_{FS}	—	±2.5	—	LSB ³
	10-bit mode	T		—	±0.5	±1.0	
	8-bit mode	T		—	±0.5	±1.0	
Quantization error	≤12 bit modes	D	E_Q	—	—	±0.5	LSB ³
Input leakage error ⁷	all modes	D	E_{IL}	$I_{IN} * R_{AS}$			mV
Temp sensor slope	-40°C– 25°C	D	m	—	3.266	—	mV/°C
	25°C– 125°C			—	3.638	—	
Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.396	—	V

1. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK}=1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization.
3. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
4. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
5. $V_{ADIN} = V_{SSA}$
6. $V_{ADIN} = V_{DDA}$
7. I_{IN} = leakage current (refer to DC characteristics)

6.3.2 Analog comparator (ACMP) electricals

Table 13. Comparator electrical specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DDA}	2.7	—	5.5	V
T	Supply current (Operation mode)	I_{DDA}	—	10	20	μA
D	Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DDA}	V
P	Analog input offset voltage	V_{AIO}	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
T	Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
C	Propagation Delay	t_D	—	0.4	1	μs

6.4 Communication interfaces

6.4.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} , unless noted, and 100 pF load on all SPI pins. All timing assumes slew rate control is disabled and high drive strength is enabled for SPI output pins.

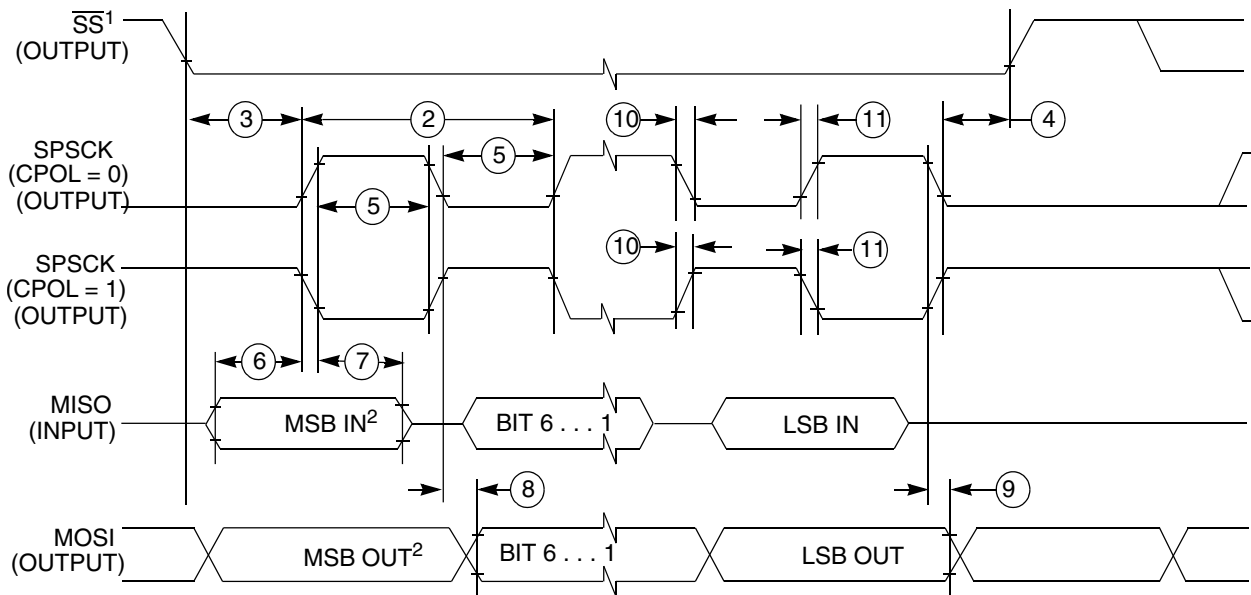
Table 14. SPI master mode timing

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	$f_{Bus}/2048$	$f_{Bus}/2$	Hz	f_{Bus} is the bus clock
2	t_{SPSCK}	SPSCK period	$2 \times t_{Bus}$	$2048 \times t_{Bus}$	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{Bus} - 30$	$1024 \times t_{Bus}$	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	25	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—

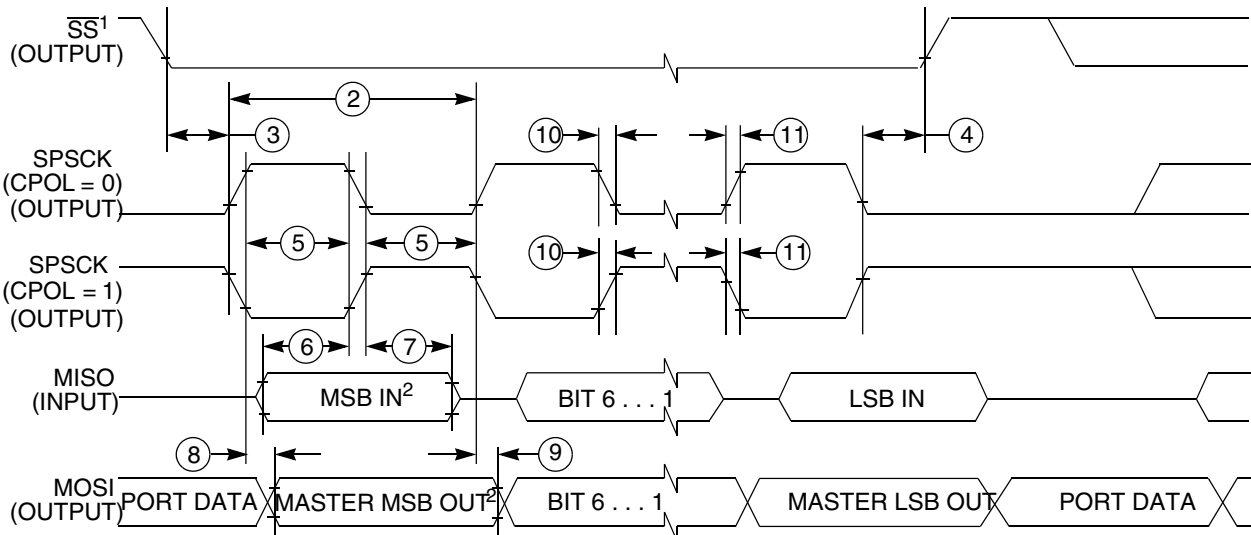
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Table 14. SPI master mode timing (continued)

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
10	t_{RI}	Rise time input	—	$t_{Bus} - 25$	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

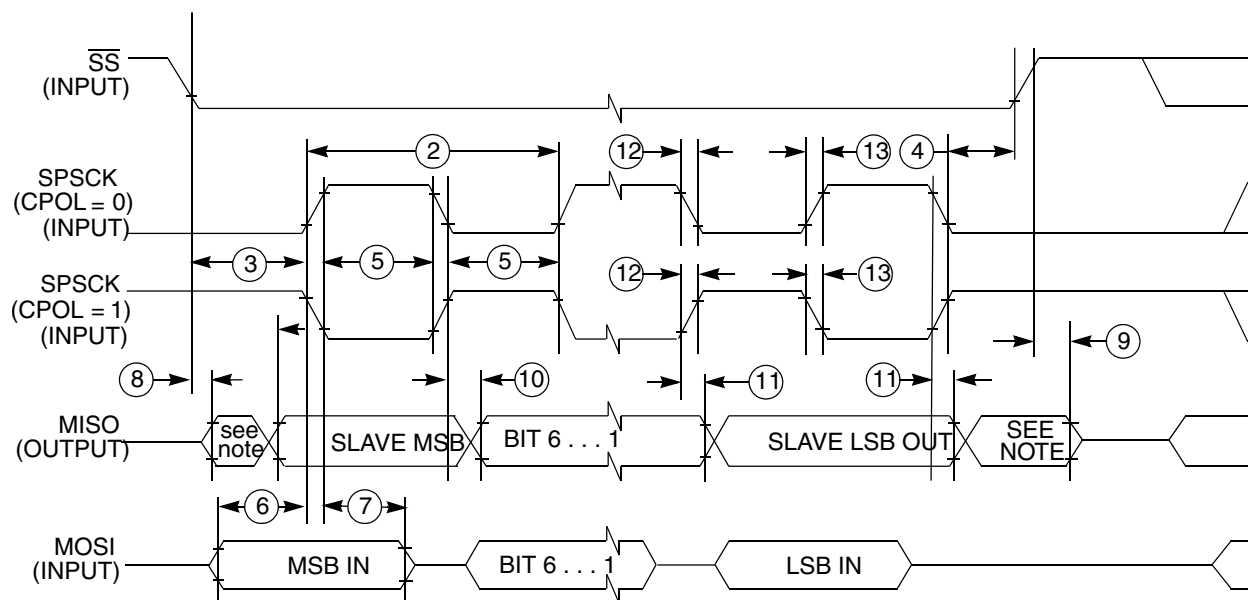
Figure 17. SPI master mode timing (CPHA=0)


1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

Table 15. SPI slave mode timing

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{Bus}/4$	Hz	f_{Bus} is the bus clock as defined in .
2	t_{SPSCK}	SPSCK period	$4 \times t_{Bus}$	—	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1	—	t_{Bus}	—
4	t_{Lag}	Enable lag time	1	—	t_{Bus}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{Bus} - 30$	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{Bus}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{Bus}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	$t_{Bus} - 25$	ns	—
	t_{FI}	Fall time input	—	$t_{Bus} - 25$	ns	—
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output	—	25	ns	—



NOTE: Not defined

Figure 19. SPI slave mode timing (CPHA = 0)

Table 17. Pin availability by package pin-count (continued)

Pin Number			Lowest Priority <-- --> Highest				
64-LQFP	48-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
20	16	11	PTC3	FTM2CH3	—	ADP11	—
21	17	12	PTC2	FTM2CH2	—	ADP10	—
22	18	—	PTD7	KBI1P7	TXD2	—	—
23	19	—	PTD6	KBI1P6	RXD2	—	—
24	20	—	PTD5	KBI1P5	—	—	—
25	21	13	PTC1	—	FTM2CH1	ADP9	TSI7
26	22	14	PTC0	—	FTM2CH0	ADP8	TSI6
27	—	—	PTF7	—	—	ADP15	—
28	—	—	PTF6	—	—	ADP14	—
29	—	—	PTF5	—	—	ADP13	—
30	—	—	PTF4	—	—	ADP12	—
31	23	15	PTB3	KBI0P7	MOSI0	ADP7	TSI5
32	24	16	PTB2	KBI0P6	SPSCK0	ADP6	TSI4
33	25	17	PTB1	KBI0P5	TXD0	ADP5	TSI3
34	26	18	PTB0	KBI0P4	RXD0	ADP4	TSI2
35	—	—	PTF3	—	—	—	TSI15
36	—	—	PTF2	—	—	—	TSI14
37	27	19	PTA7	FTM2FAULT2	—	ADP3	TSI1
38	28	20	PTA6	FTM2FAULT1	—	ADP2	TSI0
39	29	—	PTE4	—	—	—	—
40	30	—	—	—	—	—	V _{SS}
41	31	—	—	—	—	—	V _{DD}
42	—	—	PTF1	—	—	—	TSI13
43	—	—	PTF0	—	—	—	TSI12
44	32	—	PTD4	KBI1P4	—	—	—
45	33	21	PTD3	KBI1P3	SS1	—	TSI11
46	34	22	PTD2	KBI1P2	MISO1	—	TSI10
47	35	23	PTA3 ^{2, 2}	KBI0P3	TXD0	SCL	—
48	36	24	PTA2 ²	KBI0P2	RXD0	SDA	—
49	37	25	PTA1	KBI0P1	FTM0CH1	ACMP1	ADP1
50	38	26	PTA0	KBI0P0	FTM0CH0	ACMP0	ADP0
51	39	27	PTC7	—	TxD1	—	TSI9
52	40	28	PTC6	—	RxD1	—	TSI8
53	41	—	PTE3	—	SS0	—	—
54	42	—	PTE2	—	MISO0	—	—
55	—	—	PTG3	—	—	—	—
56	—	—	PTG2	—	—	—	—
57	—	—	PTG1	—	—	—	—

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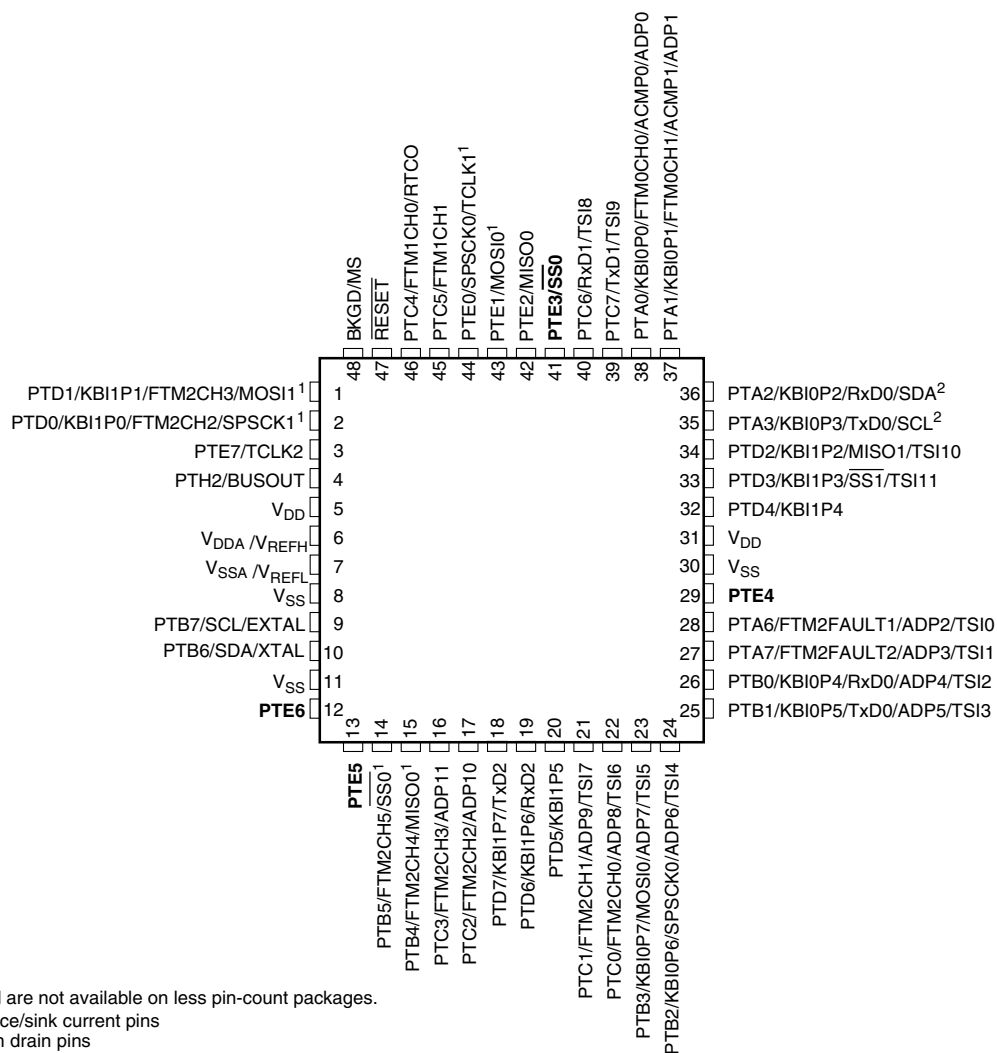


Figure 22. S9S08RN60 48-pin LQFP package

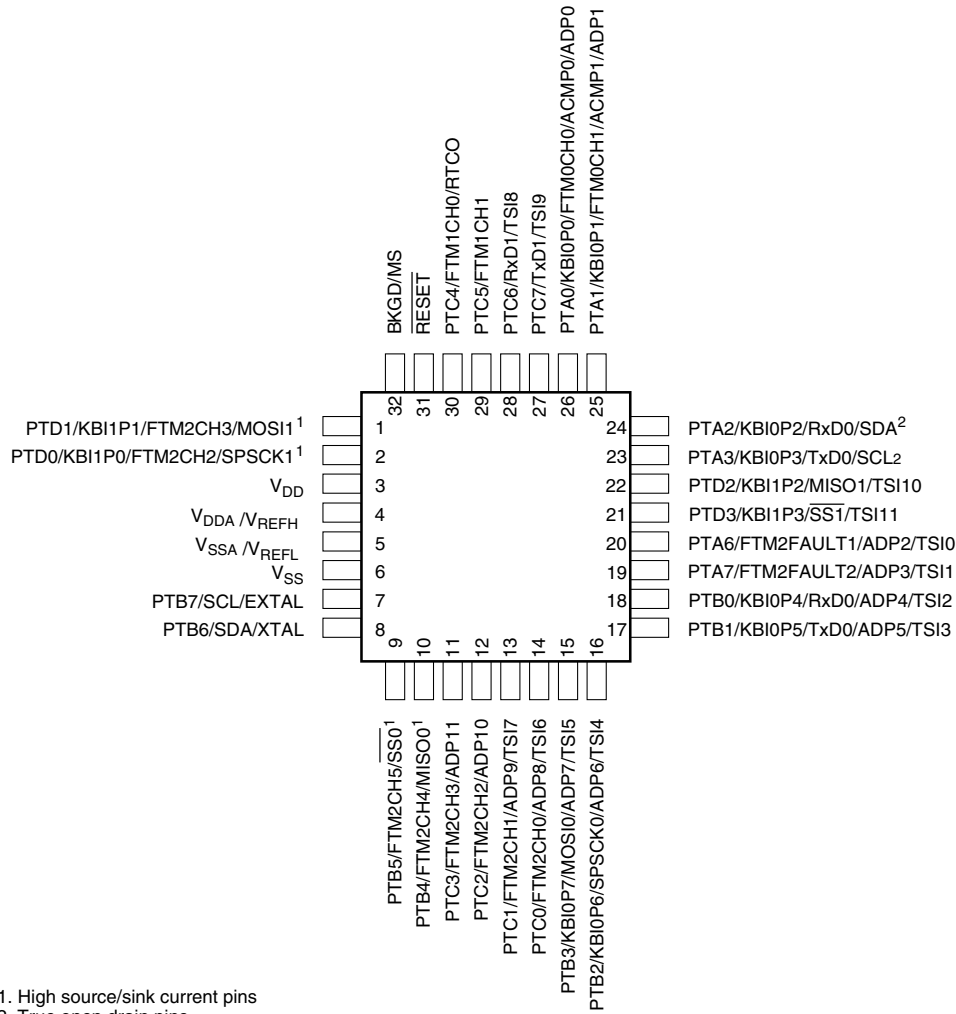


Figure 23. S9S08RN60 32-pin LQFP package

9 Revision history

The following table provides a revision history for this document.

Table 18. Revision history

Rev. No.	Date	Substantial Changes
1	01/2014	Initial Release