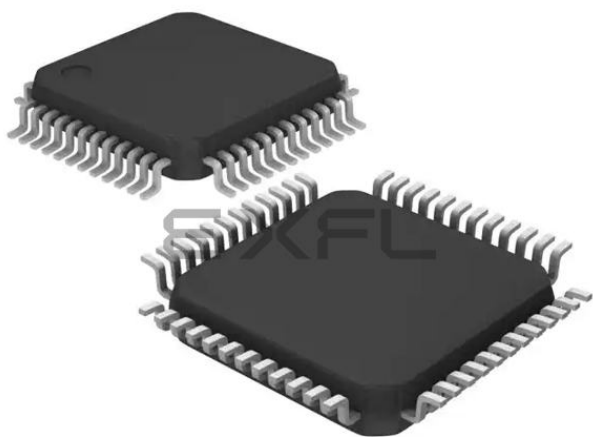




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08rn60w1vlf

- Input/Output
 - Up to 55 GPIOs including one output-only pin
 - Two 8-bit keyboard interrupt modules (KBI)
 - Two true open-drain output pins
 - Eight, ultra-high current sink pins supporting 20 mA source/sink current
- Package options
 - 64-pin LQFP
 - 48-pin LQFP
 - 32-pin LQFP

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Field	Description	Values
CC	Package designator	- LH = 64-pin LQFP - LF = 48-pin LQFP - LC = 32-pin LQFP

2.4 Example

This is an example part number:

S9S08RN60W1MLH

3 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 1. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	–55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.

2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-6000	+6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 125°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Symbol	Description	Min.	Max.	Unit
V_{DD}	Supply voltage	-0.3	5.8	V
I_{DD}	Maximum current into V_{DD}	—	120	mA

Table continues on the next page...

Table 2. DC characteristics (continued)

Symbol	C	Descriptions			Min	Typical ¹	Max	Unit
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	50	
V_{IH}	P	Input high voltage	All digital inputs	$V_{DD} > 4.5V$	$0.70 \times V_{DD}$	—	—	V
	C			$V_{DD} > 2.7V$	$0.75 \times V_{DD}$	—	—	
V_{IL}	P	Input low voltage	All digital inputs	$V_{DD} > 4.5V$	—	—	$0.30 \times V_{DD}$	V
	C			$V_{DD} > 2.7V$	—	—	$0.35 \times V_{DD}$	
V_{hys}	C	Input hysteresis	All digital inputs	—	$0.06 \times V_{DD}$	—	—	mV
I_{In}	P	Input leakage current	All input only pins (per pin)	$V_{IN} = V_{DD}$ or V_{SS}	—	0.1	1	μA
I_{OZ}	P	Hi-Z (off-state) leakage current	All input/output (per pin)	$V_{IN} = V_{DD}$ or V_{SS}	—	0.1	1	μA
I_{OZTOT}	C	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	$V_{IN} = V_{DD}$ or V_{SS}	—	—	2	μA
R_{PU}	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	k Ω
R_{PU}^3	P	Pullup resistors	PTA2 and PTA3 pin	—	30.0	—	60.0	k Ω
I_{IC}	D	DC injection current ^{4, 5, 6}	Single pin limit	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	-0.2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{in}	C	Input capacitance, all pins		—	—	—	7	pF
V_{RAM}	C	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB4, PTB5 support ultra high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD} .
5. Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{IN} > V_{DD}$) is higher than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 3. LVD and POR Specification

Symbol	C	Description	Min	Typ	Max	Unit
V_{POR}	D	POR re-arm voltage ^{1, 2}	1.5	1.75	2.0	V

Table continues on the next page...

Table 3. LVD and POR Specification (continued)

Symbol	C	Description		Min	Typ	Max	Unit
V _{LVDH}	C	Falling low-voltage detect threshold - high range (LVDV = 1) ³		4.2	4.3	4.4	V
V _{LVW1H}	C	Falling low-voltage warning threshold - high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V _{LVW2H}	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V _{LVW3H}	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V _{LVW4H}	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V _{HYSH}	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V _{LVDL}	C	Falling low-voltage detect threshold - low range (LVDV = 0)		2.56	2.61	2.66	V
V _{LVDW1L}	C	Falling low-voltage warning threshold - low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V _{LVDW2L}	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V _{LVDW3L}	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V _{LVDW4L}	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V _{HYSDL}	C	Low range low-voltage detect hysteresis		—	40	—	mV
V _{HYSWL}	C	Low range low-voltage warning hysteresis		—	80	—	mV
V _{BG}	P	Buffered bandgap output ⁴		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. POR ramp time must be longer than 20 μ s/V to get a stable startup.
3. Rising thresholds are falling threshold + hysteresis.
4. Voltage factory trimmed at V_{DD} = 5.0 V, Temp = 125 °C

Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (low drive strength) ($V_{DD} = 5\text{ V}$)

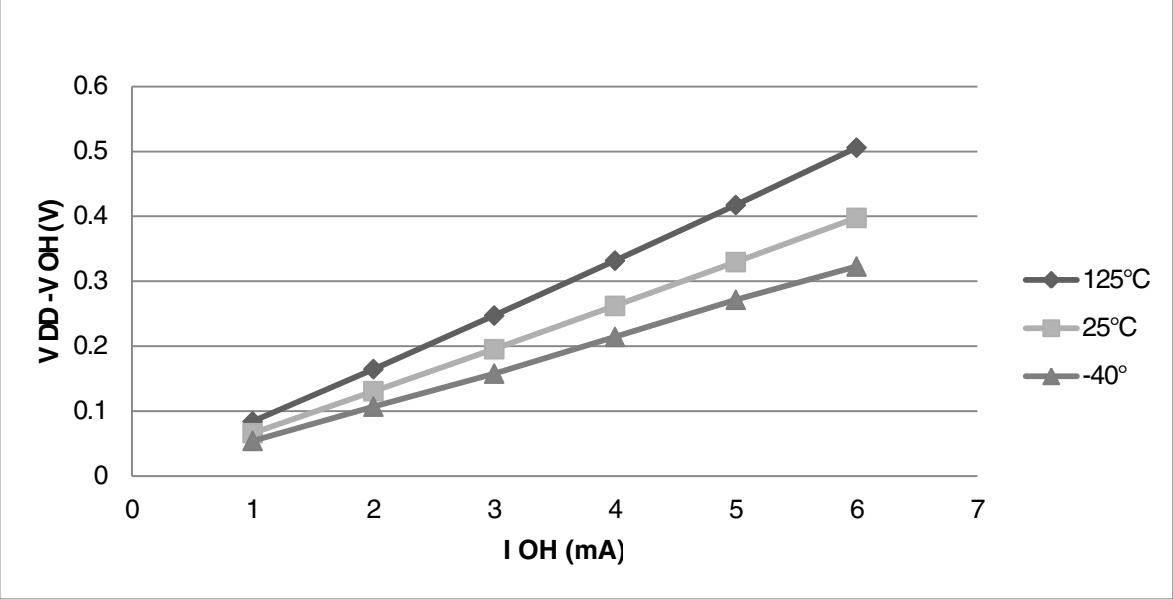


Figure 1. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (standard drive strength) ($V_{DD} = 5\text{ V}$)

Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (low drive strength) ($V_{DD} = 3\text{ V}$)

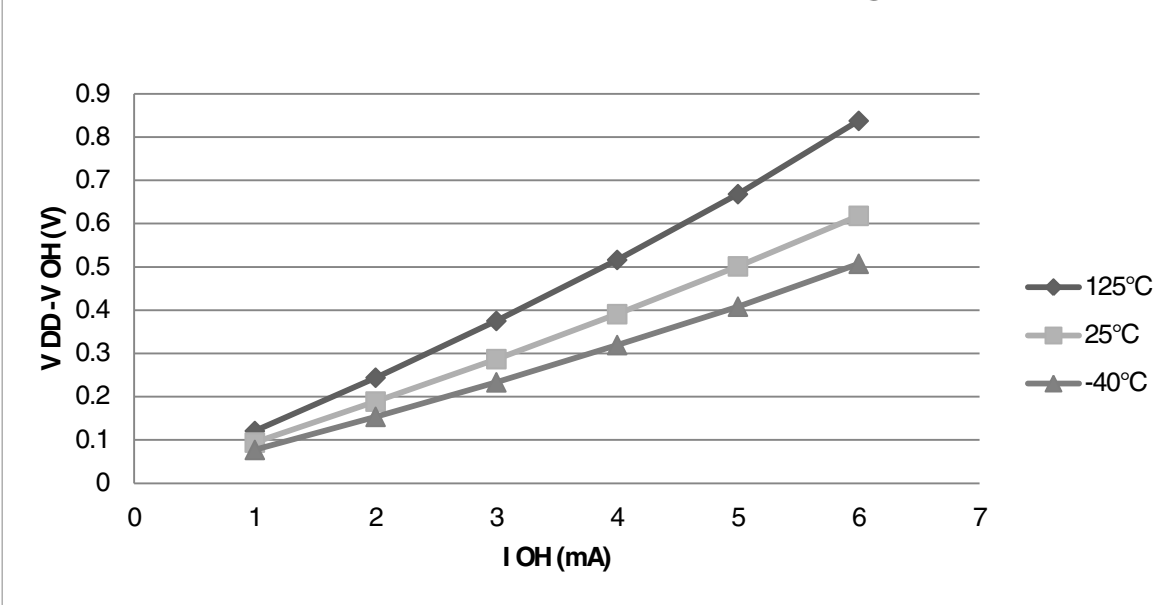


Figure 2. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (standard drive strength) ($V_{DD} = 3\text{ V}$)

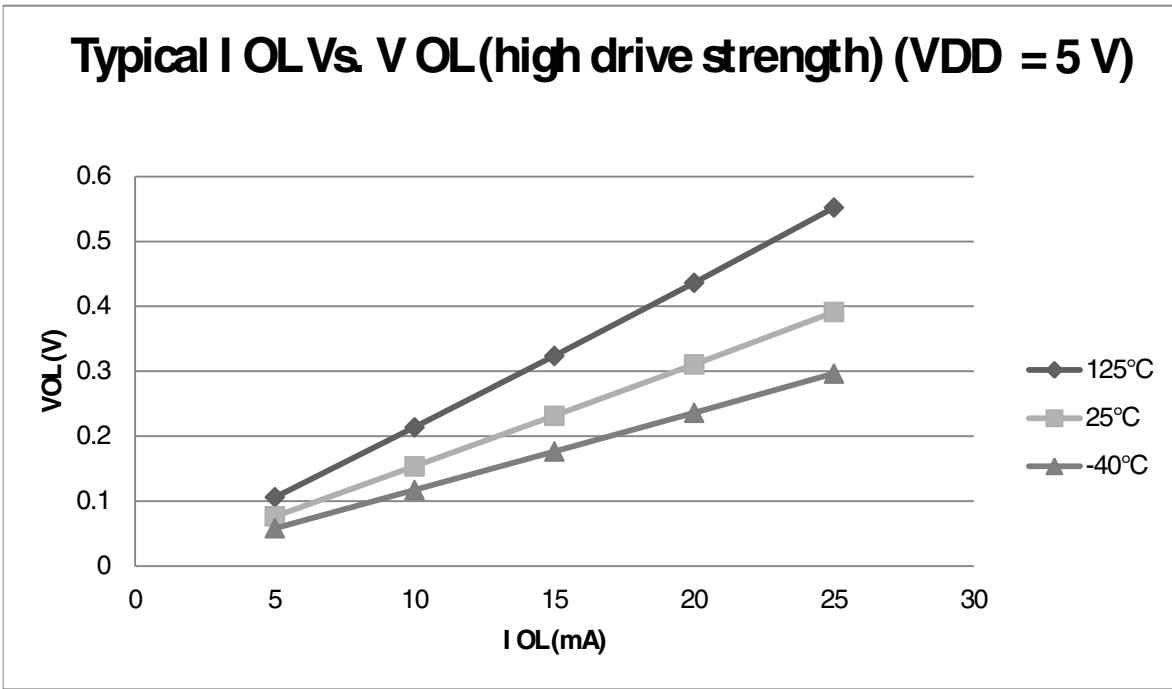


Figure 7. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 5\text{ V}$)

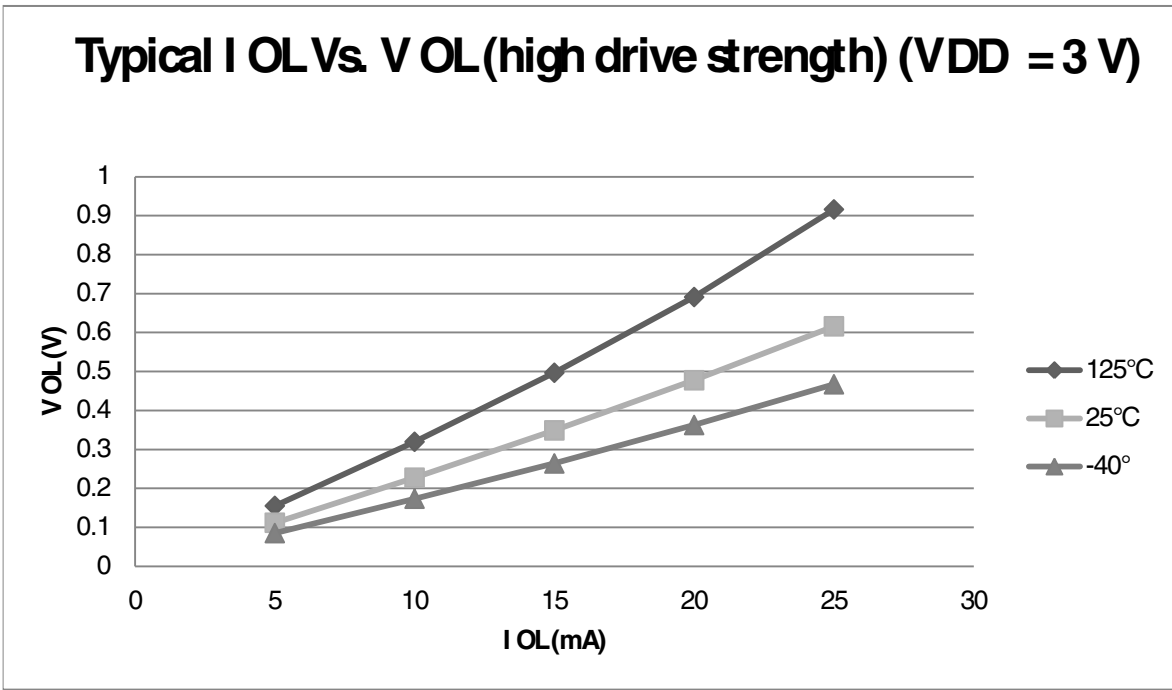


Figure 8. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 3\text{ V}$)

Table 4. Supply current characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp
7	C	ADC adder to stop3	—	—	5	44	—	μA	-40 to 125 °C
	C	ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B			3	40	—		
8	C	TSI adder to stop3 ⁴	—	—	5	111	—	μA	-40 to 125 °C
	C	PS = 010B NSCN = 0x0F EXTCHRG = 0 REFCHRG = 0 DVOLT = 01B			3	110	—		
9	C	LVD adder to stop3 ⁵	—	—	5	130	—	μA	-40 to 125 °C
	C				3	125	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. RTC adder cause <1 μA I_{DD} increase typically, RTC clock source is 1 kHz LPO clock.
3. ACMP adder cause <1 μA I_{DD} increase typically.
4. The current varies with TSI configuration and capacity of touch electrode. Please refer to [TSI electrical specifications](#).
5. LVD is periodically woken up from stop3 by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

5.1.3.1 EMC radiated emissions operating behaviors

5.2 Switching specifications

5.2.1 Control timing

Table 5. Control timing

Num	C	Rating	Symbol	Min	Typical ¹	Max	Unit
1	P	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	DC	—	20	MHz
2	P	Internal low power oscillator frequency	f_{LPO}	0.67	1.0	1.25	KHz
3	D	External reset pulse width ^{2, 2}	t_{extrst}	$1.5 \times t_{Self_reset}$	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes ³	t_{MSH}	100	—	—	ns
7	D	Keyboard interrupt pulse width	Asynchronous path ²	t_{ILIH}	100	—	ns
	D		Synchronous path	t_{IHIL}	$1.5 \times t_{cyc}$	—	ns
8	C	Port rise and fall time - Normal drive strength (HDRV_PTXx = 0) (load = 50 pF) ^{4, 4}	—	t_{Rise}	—	10.2	ns
	C		—	t_{Fall}	—	9.5	ns
	C	Port rise and fall time - Extreme high drive strength (HDRV_PTXx = 1) (load = 50 pF) ⁴	—	t_{Rise}	—	5.4	ns
	C		—	t_{Fall}	—	4.6	ns

1. Typical values are based on characterization data at $V_{DD} = 5.0$ V, 25 °C unless otherwise stated.

2. This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3. To enter BDM mode following a POR, BKGD/MS must be held low during the powerup and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD} .

4. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range -40 °C to 125 °C.

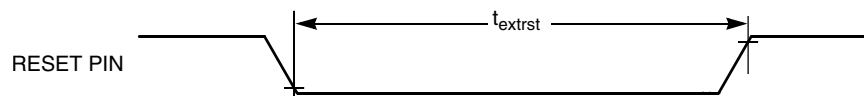


Figure 9. Reset timing

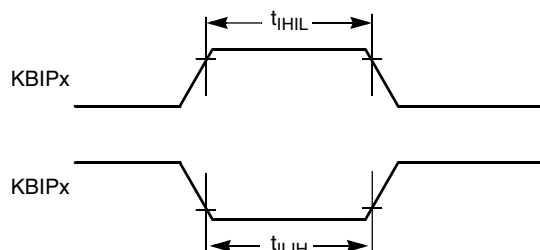


Figure 10. KBIPx timing

Table 8. Thermal characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H -40 to 125	$^{\circ}\text{C}$
Junction temperature range	T_J	-40 to 135	$^{\circ}\text{C}$
Thermal resistance single-layer board			
64-pin LQFP	θ_{JA}	71	$^{\circ}\text{C}/\text{W}$
48-pin LQFP	θ_{JA}	81	$^{\circ}\text{C}/\text{W}$
32-pin LQFP	θ_{JA}	86	$^{\circ}\text{C}/\text{W}$
Thermal resistance four-layer board			
64-pin LQFP	θ_{JA}	53	$^{\circ}\text{C}/\text{W}$
48-pin LQFP	θ_{JA}	57	$^{\circ}\text{C}/\text{W}$
32-pin LQFP	θ_{JA}	57	$^{\circ}\text{C}/\text{W}$

The average chip-junction temperature (T_J) in $^{\circ}\text{C}$ can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

T_A = Ambient temperature, $^{\circ}\text{C}$

θ_{JA} = Package thermal resistance, junction-to-ambient, $^{\circ}\text{C}/\text{W}$

$$P_D = P_{\text{int}} + P_{\text{I/O}}$$

$P_{\text{int}} = I_{\text{DD}} \times V_{\text{DD}}$, Watts - chip internal power

$P_{\text{I/O}}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{\text{I/O}} \ll P_{\text{int}}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{\text{I/O}}$ is neglected) is:

$$P_D = K \div (T_J + 273 \text{ }^{\circ}\text{C})$$

Solving the equations above for K gives:

$$K = P_D \times (T_A + 273 \text{ }^{\circ}\text{C}) + \theta_{JA} \times (P_D)^2$$

where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A .

6 Peripheral operating requirements and behaviors

6.2 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash and EEPROM memories.

Table 10. Flash characteristics

C	Characteristic	Symbol	Min ¹	Typical ²	Max ³	Unit ⁴
D	Supply voltage for program/erase -40 °C to 125 °C	V _{prog/erase}	2.7	—	5.5	V
D	Supply voltage for read operation	V _{Read}	2.7	—	5.5	V
D	NVM Bus frequency	f _{NVMBUS}	1	—	25	MHz
D	NVM Operating frequency	f _{NVMOP}	0.8	1	1.05	MHz
D	Erase Verify All Blocks	t _{VFYALL}	—	—	17338	t _{cyc}
D	Erase Verify Flash Block	t _{RD1BLK}	—	—	16913	t _{cyc}
D	Erase Verify EEPROM Block	t _{RD1BLK}	—	—	810	t _{cyc}
D	Erase Verify Flash Section	t _{RD1SEC}	—	—	484	t _{cyc}
D	Erase Verify EEPROM Section	t _{DRD1SEC}	—	—	555	t _{cyc}
D	Read Once	t _{RDONCE}	—	—	450	t _{cyc}
D	Program Flash (2 word)	t _{PGM2}	0.12	0.12	0.29	ms
D	Program Flash (4 word)	t _{PGM4}	0.20	0.21	0.46	ms
D	Program Once	t _{PGMONCE}	0.20	0.21	0.21	ms
D	Program EEPROM (1 Byte)	t _{DPGM1}	0.10	0.10	0.27	ms
D	Program EEPROM (2 Byte)	t _{DPGM2}	0.17	0.18	0.43	ms
D	Program EEPROM (3 Byte)	t _{DPGM3}	0.25	0.26	0.60	ms
D	Program EEPROM (4 Byte)	t _{DPGM4}	0.32	0.33	0.77	ms
D	Erase All Blocks	t _{ERSALL}	96.01	100.78	101.49	ms
D	Erase Flash Block	t _{ERSBLK}	95.98	100.75	101.44	ms
D	Erase Flash Sector	t _{ERSPG}	19.10	20.05	20.08	ms
D	Erase EEPROM Sector	t _{DERSPG}	4.81	5.05	20.57	ms
D	Unsecure Flash	t _{UNSECU}	96.01	100.78	101.48	ms
D	Verify Backdoor Access Key	t _{VFYKEY}	—	—	464	t _{cyc}
D	Set User Margin Level	t _{MLOADU}	—	—	407	t _{cyc}
C	FLASH Program/erase endurance T _L to T _H = -40 °C to 125 °C	n _{FLPE}	10 k	100 k	—	Cycles
C	EEPROM Program/erase endurance T _L to T _H = -40 °C to 125 °C	n _{FLPE}	50 k	500 k	—	Cycles
C	Data retention at an average junction temperature of T _{Javg} = 85°C after up to 10,000 program/erase cycles	t _{D_ret}	15	100	—	years

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. t_{cyc} = 1 / f_{NVMBUS}

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

6.3 Analog

6.3.1 ADC characteristics

Table 11. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} ($V_{DD}-V_{DDAD}$)	ΔV_{DDA}	-100	0	+100	mV	
Ground voltage	Delta to V_{SS} ($V_{SS}-V_{SSA}$) ²	ΔV_{SSA}	-100	0	+100	mV	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	k Ω	—
Analog source resistance	12-bit mode	R_{AS}	—	—	2	k Ω	External to MCU
	• $f_{ADCK} > 4$ MHz		—	—	5		
	• $f_{ADCK} < 4$ MHz		—	—	5		
	10-bit mode		—	—	5		
	• $f_{ADCK} > 4$ MHz		—	—	10		
	• $f_{ADCK} < 4$ MHz		—	—	10		
	8-bit mode		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK}=1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.

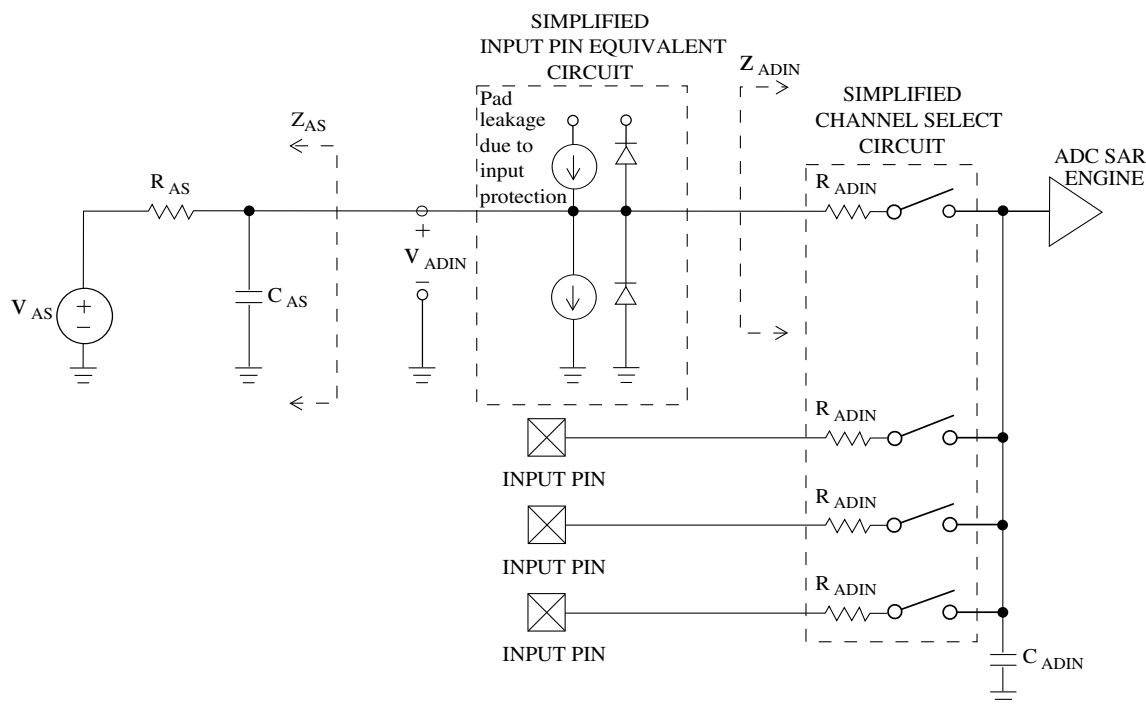


Figure 16. ADC input impedance equivalency diagram

Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	μA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	μA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	μA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	990	μA
Supply current Stop, reset, module off		T	I_{DDA}	—	0.011	1	μA

Table continues on the next page...

Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error ^{2, 2}	12-bit mode	T	E_{TUE}	—	±5.0	—	LSB ^{3, 3}
	10-bit mode	P		—	±1.5	±2.0	
	8-bit mode	P		—	±0.7	±1.0	
Differential Non-Linearity	12-bit mode	T	DNL	—	±1.0	—	LSB ³
	10-bit mode ^{4, 4}	P		—	±0.25	±0.5	
	8-bit mode ⁴	P		—	±0.15	±0.25	
Integral Non-Linearity	12-bit mode	T	INL	—	±1.0	—	LSB ³
	10-bit mode	T		—	±0.3	±0.5	
	8-bit mode	T		—	±0.15	±0.25	
Zero-scale error ^{5, 5}	12-bit mode	C	E_{ZS}	—	±2.0	—	LSB ³
	10-bit mode	P		—	±0.25	±1.0	
	8-bit mode	P		—	±0.65	±1.0	
Full-scale error ⁶	12-bit mode	T	E_{FS}	—	±2.5	—	LSB ³
	10-bit mode	T		—	±0.5	±1.0	
	8-bit mode	T		—	±0.5	±1.0	
Quantization error	≤12 bit modes	D	E_Q	—	—	±0.5	LSB ³
Input leakage error ⁷	all modes	D	E_{IL}	$I_{in} * R_{AS}$			mV
Temp sensor slope	-40°C– 25°C	D	m	—	3.266	—	mV/°C
	25°C– 125°C			—	3.638	—	
Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.396	—	V

1. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK}=1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization.
3. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
4. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
5. $V_{ADIN} = V_{SSA}$
6. $V_{ADIN} = V_{DDA}$
7. I_{in} = leakage current (refer to DC characteristics)

6.3.2 Analog comparator (ACMP) electricals

Table 13. Comparator electrical specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DDA}	2.7	—	5.5	V
T	Supply current (Operation mode)	I_{DDA}	—	10	20	μA
D	Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DDA}	V
P	Analog input offset voltage	V_{AIO}	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
T	Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
C	Propagation Delay	t_D	—	0.4	1	μs

6.4 Communication interfaces

6.4.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} , unless noted, and 100 pF load on all SPI pins. All timing assumes slew rate control is disabled and high drive strength is enabled for SPI output pins.

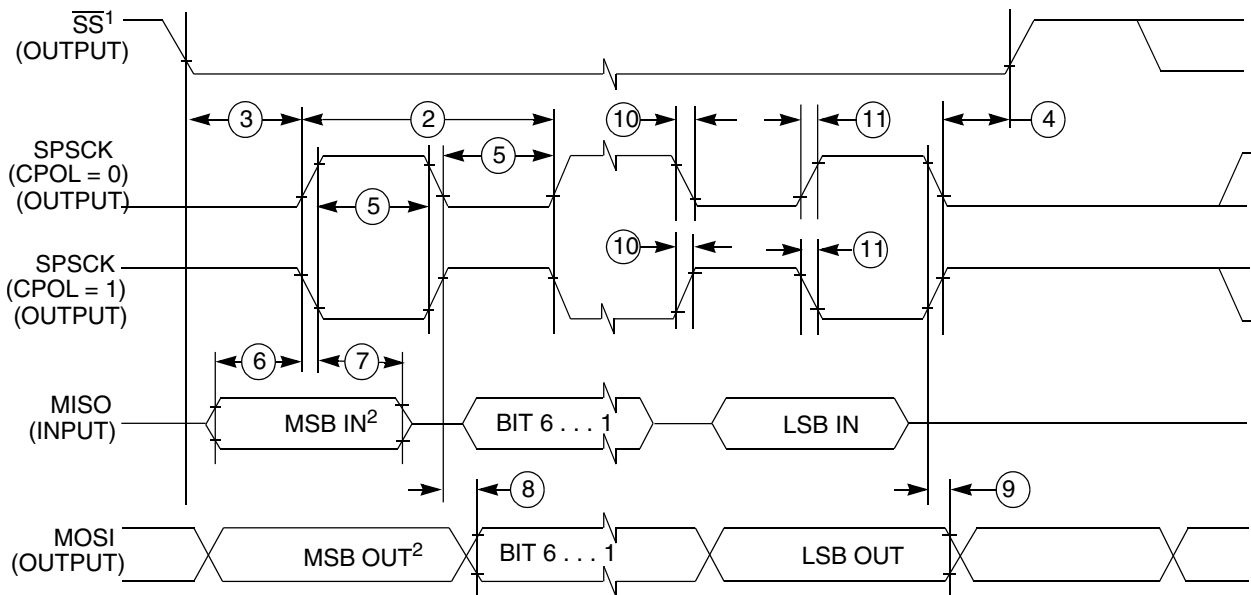
Table 14. SPI master mode timing

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	$f_{Bus}/2048$	$f_{Bus}/2$	Hz	f_{Bus} is the bus clock
2	t_{SPSCK}	SPSCK period	$2 \times t_{Bus}$	$2048 \times t_{Bus}$	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{Bus} - 30$	$1024 \times t_{Bus}$	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	25	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—

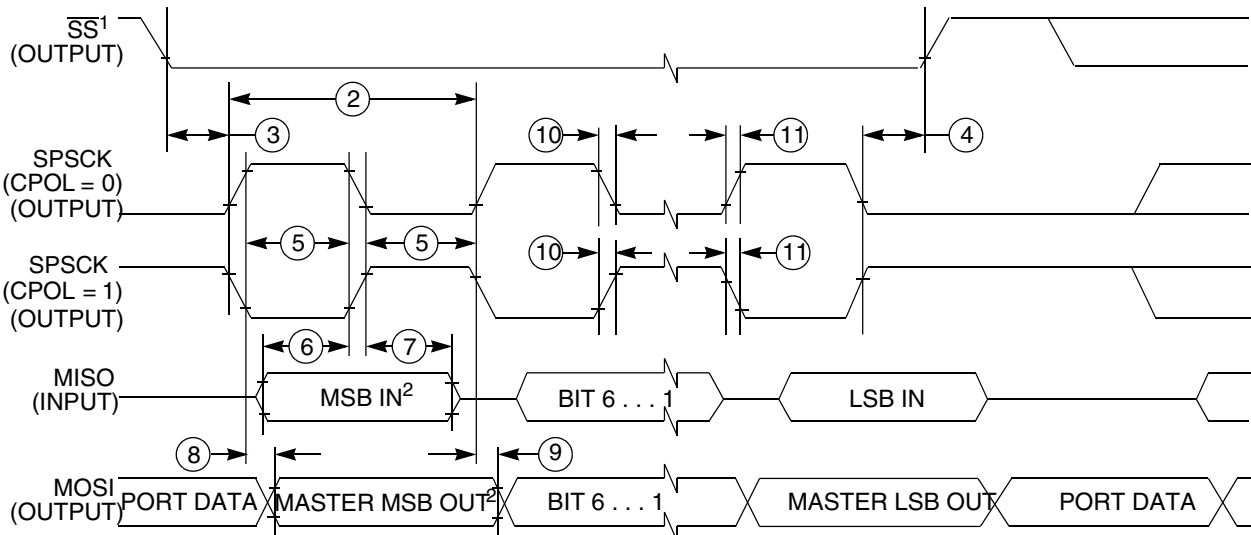
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Table 14. SPI master mode timing (continued)

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
10	t_{RI}	Rise time input	—	$t_{Bus} - 25$	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. SPI master mode timing (CPHA=0)


1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

Table 17. Pin availability by package pin-count (continued)

Pin Number			Lowest Priority <-- --> Highest				
64-LQFP	48-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
20	16	11	PTC3	FTM2CH3	—	ADP11	—
21	17	12	PTC2	FTM2CH2	—	ADP10	—
22	18	—	PTD7	KBI1P7	TXD2	—	—
23	19	—	PTD6	KBI1P6	RXD2	—	—
24	20	—	PTD5	KBI1P5	—	—	—
25	21	13	PTC1	—	FTM2CH1	ADP9	TSI7
26	22	14	PTC0	—	FTM2CH0	ADP8	TSI6
27	—	—	PTF7	—	—	ADP15	—
28	—	—	PTF6	—	—	ADP14	—
29	—	—	PTF5	—	—	ADP13	—
30	—	—	PTF4	—	—	ADP12	—
31	23	15	PTB3	KBI0P7	MOSI0	ADP7	TSI5
32	24	16	PTB2	KBI0P6	SPSCK0	ADP6	TSI4
33	25	17	PTB1	KBI0P5	TXD0	ADP5	TSI3
34	26	18	PTB0	KBI0P4	RXD0	ADP4	TSI2
35	—	—	PTF3	—	—	—	TSI15
36	—	—	PTF2	—	—	—	TSI14
37	27	19	PTA7	FTM2FAULT2	—	ADP3	TSI1
38	28	20	PTA6	FTM2FAULT1	—	ADP2	TSI0
39	29	—	PTE4	—	—	—	—
40	30	—	—	—	—	—	V _{SS}
41	31	—	—	—	—	—	V _{DD}
42	—	—	PTF1	—	—	—	TSI13
43	—	—	PTF0	—	—	—	TSI12
44	32	—	PTD4	KBI1P4	—	—	—
45	33	21	PTD3	KBI1P3	SS1	—	TSI11
46	34	22	PTD2	KBI1P2	MISO1	—	TSI10
47	35	23	PTA3 ^{2, 2}	KBI0P3	TXD0	SCL	—
48	36	24	PTA2 ²	KBI0P2	RXD0	SDA	—
49	37	25	PTA1	KBI0P1	FTM0CH1	ACMP1	ADP1
50	38	26	PTA0	KBI0P0	FTM0CH0	ACMP0	ADP0
51	39	27	PTC7	—	TxD1	—	TSI9
52	40	28	PTC6	—	RxD1	—	TSI8
53	41	—	PTE3	—	SS0	—	—
54	42	—	PTE2	—	MISO0	—	—
55	—	—	PTG3	—	—	—	—
56	—	—	PTG2	—	—	—	—
57	—	—	PTG1	—	—	—	—

Table continues on the next page...

Table 17. Pin availability by package pin-count (continued)

Pin Number			Lowest Priority <-- --> Highest				
64-LQFP	48-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
58	—	—	PTG0	—	—	—	—
59	43	—	PTE1 ¹	—	MOSI0	—	—
60	44	—	PTE0 ¹	—	SPSCK0	TCLK1	—
61	45	29	PTC5	—	FTM1CH1	—	—
62	46	30	PTC4	—	FTM1CH0	RTCO	—
63	47	31	—	—	—	—	RESET
64	48	32	—	—	—	BKGD	MS

1. This is a high current drive pin when operated as output.
2. This is a true open-drain pin when operated as output.

Note

When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

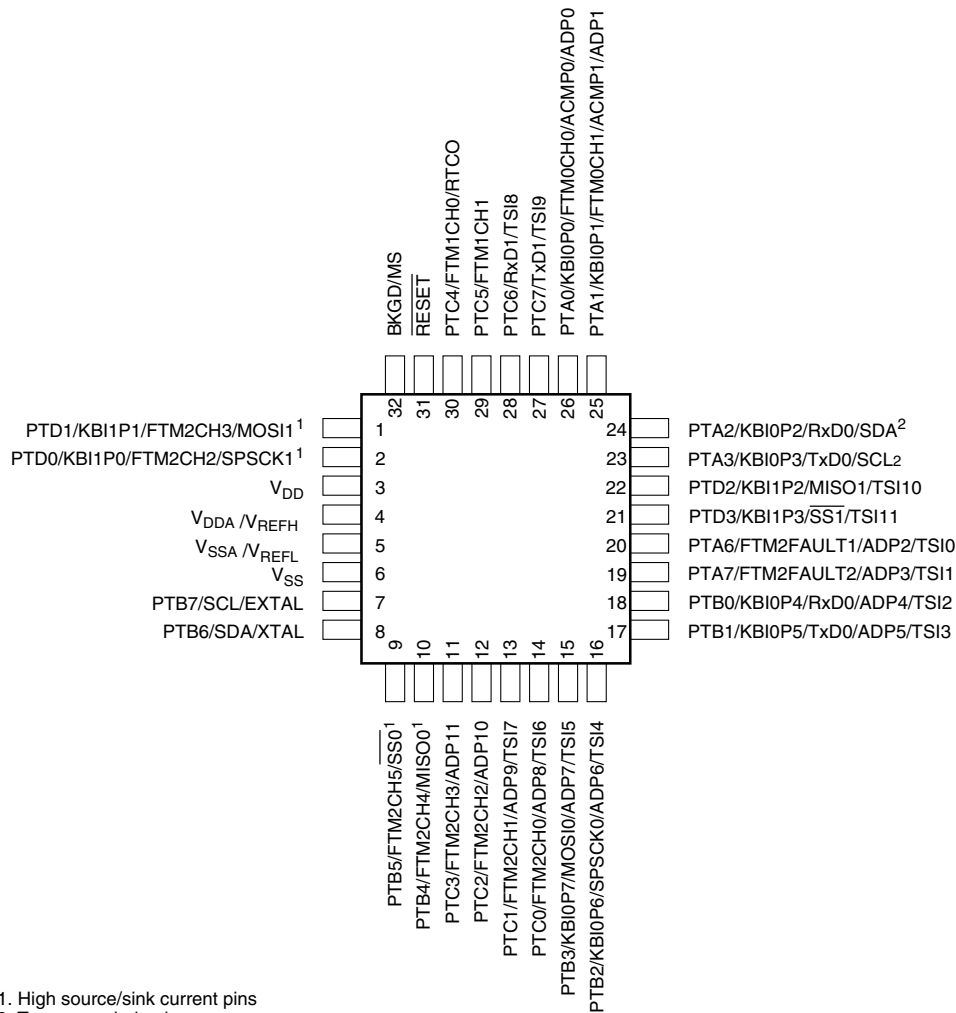


Figure 23. S9S08RN60 32-pin LQFP package

9 Revision history

The following table provides a revision history for this document.

Table 18. Revision history

Rev. No.	Date	Substantial Changes
1	01/2014	Initial Release