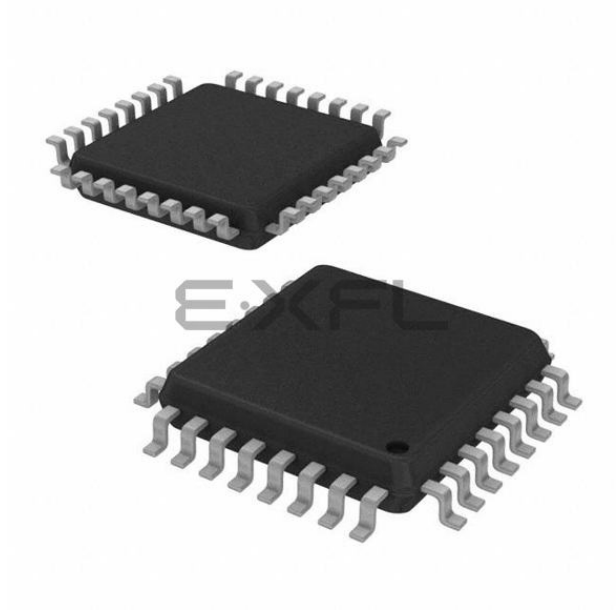

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08rna32w1mlc

- Input/Output
  - Up to 55 GPIOs including one output-only pin
  - Two 8-bit keyboard interrupt modules (KBI)
  - Two true open-drain output pins
  - Eight, ultra-high current sink pins supporting 20 mA source/sink current

- Package options
  - 64-pin LQFP
  - 48-pin LQFP
  - 32-pin LQFP

Table of Contents

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: RN60, RN48 and RN32.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

S 9 S08 RN AA F1 B CC

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
S	Qualification status	• S = fully qualified, general market flow
9	Memory	• 9 = flash based
S08	Core	• S08 = 8-bit CPU
RN	Device family	• RN
AA	Approximate flash size in KB	• 60 = 60 KB • 48 = 48 KB • 32 = 32 KB
F1	Fab and mask set identifier	• W1
B	Temperature range (°C)	• M = –40 to 125

Table continues on the next page...

Field	Description	Values
CC	Package designator	• LH = 64-pin LQFP • LF = 48-pin LQFP • LC = 32-pin LQFP

2.4 Example

This is an example part number:

S9S08RN60W1MLH

3 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 1. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.

Table 2. DC characteristics (continued)

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	50	
V_{IH}	P	Input high voltage	All digital inputs	V_{DD}>4.5V	0.70 × V_{DD}	—	—	V
	C			V_{DD}>2.7V	0.75 × V_{DD}	—	—	
V_{IL}	P	Input low voltage	All digital inputs	V_{DD}>4.5V	—	—	0.30 × V_{DD}	V
	C			V_{DD}>2.7V	—	—	0.35 × V_{DD}	
V_{hys}	C	Input hysteresis	All digital inputs	—	0.06 × V_{DD}	—	—	mV
$\lvert I_{In}\rvert$	P	Input leakage current	All input only pins (per pin)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA
$\lvert I_{OZ}\rvert$	P	Hi-Z (off-state) leakage current	All input/output (per pin)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA
$\lvert I_{OZTOT}\rvert$	C	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	V_{IN} = V_{DD} or V_{SS}	—	—	2	µA
R_{PU}	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	kΩ
R_{PU}[3]	P	Pullup resistors	PTA2 and PTA3 pin	—	30.0	—	60.0	kΩ
I_{IC}	D	DC injection current[4, 5, 6]	Single pin limit	V_{IN} < V_{SS}, V_{IN} > V_{DD}	-0.2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{In}	C	Input capacitance, all pins		—	—	—	7	pF
V_{RAM}	C	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB4, PTB5 support ultra high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}.
5. Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current (V_{In} > V_{DD}) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 3. LVD and POR Specification

Symbol	C	Description	Min	Typ	Max	Unit
V_{POR}	D	POR re-arm voltage[1, 2]	1.5	1.75	2.0	V

Table continues on the next page...

Table 3. LVD and POR Specification (continued)

Symbol	C	Description		Min	Typ	Max	Unit
V_{LVDH}	C	Falling low-voltage detect threshold - high range (LVDV = 1)[3]		4.2	4.3	4.4	V
V_{LVW1H}	C	Falling low-voltage warning threshold - high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V_{LVW2H}	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V_{LVW3H}	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V_{LVW4H}	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V_{HYSH}	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V_{LVDL}	C	Falling low-voltage detect threshold - low range (LVDV = 0)		2.56	2.61	2.66	V
V_{LVDW1L}	C	Falling low-voltage warning threshold - low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V_{LVDW2L}	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V_{LVDW3L}	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V_{LVDW4L}	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V_{HYSDL}	C	Low range low-voltage detect hysteresis		—	40	—	mV
V_{HYSWL}	C	Low range low-voltage warning hysteresis		—	80	—	mV
V_{BG}	P	Buffered bandgap output [4]		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. POR ramp time must be longer than 20us/V to get a stable startup.
3. Rising thresholds are falling threshold + hysteresis.
4. Voltage factory trimmed at V_{DD} = 5.0 V, Temp = 125 °C

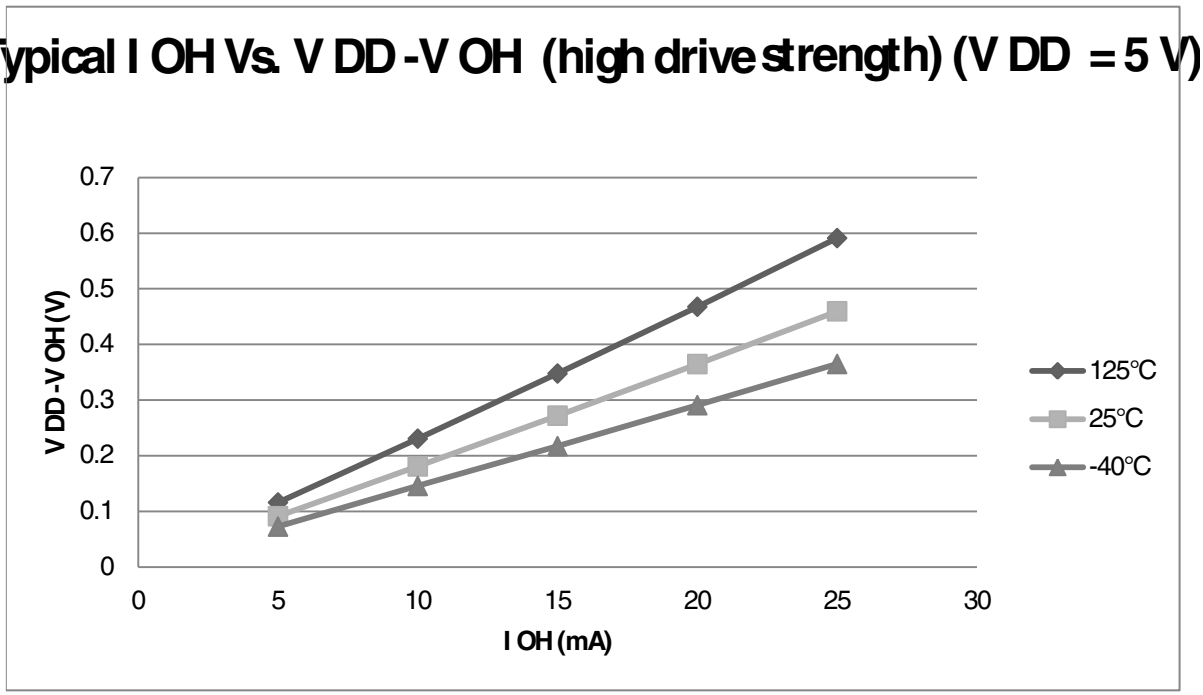


Figure 3. Typical I_{OH} Vs. V_{DD}-V_{OH} (high drive strength) (V_{DD} = 5 V)

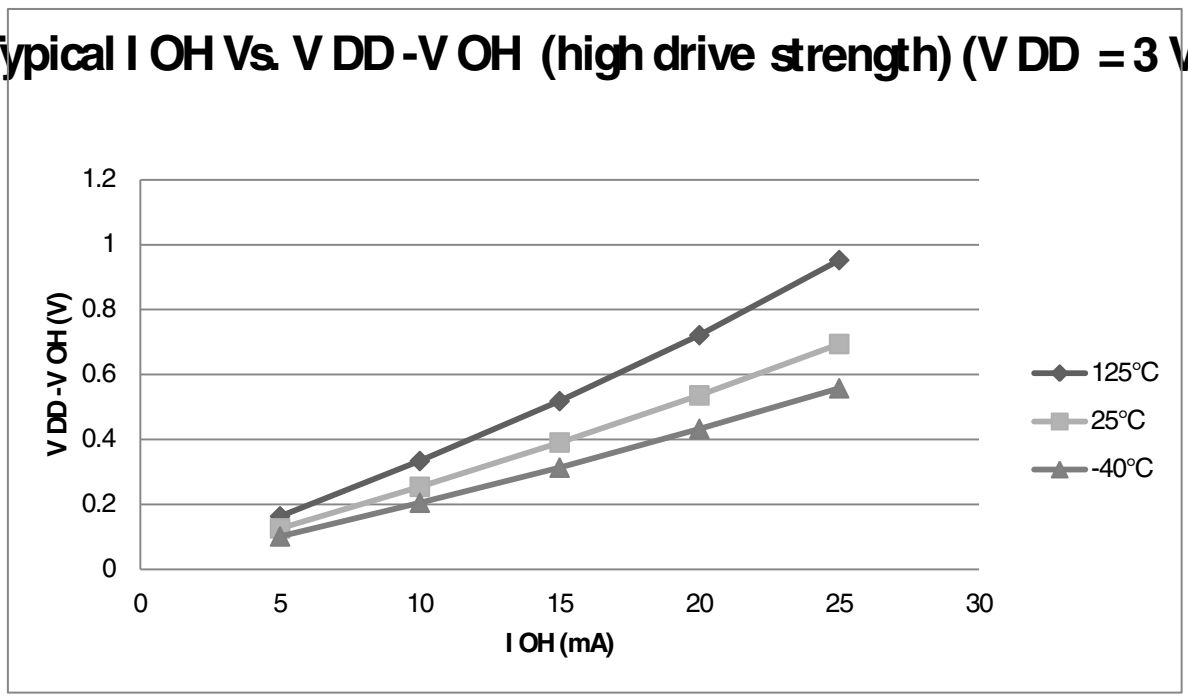


Figure 4. Typical I_{OH} Vs. V_{DD}-V_{OH} (high drive strength) (V_{DD} = 3 V)

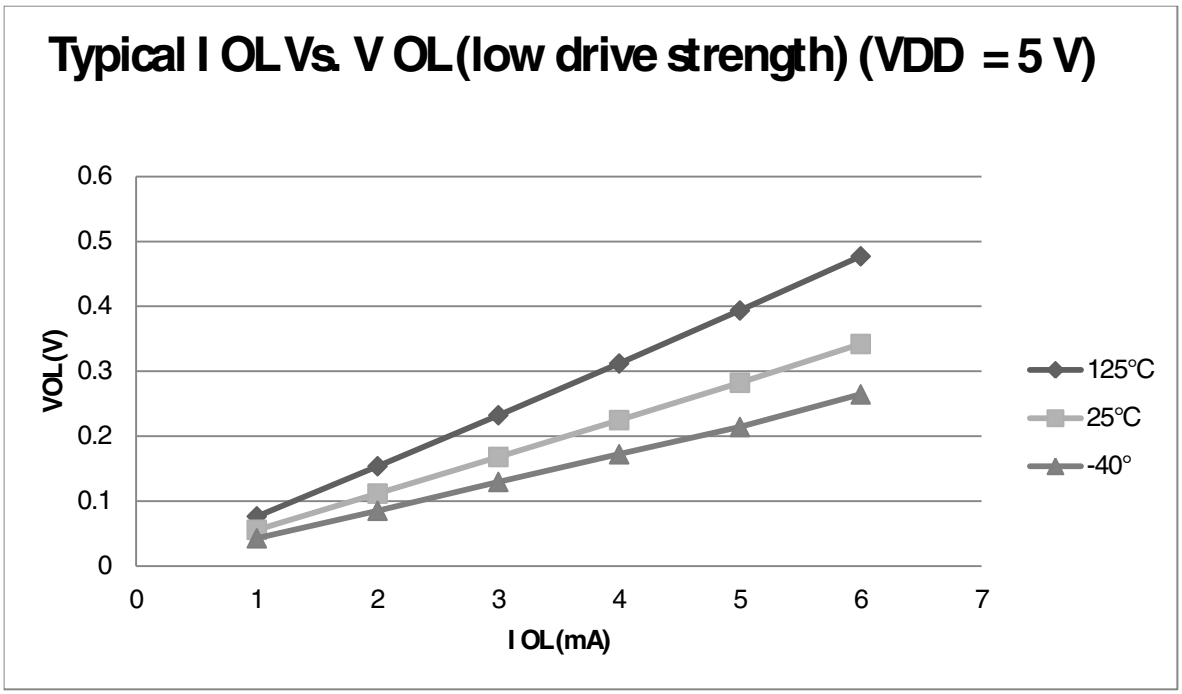


Figure 5. Typical I_{OL} Vs. V_{OL} (standard drive strength) (V_{DD} = 5 V)

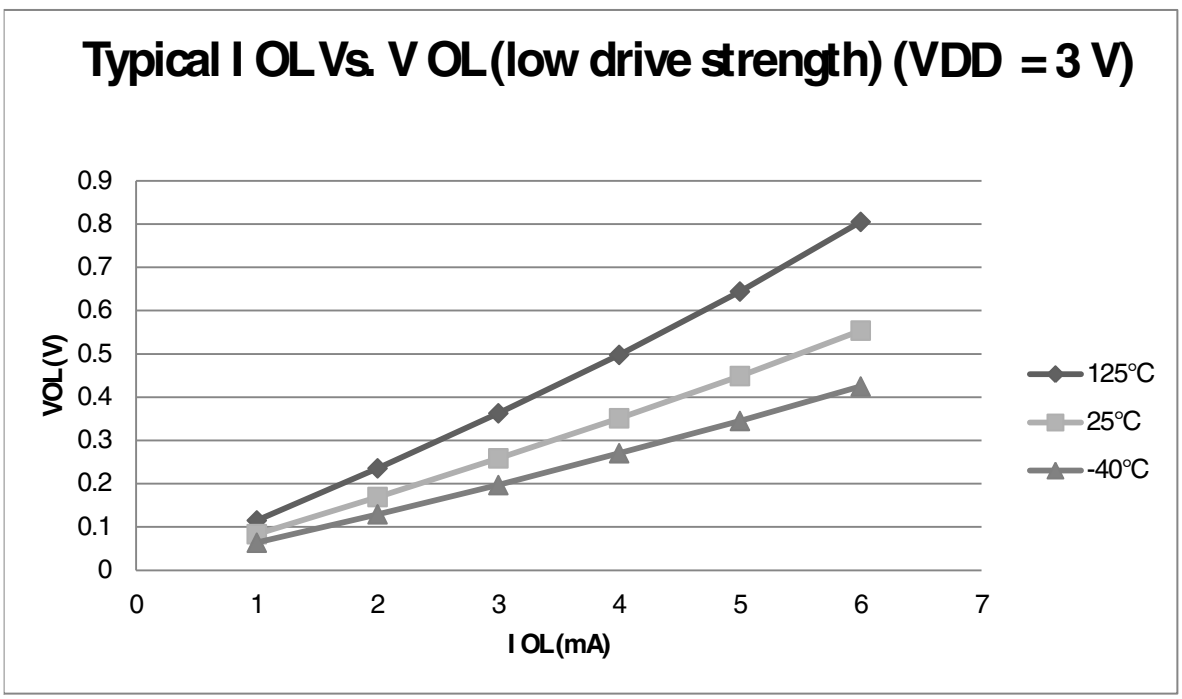


Figure 6. Typical I_{OL} Vs. V_{OL} (standard drive strength) (V_{DD} = 3 V)

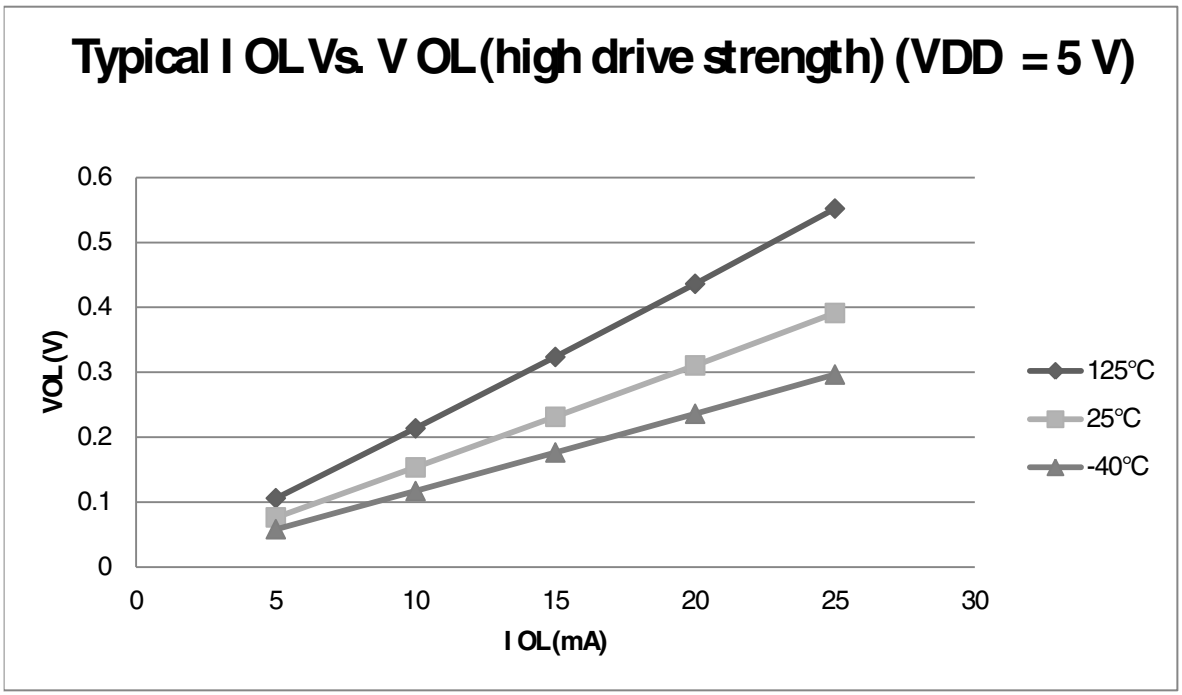


Figure 7. Typical I_{OL} Vs. V_{OL} (high drive strength) (V_{DD} = 5 V)

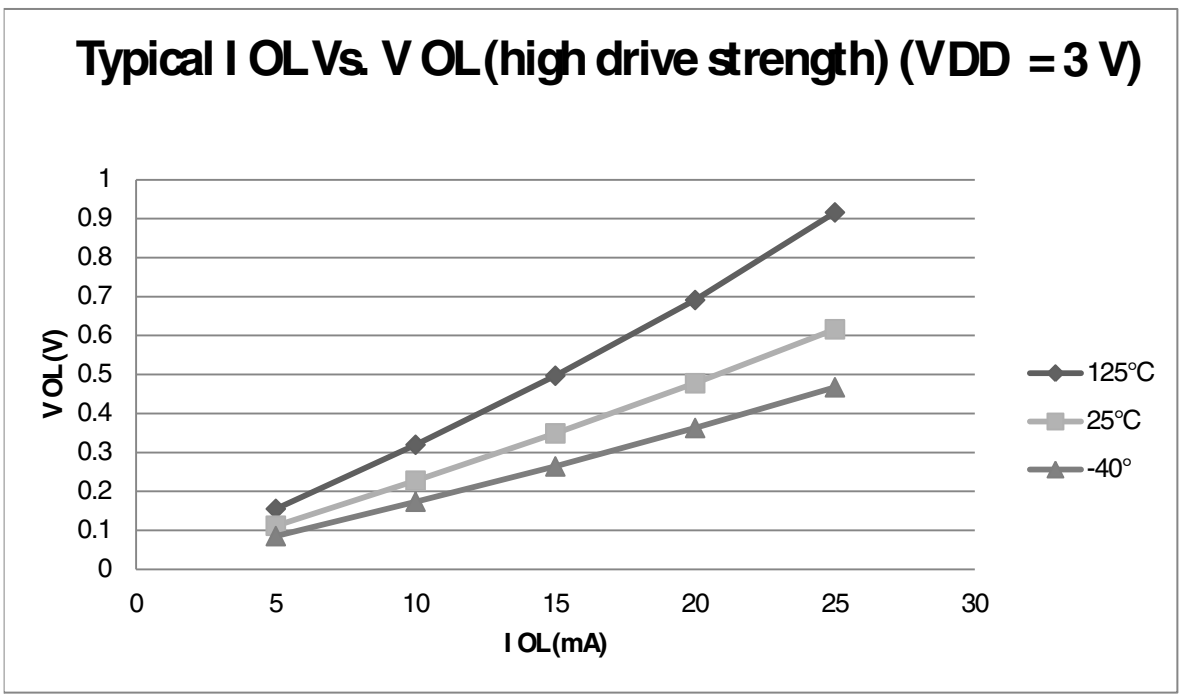


Figure 8. Typical I_{OL} Vs. V_{OL} (high drive strength) (V_{DD} = 3 V)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
1	C	Run supply current FEI mode, all modules on; run from flash	RI_{DD}	20 MHz	5	12.6	—	mA	-40 to 125 °C
	C			10 MHz		7.2	—		
				1 MHz		2.4	—		
	C			20 MHz	3	9.6	—		
	C			10 MHz		6.1	—		
				1 MHz		2.1	—		
2	C	Run supply current FEI mode, all modules off & gated; run from flash	RI_{DD}	20 MHz	5	10.5	—	mA	-40 to 125 °C
	C			10 MHz		6.2	—		
				1 MHz		2.3	—		
	C			20 MHz	3	7.4	—		
	C			10 MHz		5.0	—		
				1 MHz		2.0	—		
3	P	Run supply current FBE mode, all modules on; run from RAM	RI_{DD}	20 MHz	5	12.1	14.8	mA	-40 to 125 °C
	C			10 MHz		6.5	—		
				1 MHz		1.8	—		
	P			20 MHz	3	9.1	11.8		
	C			10 MHz		5.5	—		
				1 MHz		1.5	—		
4	P	Run supply current FBE mode, all modules off & gated; run from RAM	RI_{DD}	20 MHz	5	9.8	12.3	mA	-40 to 125 °C
	C			10 MHz		5.4	—		
				1 MHz		1.6	—		
	P			20 MHz	3	6.9	9.2		
	C			10 MHz		4.4	—		
				1 MHz		1.4	—		
5	C	Wait mode current FEI mode, all modules on	WI_{DD}	20 MHz	5	7.8	—	mA	-40 to 125 °C
	C			10 MHz		4.5	—		
				1 MHz		1.3	—		
	C			20 MHz	3	5.1	—		
				10 MHz		3.5	—		
				1 MHz		1.2	—		
6	C	Stop3 mode supply current no clocks active (except 1 kHz LPO clock)[2, 3]	$S3I_{DD}$	—	5	3.8	—	µA	-40 to 125 °C
	C			—	3	3	—		-40 to 125 °C

Table continues on the next page...

5.2 Switching specifications

5.2.1 Control timing

Table 5. Control timing

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	P	Bus frequency (t_{cyc} = 1/f_{Bus})		f_{Bus}	DC	—	20	MHz
2	P	Internal low power oscillator frequency		f_{LPO}	0.67	1.0	1.25	KHz
3	D	External reset pulse width[2, 2]		t_{extrst}	1.5 × t_{Self_reset}	—	—	ns
4	D	Reset low drive		t_{rstdrv}	34 × t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes		t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes[3]		t_{MSH}	100	—	—	ns
7	D	Keyboard interrupt pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
	D		Synchronous path	t_{IHIL}	1.5 × t_{cyc}	—	—	ns
8	C	Port rise and fall time - Normal drive strength (HDRVE_PTXx = 0) (load = 50 pF)[4, 4]	—	t_{Rise}	—	10.2	—	ns
	C			t_{Fall}	—	9.5	—	ns
	C	Port rise and fall time - Extreme high drive strength (HDRVE_PTXx = 1) (load = 50 pF)[4]	—	t_{Rise}	—	5.4	—	ns
	C			t_{Fall}	—	4.6	—	ns

1. Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
3. To enter BDM mode following a POR, BKGD/MS must be held low during the powerup and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.
4. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range -40 °C to 125 °C.

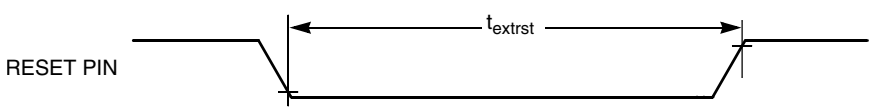


Figure 9. Reset timing

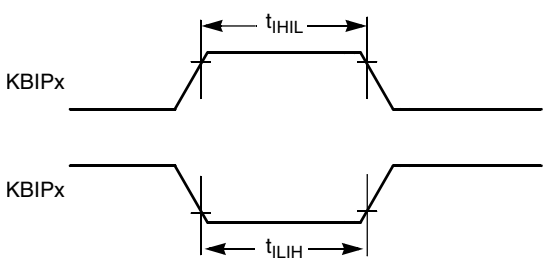


Figure 10. KBIPx timing

Table 8. Thermal characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H -40 to 125	°C
Junction temperature range	T_J	-40 to 135	°C
Thermal resistance single-layer board			
64-pin LQFP	θ_{JA}	71	°C/W
48-pin LQFP	θ_{JA}	81	°C/W
32-pin LQFP	θ_{JA}	86	°C/W
Thermal resistance four-layer board			
64-pin LQFP	θ_{JA}	53	°C/W
48-pin LQFP	θ_{JA}	57	°C/W
32-pin LQFP	θ_{JA}	57	°C/W

The average chip-junction temperature (T_J) in °C can be obtained from:

$T_J = T_A + (P_D \times \theta_{JA})$

Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$P_D = K \div (T_J + 273\ °C)$

Solving the equations above for K gives:

$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2$

where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

6 Peripheral operating requirements and behaviors

6.1 External oscillator (XOSC) and ICS characteristics

Table 9. XOSC and ICS specifications (temperature range = -40 to 125 °C ambient)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator	Low range (RANGE = 0)	f_{lo}	32	—	40	kHz
	C		High range (RANGE = 1) FEE or FBE mode[2, 2]	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), high gain (HGO = 1), FBELP mode	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), low power (HGO = 0), FBELP mode	f_{hi}	4	—	20	MHz
2	D	Load capacitors		C1, C2	See Note[3]			
3	D	Feedback resistor	Low Frequency, Low-Power Mode[4, 4]	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode [4]	R_S	—	—	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode[4]	R_S	—	—	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time Low range = 39.0625 kHz crystal; High range = 20 MHz crystal[5, 5, 6]	Low range, low power	t_{CSTL}	—	1000	—	ms
	C		Low range, high power		—	800	—	ms
	C		High range, low power	t_{CSTH}	—	3	—	ms
	C		High range, high power		—	1.5	—	ms
7	T	Internal reference start-up time		t_{IRST}	—	20	50	µs
8	D	Square wave input clock frequency	FEE or FBE mode[2]	f_{extal}	0.03125	—	5	MHz
	D		FBELP mode		0	—	20	MHz
9	P	Average internal reference frequency - trimmed		f_{int_t}	—	39.0625	—	kHz
10	P	DCO output frequency range - trimmed		f_{dco_t}	16	—	20	MHz

Table continues on the next page...

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

6.3 Analog

6.3.1 ADC characteristics

Table 11. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} (V_{DD}-V_{DDAD})	ΔV_{DDA}	-100	0	+100	mV	
Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})[2]	ΔV_{SSA}	-100	0	+100	mV	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	kΩ	—
Analog source resistance	12-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz	R_{AS}	— —	— —	2 5	kΩ	External to MCU
	10-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz		— —	— —	5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.

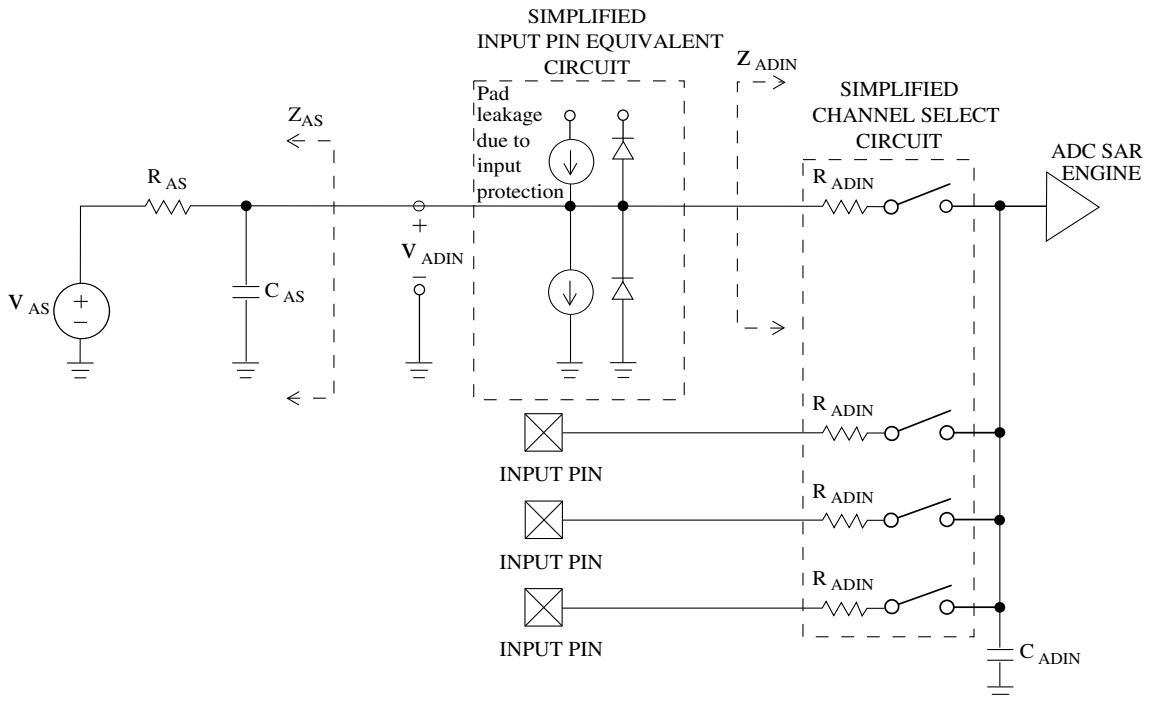


Figure 16. ADC input impedance equivalency diagram

Table 12. 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	µA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	µA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	µA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	990	µA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	µA

Table continues on the next page...

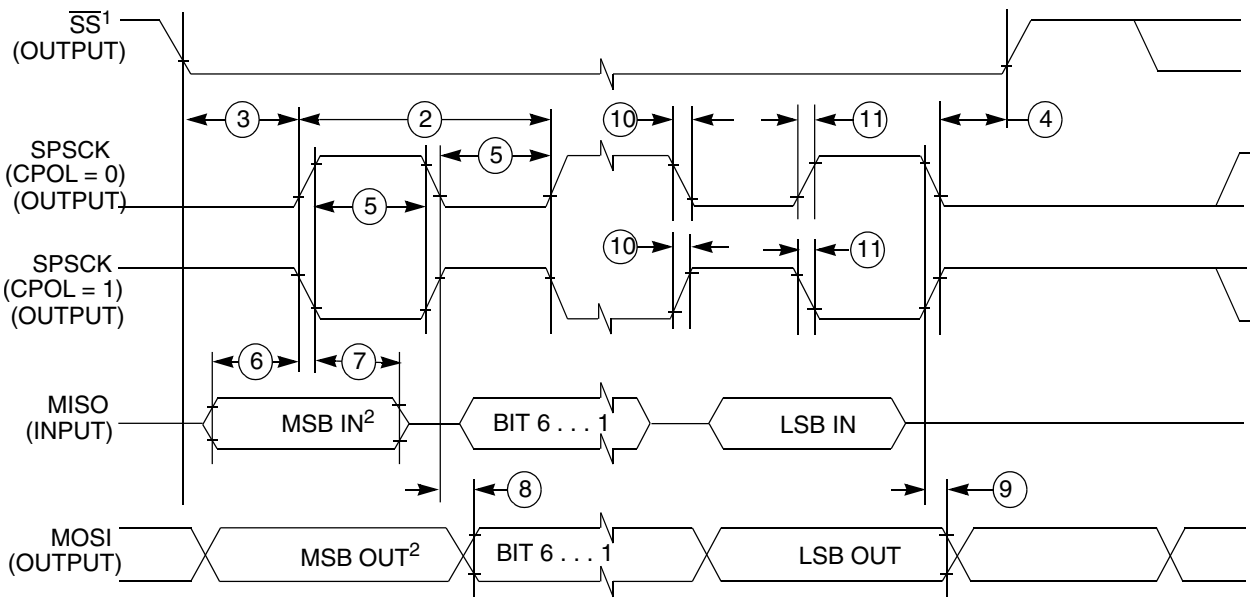
Table 12. 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error[2, 2]	12-bit mode	T	E_{TUE}	—	±5.0	—	LSB[3, 3]
	10-bit mode	P		—	±1.5	±2.0	
	8-bit mode	P		—	±0.7	±1.0	
Differential Non-Linearity	12-bit mode	T	DNL	—	±1.0	—	LSB[3]
	10-bit mode[4, 4]	P		—	±0.25	±0.5	
	8-bit mode[4]	P		—	±0.15	±0.25	
Integral Non-Linearity	12-bit mode	T	INL	—	±1.0	—	LSB[3]
	10-bit mode	T		—	±0.3	±0.5	
	8-bit mode	T		—	±0.15	±0.25	
Zero-scale error[5, 5]	12-bit mode	C	E_{ZS}	—	±2.0	—	LSB[3]
	10-bit mode	P		—	±0.25	±1.0	
	8-bit mode	P		—	±0.65	±1.0	
Full-scale error[6]	12-bit mode	T	E_{FS}	—	±2.5	—	LSB[3]
	10-bit mode	T		—	±0.5	±1.0	
	8-bit mode	T		—	±0.5	±1.0	
Quantization error	≤12 bit modes	D	E_Q	—	—	±0.5	LSB[3]
Input leakage error[7]	all modes	D	E_{IL}	I_{In} * R_{AS}			mV
Temp sensor slope	-40°C– 25°C	D	m	—	3.266	—	mV/°C
	25°C– 125°C			—	3.638	—	
Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.396	—	V

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization.
3. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
4. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
5. V_{ADIN} = V_{SSA}
6. V_{ADIN} = V_{DDA}
7. I_{In} = leakage current (refer to DC characteristics)

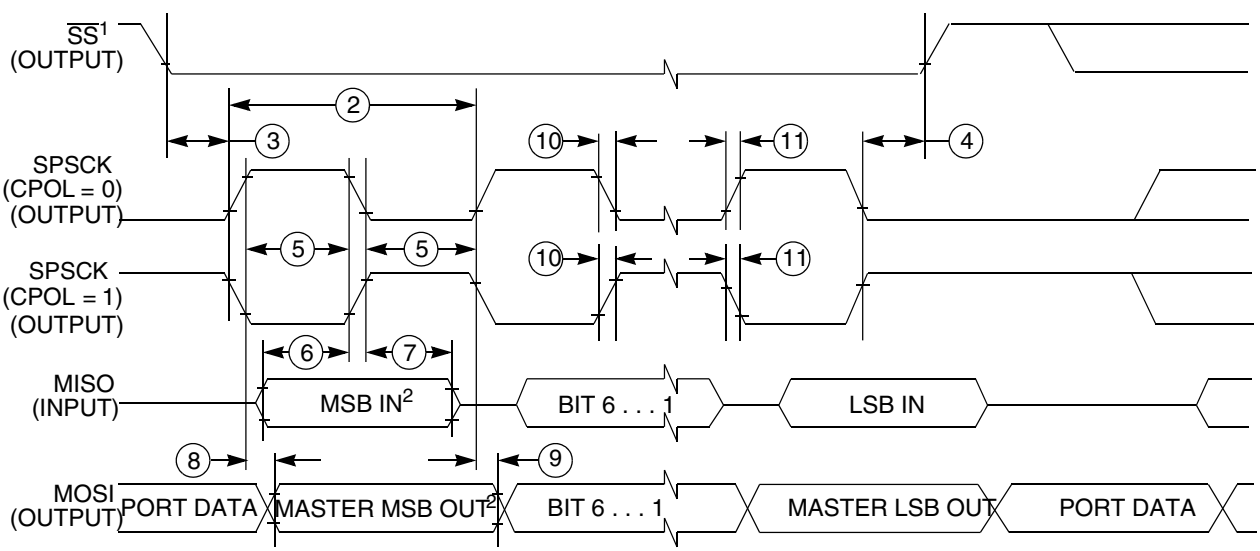
Table 14. SPI master mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
10	t_{RI}	Rise time input	—	t_{Bus} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. SPI master mode timing (CPHA=0)



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin LQFP	98ASH70029A
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W

8 Pinout

8.1 Signal multiplexing and pin assignments

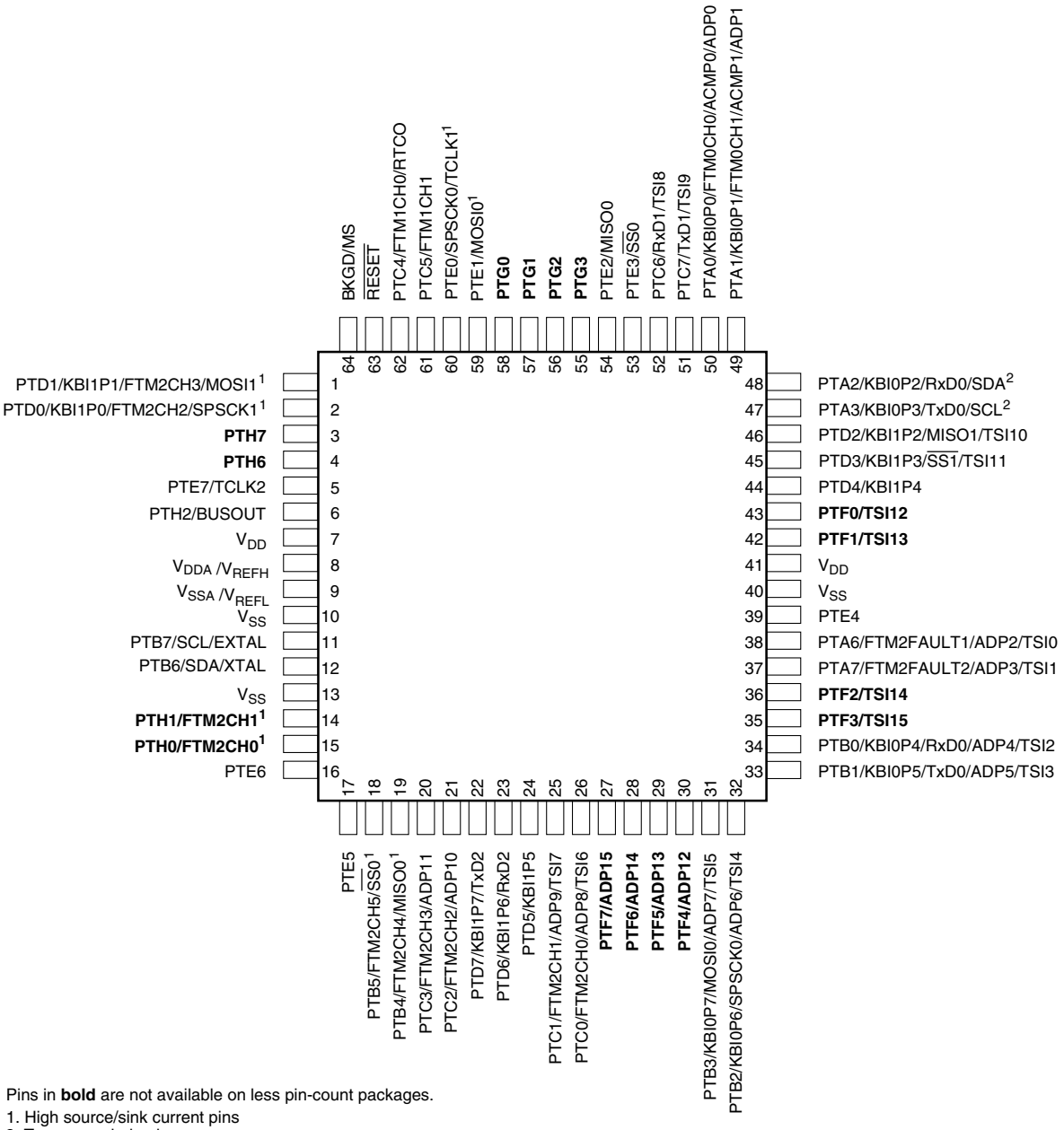
The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 17. Pin availability by package pin-count

Pin Number			Lowest Priority <-- --> Highest				
64-LQFP	48-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	1	PTD1[1, 1]	KBI1P1	FTM2CH3	MOSI1	—
2	2	2	PTD0[1]	KBI1P0	FTM2CH2	SPSCK1	—
3	—	—	PTH7	—	—	—	—
4	—	—	PTH6	—	—	—	—
5	3	—	PTE7	—	TCLK2	—	—
6	4	—	PTH2	—	BUSOUT	—	—
7	5	3	—	—	—	—	V_{DD}
8	6	4	—	—	—	V_{DDA}	V_{REFH}
9	7	5	—	—	—	V_{SSA}	V_{REFL}
10	8	6	—	—	—	—	V_{SS}
11	9	7	PTB7	—	SCL	—	EXTAL
12	10	8	PTB6	—	SDA	—	XTAL
13	11	—	—	—	—	—	V_{SS}
14	—	—	PTH1[1]	—	FTM2CH1	—	—
15	—	—	PTH0[1]	—	FTM2CH0	—	—
16	12	—	PTE6	—	—	—	—
17	13	—	PTE5	—	—	—	—
18	14	9	PTB5[1]	FTM2CH5	$\overline{SS0}$	—	—
19	15	10	PTB4[1]	FTM2CH4	MISO0	—	—

Table continues on the next page...

8.2 Device pin assignment



Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins
2. True open drain pins

Figure 21. S9S08RN60 64-pin LQFP package

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Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

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