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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08rna60w1mlf

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- Input/Output
 - Up to 55 GPIOs including one output-only pin
 - Two 8-bit keyboard interrupt modules (KBI)
 - Two true open-drain output pins
 - Eight, ultra-high current sink pins supporting 20 mA source/sink current
- Package options
 - 64-pin LQFP
 - 48-pin LQFP
 - 32-pin LQFP



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1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: RN60, RN48 and RN32.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

S 9 S08 RN AA F1 B CC

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
s	Qualification status	S = fully qualified, general market flow
9	Memory	9 = flash based
S08	Core	• S08 = 8-bit CPU
RN	Device family	• RN
AA	Approximate flash size in KB	 60 = 60 KB 48 = 48 KB 32 = 32 KB
F1	Fab and mask set identifier	• W1
В	Temperature range (°C)	• M = -40 to 125



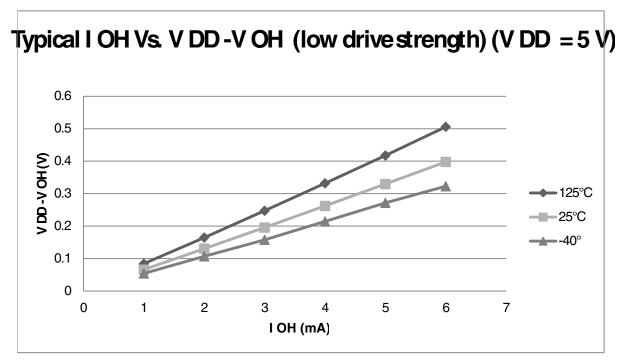


Figure 1. Typical I_{OH} Vs. V_{DD} - V_{OH} (standard drive strength) (V_{DD} = 5 V)

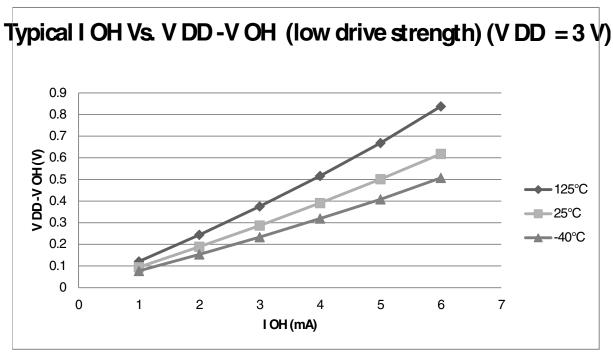


Figure 2. Typical I_{OH} Vs. V_{DD} - V_{OH} (standard drive strength) (V_{DD} = 3 V)



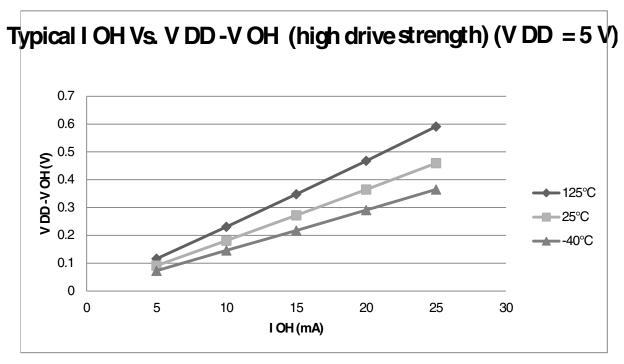


Figure 3. Typical I_{OH} Vs. V_{DD} - V_{OH} (high drive strength) (V_{DD} = 5 V)

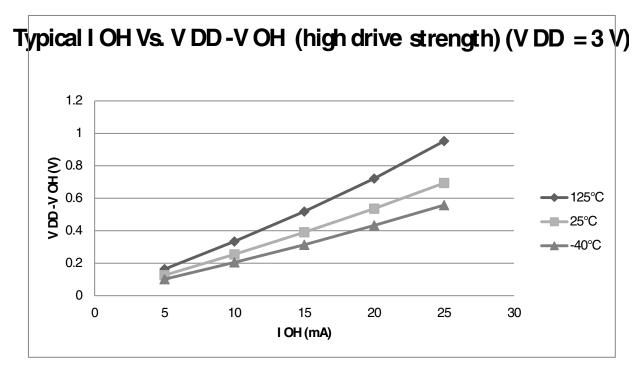


Figure 4. Typical I_{OH} Vs. V_{DD} - V_{OH} (high drive strength) (V_{DD} = 3 V)



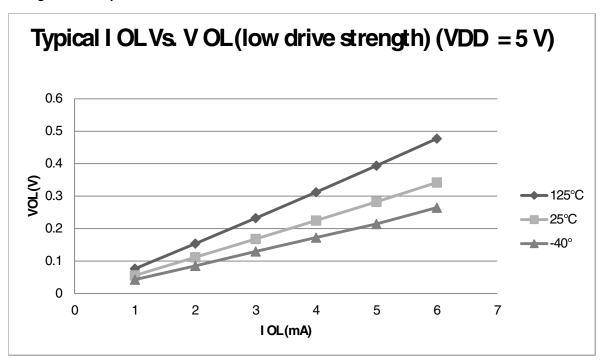


Figure 5. Typical I_{OL} Vs. V_{OL} (standard drive strength) ($V_{DD} = 5 \text{ V}$)

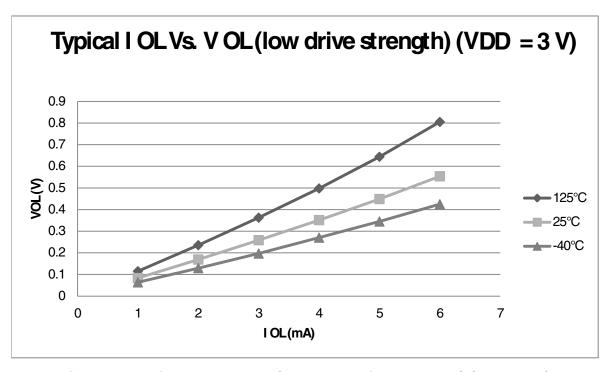


Figure 6. Typical I_{OL} Vs. V_{OL} (standard drive strength) ($V_{DD} = 3 \text{ V}$)



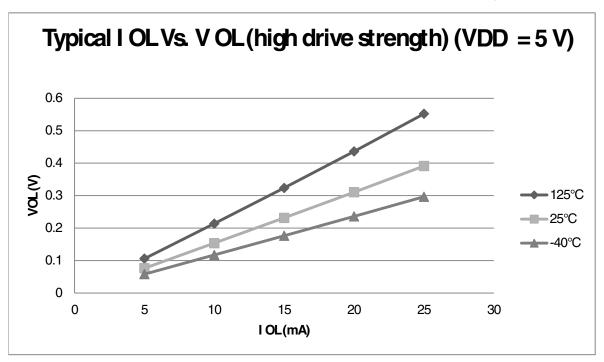


Figure 7. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 5 \text{ V}$)

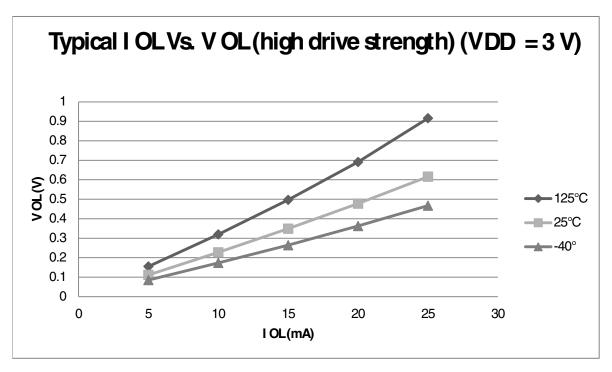


Figure 8. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 3 \text{ V}$)



Table 4.	Supply current	characteristics ((continued)
----------	----------------	-------------------	-------------

Num	С	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp
7	С	ADC adder to stop3	_	_	5	44	_	μΑ	-40 to 125 °C
	С	ADLPC = 1			3	40	_		
		ADLSMP = 1							
		ADCO = 1							
		MODE = 10B							
		ADICLK = 11B							
8	С	TSI adder to stop34	_	_	5	111	_	μΑ	-40 to 125 °C
	С	PS = 010B			3	110	_		
		NSCN =0x0F							
		EXTCHRG = 0							
		REFCHRG = 0							
		DVOLT = 01B							
9	С	LVD adder to stop3 ⁵	_	_	5	130		μΑ	-40 to 125 °C
	С				3	125			

- 1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
- 2. RTC adder cause <1 μA I_{DD} increase typically, RTC clock source is 1 kHz LPO clock.
- 3. ACMP adder cause <1 μ A I_{DD} increase typically.
- 4. The current varies with TSI configuration and capacity of touch electrode. Please refer to TSI electrical specifications.
- 5. LVD is periodically woken up from stop3 by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

5.1.3.1 EMC radiated emissions operating behaviors



5.2 Switching specifications

5.2.1 Control timing

Table 5. Control timing

Num	С	Rating		Symbol	Min	Typical ¹	Max	Unit
1	Р	Bus frequency (t _{cyc} = 1/f _{Bus})	f _{Bus}	DC	_	20	MHz	
2	Р	Internal low power oscillator	frequency	f _{LPO}	0.67	1.0	1.25	KHz
3	D	External reset pulse width ^{2,}	t _{extrst}	1.5 ×	_	_	ns	
					t _{Self_reset}			
4	D	Reset low drive		t _{rstdrv}	$34 \times t_{cyc}$	_	_	ns
5	D	BKGD/MS setup time after debug force reset to enter u	t _{MSSU}	500	_	_	ns	
6	D	BKGD/MS hold time after is debug force reset to enter u		t _{MSH}	100	_	_	ns
7	D	Keyboard interrupt pulse width	Asynchronous path ²	t _{ILIH}	100	_	_	ns
	D		Synchronous path	t _{IHIL}	$1.5 \times t_{cyc}$	_	_	ns
8	С	Port rise and fall time -	_	t _{Rise}	_	10.2	_	ns
	Normal drive strength (HDRVE_PTXx = 0) (load = 50 pF) ^{4, 4}			t _{Fall}	_	9.5	_	ns
	С	Port rise and fall time - —		t _{Rise}	_	5.4	_	ns
	С	Extreme high drive strength (HDRVE_PTXx = 1) (load = 50 pF) ⁴		t _{Fall}	_	4.6	_	ns

- 1. Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.
- 2. This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
- To enter BDM mode following a POR, BKGD/MS must be held low during the powerup and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.
- 4. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range -40 °C to 125 °C.

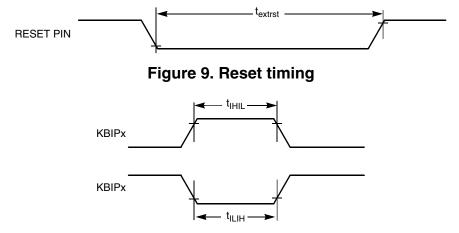


Figure 10. KBIPx timing

S9S08RN60 Series Data Sheet Data Sheet, Rev. 1, 01/2014.



5.2.2 Debug trace timing specifications

Table 6. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
t _{cyc}	Clock period	Frequency	dependent	MHz
t _{wl}	Low pulse width	2	_	ns
t _{wh}	High pulse width	2	_	ns
t _r	Clock and data rise time	_	3	ns
t _f	Clock and data fall time	_	3	ns
t _s	Data setup	3	_	ns
t _h	Data hold	2	_	ns

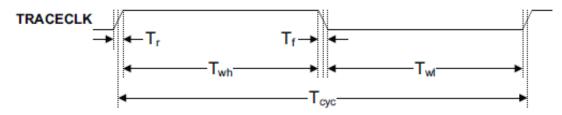


Figure 11. TRACE_CLKOUT specifications

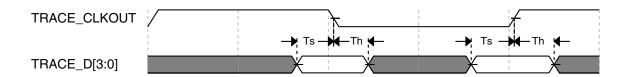


Figure 12. Trace data specifications

5.2.3 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 7. FTM input timing

No.	С	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f _{TCLK}	0	f _{Bus} /4	Hz



6.1 External oscillator (XOSC) and ICS characteristics

Table 9. XOSC and ICS specifications (temperature range = -40 to 125 °C ambient)

Num	С	C	haracteristic	Symbol	Min	Typical ¹	Max	Unit		
1	С	Oscillator	Low range (RANGE = 0)	f _{lo}	32	_	40	kHz		
	С	crystal or resonator	High range (RANGE = 1) FEE or FBE mode ^{2, 2}	f _{hi}	4	_	20	MHz		
	С		High range (RANGE = 1), high gain (HGO = 1), FBELP mode	f _{hi}	4	_	20	MHz		
	С		High range (RANGE = 1), low power (HGO = 0), FBELP mode	f _{hi}	4	_	20	MHz		
2	D	Lo	ad capacitors	C1, C2		See Note ³				
3	D	Feedback resistor	Low Frequency, Low-Power Mode ^{4, 4}	R_{F}	_	_	_	ΜΩ		
			Low Frequency, High-Gain Mode		_	10	_	ΜΩ		
						High Frequency, Low- Power Mode		_	1	_
		High Frequency, High-Gain Mode		_	1	_	ΜΩ			
4	D	Series resistor -	Low-Power Mode ⁴	R _S	_	_	_	kΩ		
		Low Frequency	High-Gain Mode		_	200	_	kΩ		
5	D	Series resistor - High Frequency	Low-Power Mode ⁴	R_S	_	_	_	kΩ		
	D	Series resistor -	4 MHz		_	0	_	kΩ		
	D	High Frequency,	8 MHz		_	0	_	kΩ		
	D	High-Gain Mode	16 MHz		_	0	_	kΩ		
6	С	Crystal start-up	Low range, low power	t _{CSTL}	_	1000	_	ms		
	С	time Low range = 39.0625 kHz	Low range, high power		_	800	_	ms		
	С	crystal; High	High range, low power	t _{CSTH}	_	3	_	ms		
	С	range = 20 MHz crystal ^{5, 5} , ⁶	High range, high power		_	1.5	_	ms		
7	Т	Internal re	eference start-up time	t _{IRST}	_	20	50	μs		
8	D	Square wave	FEE or FBE mode ²	f _{extal}	0.03125	_	5	MHz		
	D	input clock frequency	FBELP mode		0	_	20	MHz		
9	Р	Average inter	nal reference frequency - trimmed	f _{int_t}	_	39.0625	_	kHz		
10	Р	DCO output fr	equency range - trimmed	f _{dco_t}	16	_	20	MHz		



Table 9. XOSC and ICS specifications (temperature range = -40 to 125 °C ambient) (continued)

Num	С	C	Characteristic	Symbol	Min	Typical ¹	Max	Unit
11	Р	Total deviation of DCO output from trimmed	Over full voltage range and temperature range of -40 to 125 °C	Δf_{dco_t}	_	_	±2.0	
	С	frequency ⁵	Over full voltage range and temperature range of -40 to 105 °C				±1.5	%f _{dco}
	С		Over fixed voltage and temperature range of 0 to 70 °C				±1.0	
12	С	FLL a	cquisition time ⁵ , ⁷	t _{Acquire}	_	_	2	ms
13	С		Long term jitter of DCO output clock (averaged over 2 ms interval) ⁸		_	0.02	0.2	%f _{dco}

- 1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
- 2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
- 3. See crystal or resonator manufacturer's recommendation.
- Load capacitors (C₁,C₂), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
- 5. This parameter is characterized and not tested on each device.
- 6. Proper PC board layout procedures must be followed to achieve specifications.
- 7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
- 8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

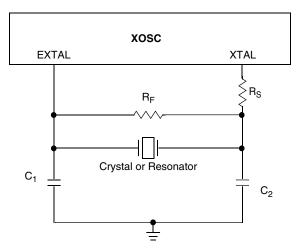


Figure 15. Typical crystal or resonator circuit



Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

6.3 Analog

6.3.1 ADC characteristics

Table 11. 5 V 12-bit ADC operating conditions

Characteri stic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
Supply	Absolute	V _{DDA}	2.7	_	5.5	V	_
voltage	Delta to V _{DD} (V _{DD} -V _{DDAD})	ΔV_{DDA}	-100	0	+100	mV	
Ground voltage	Delta to V _{SS} (V _{SS} -V _{SSA}) ²	ΔV_{SSA}	-100	0	+100	mV	
Input voltage		V _{ADIN}	V _{REFL}	_	V _{REFH}	V	
Input capacitance		C _{ADIN}	_	4.5	5.5	pF	
Input resistance		R _{ADIN}	_	3	5	kΩ	_
Analog source	12-bit mode • f _{ADCK} > 4 MHz	R _{AS}	_	_	2	kΩ	External to MCU
resistance	• f _{ADCK} < 4 MHz		_	_	5		
	10-bit modef_{ADCK} > 4 MHz		_	_	5		
	• f _{ADCK} < 4 MHz		_	_	10		
	8-bit mode	1	_	_	10	1	
	(all valid f _{ADCK})						
ADC	High speed (ADLPC=0)	f _{ADCK}	0.4	_	8.0	MHz	_
conversion clock frequency	Low power (ADLPC=1)		0.4	_	4.0		

^{1.} Typical values assume $V_{DDA} = 5.0 \text{ V}$, Temp = 25°C, $f_{ADCK} = 1.0 \text{ MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.

^{2.} DC potential difference.



reripheral operating requirements and behaviors

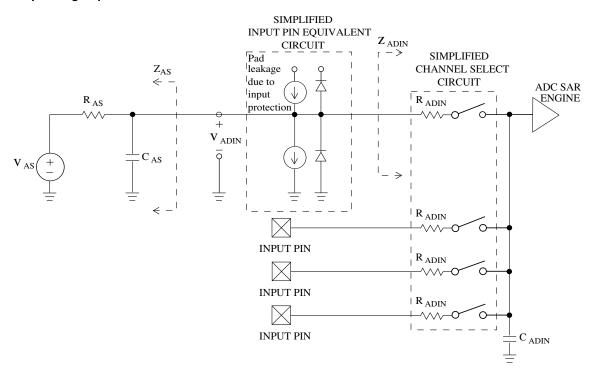


Figure 16. ADC input impedance equivalency diagram

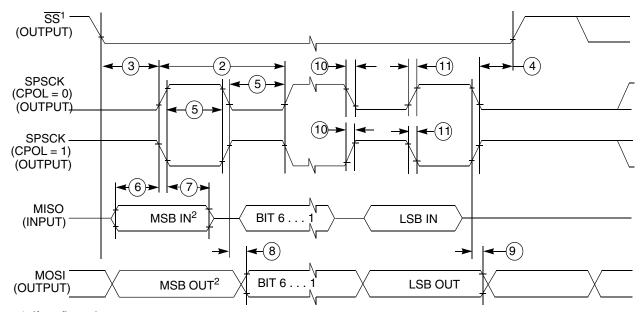
Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	С	Symb	Min	Typ ¹	Max	Unit
Supply current		Т	I _{DDA}	_	133	_	μA
ADLPC = 1							
ADLSMP = 1							
ADCO = 1							
Supply current		Т	I _{DDA}	_	218	_	μA
ADLPC = 1							
ADLSMP = 0							
ADCO = 1							
Supply current		Т	I _{DDA}	_	327	_	μA
ADLPC = 0							
ADLSMP = 1							
ADCO = 1							
Supply current		Т	I _{DDAD}	_	582	990	μA
ADLPC = 0							
ADLSMP = 0							
ADCO = 1							
Supply current	Stop, reset, module off	Т	I _{DDA}	_	0.011	1	μА



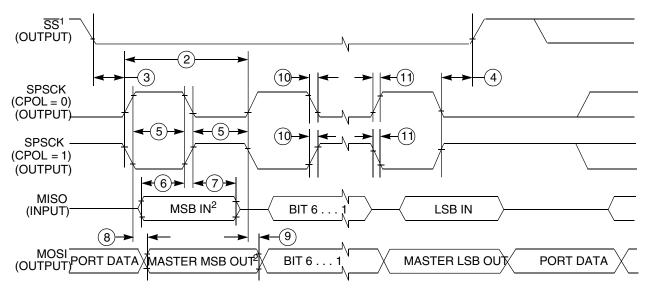
Table 14.	SPI master	mode timing	(continued)
I UDIC IT.	OI I IIIGGIGI	mode uning	(OOIILIII aca)

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
10	t _{RI}	Rise time input	_	t _{Bus} - 25	ns	_
	t _{FI}	Fall time input				
11	t _{RO}	Rise time output	_	25	ns	_
	t _{FO}	Fall time output				



- 1. If configured as an output.
- 2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. SPI master mode timing (CPHA=0)



- 1.If configured as output
- 2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

S9S08RN60 Series Data Sheet Data Sheet, Rev. 1, 01/2014.



reripheral operating requirements and behaviors

Table 15. SPI slave mode timing

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	f _{op}	Frequency of operation	0	f _{Bus} /4	Hz	f _{Bus} is the bus clock as defined in .
2	t _{SPSCK}	SPSCK period	4 x t _{Bus}	_	ns	$t_{Bus} = 1/f_{Bus}$
3	t _{Lead}	Enable lead time	1	_	t _{Bus}	_
4	t _{Lag}	Enable lag time	1	_	t _{Bus}	_
5	t _{WSPSCK}	Clock (SPSCK) high or low time	t _{Bus} - 30	_	ns	_
6	t _{SU}	Data setup time (inputs)	15	_	ns	_
7	t _{HI}	Data hold time (inputs)	25	_	ns	_
8	t _a	Slave access time	_	t _{Bus}	ns	Time to data active from high-impedance state
9	t _{dis}	Slave MISO disable time	_	t _{Bus}	ns	Hold time to high- impedance state
10	t _v	Data valid (after SPSCK edge)	_	25	ns	_
11	t _{HO}	Data hold time (outputs)	0	_	ns	_
12	t _{RI}	Rise time input	_	t _{Bus} - 25	ns	_
	t _{Fl}	Fall time input				
13	t _{RO}	Rise time output	_	25	ns	_
	t _{FO}	Fall time output				

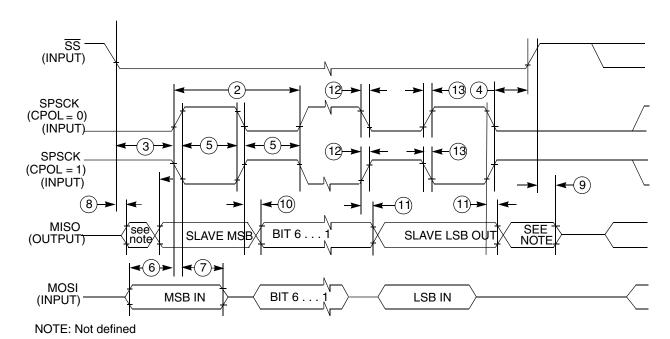


Figure 19. SPI slave mode timing (CPHA = 0)



Table 17. Pin availability by package pin-count (continued)

Pin Number			Lowest Priority <> Highest					
64-LQFP	48-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4	
20	16	11	PTC3	FTM2CH3	_	ADP11	_	
21	17	12	PTC2	FTM2CH2	_	ADP10	_	
22	18	_	PTD7	KBI1P7	TXD2	_	_	
23	19	_	PTD6	KBI1P6	RXD2	_	_	
24	20	_	PTD5	KBI1P5	_	_	_	
25	21	13	PTC1	_	FTM2CH1	ADP9	TSI7	
26	22	14	PTC0	_	FTM2CH0	ADP8	TSI6	
27	_	_	PTF7	_	_	ADP15	_	
28	_	_	PTF6	_	_	ADP14	_	
29	_	_	PTF5	_	_	ADP13	_	
30	_	_	PTF4	_	_	ADP12	_	
31	23	15	PTB3	KBI0P7	MOSI0	ADP7	TSI5	
32	24	16	PTB2	KBI0P6	SPSCK0	ADP6	TSI4	
33	25	17	PTB1	KBI0P5	TXD0	ADP5	TSI3	
34	26	18	PTB0	KBI0P4	RXD0	ADP4	TSI2	
35	_	_	PTF3	_	_	_	TSI15	
36	_	_	PTF2	_	_	_	TSI14	
37	27	19	PTA7	FTM2FAULT2	_	ADP3	TSI1	
38	28	20	PTA6	FTM2FAULT1	_	ADP2	TSI0	
39	29	_	PTE4	_	_	_	_	
40	30	_	_	_	_	_	V _{SS}	
41	31	_		_	_	_	V_{DD}	
42	_	_	PTF1	_	_	_	TSI13	
43	_	_	PTF0	_	_	_	TSI12	
44	32	_	PTD4	KBI1P4	_	_	_	
45	33	21	PTD3	KBI1P3	SS1	_	TSI11	
46	34	22	PTD2	KBI1P2	MISO1	_	TSI10	
47	35	23	PTA3 ^{2, 2}	KBI0P3	TXD0	SCL	_	
48	36	24	PTA2 ²	KBI0P2	RXD0	SDA	_	
49	37	25	PTA1	KBI0P1	FTM0CH1	ACMP1	ADP1	
50	38	26	PTA0	KBI0P0	FTM0CH0	ACMP0	ADP0	
51	39	27	PTC7	_	TxD1	_	TSI9	
52	40	28	PTC6	_	RxD1	_	TSI8	
53	41	_	PTE3	_	SS0	_	_	
54	42	_	PTE2	_	MISO0	_	_	
55	_	_	PTG3	_	_	_	_	
56	_	_	PTG2	_	_	_	_	
57	_	_	PTG1		_	_	_	



rmoul

Table 17. Pin availability by package pin-count (continued)

	Pin Number		Lowest Priority <> Highest				
64-LQFP	48-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
58	_	_	PTG0	_	_	_	_
59	43	_	PTE1 ¹	_	MOSI0	_	_
60	44	_	PTE0 ¹	_	SPSCK0	TCLK1	_
61	45	29	PTC5	_	FTM1CH1	_	_
62	46	30	PTC4	_	FTM1CH0	RTCO	_
63	47	31	_	_	_	_	RESET
64	48	32	_	_	_	BKGD	MS

- 1. This is a high current drive pin when operated as output.
- 2. This is a true open-drain pin when operated as output.

Note

When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

rmout

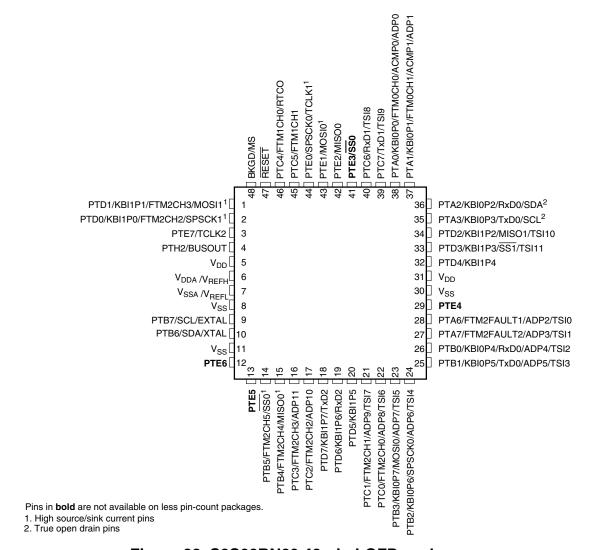


Figure 22. S9S08RN60 48-pin LQFP package



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