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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gpf-g

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1. Product Lineup

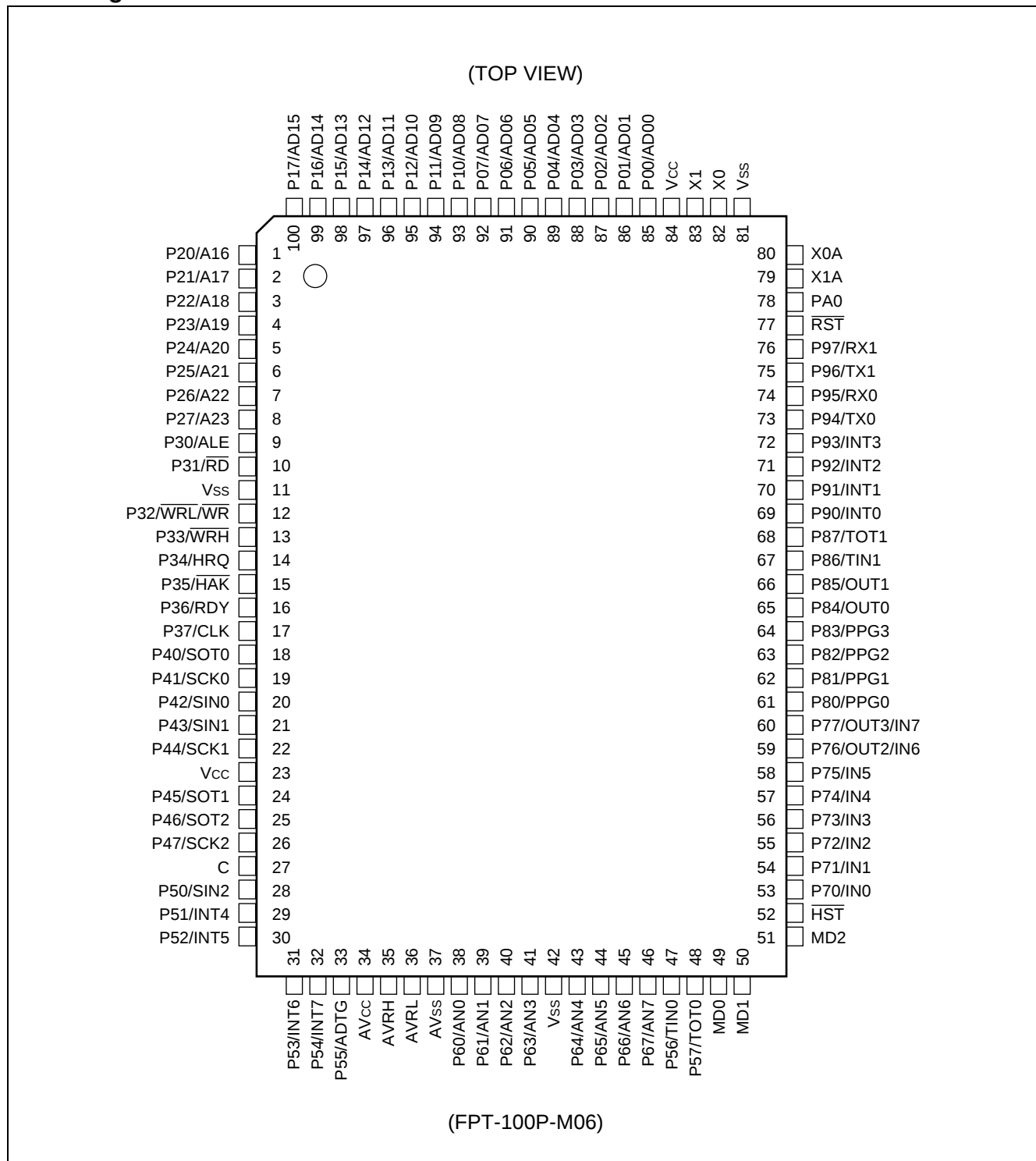
Features	MB90F543G (S) /F548G (S) MB90F549G (S) /F546G (S) MB90F548GL(S)	MB90543G (S) MB90547G (S) MB90548G (S) MB90549G (S)	MB90V540G
CPU	F ² MC-16LX CPU		
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, 1/2 when PLL stop) Minimum instruction execution time : 62.5 ns (machine clock 16MHz, 4MHz osc. four times multiplied by PLL)		
ROM	Flash memory MB90F543G(S)/F548G(S) / F548GL(S) : 128 Kbytes MB90F549G(S)/F546G(S) : 256 Kbytes	MASK ROM : MB90547G(S): 64 Kbytes MB90543G(S)/548G(S): 128 Kbytes MB90549G(S): 256 Kbytes	External
RAM	MB90F548G(S)/F548GL(S): 4 Kbytes MB90F543G (S) /F549G(S) : 6 Kbytes MB90F546G(S) : 8 Kbytes	MB90547G(S): 2 Kbytes MB90548G(S): 4 Kbytes MB90543G(S)/549G(S): 6 Kbytes	8 Kbytes
Clocks	MB90F543G/F548G/F549G/F546G/ F548GL : Two clocks system MB90F543GS/F548GS/F549GS/ F546GS/F548GLS : One clock system	MB90543G/547G/548G/549G : Two clocks system MB90543GS/547GS/548GS/ 549GS : One clock system	Two clocks system*1
Operating voltage range	*3		
Temperature range	−40 °C to 105 °C		
Package	QFP100, LQFP100		PGA-256
Emulator-specify power supply*2	—		None
UART0	Full duplex double buffer Support asynchronous/synchronous (with start/stop bit) transfer Baud rate : 4808/5208/9615/10417/19230/38460/62500/500000 bps (asynchronous) 500 K/1 M/2 Mbps (synchronous) at System clock = 16 MHz		
UART1 (SCI)	Full duplex double buffer Asynchronous (start-stop synchronized) and CLK-synchronous communication Baud rate : 1202/2404/4808/9615/19230/31250/38460/62500 bps (asynchronous) 62.5 K/125 K/250 K/500 K/1 M/2 Mbps (synchronous) at 6, 8, 10, 12, 16 MHz		
Serial I/O	Transfer can be started from MSB or LSB Supports internal clock synchronized transfer and external clock synchronized transfer Supports positive-edge and negative-edge clock synchronization Baud rate : 31.25 K/62.5 K/125 K/500 K/1 Mbps at System clock = 16 MHz		
A/D Converter	10-bit or 8-bit resolution 8 input channels Conversion time : 26.3 μs (per one channel)		

(Continued)

Features	MB90F543G (S) /F548G (S) MB90F549G (S) /F546G (S) MB90F548GL(S)	MB90543G (S) MB90547G (S) MB90548G (S) MB90549G (S)	MB90V540G
16-bit Reload Timer (2 channels)	Operation clock frequency : $f_{sys}/2^1$, $f_{sys}/2^3$, $f_{sys}/2^5$ (f_{sys} = System clock frequency) Supports External Event Count function Signals an interrupt when overflow		
16-bit Free-run Timer	Supports Timer Clear when a match with Output Compare (Channel 0) Operation clock freq. : $f_{sys}/2^2$, $f_{sys}/2^4$, $f_{sys}/2^6$, $f_{sys}/2^8$ (f_{sys} = System clock freq.)		
16-bit Output Compare (4 channels)	Signals an interrupt when a match with 16-bit Free-run Timer Four 16-bit compare registers A pair of compare registers can be used to generate an output signal		
16-bit Input Capture (8 channels)	Rising edge, falling edge or rising & falling edge sensitive Four 16-bit Capture registers Signals an interrupt upon external event		
8/16-bit Programmable Pulse Generator (4 channels)	Supports 8-bit and 16-bit operation modes Eight 8-bit reload counters Eight 8-bit reload registers for L pulse width Eight 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter 4 output pins Operation clock freq. : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$ or $128 \mu s @ f_{osc} = 4 \text{ MHz}$ (f_{sys} = System clock frequency, f_{osc} = Oscillation clock frequency)		
CAN Interface MB90540G series : 2 channels MB90545G series : 1 channel	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's supports multiple messages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps		
32 kHz Sub-clock	Sub-clock for low power operation		
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive		
External bus interface	External access using the selectable 8-bit or 16-bit bus is enabled (external bus mode.)		
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs and schmitt trigger inputs Bit-wise programmable as input/output or peripheral signal Sub-clock for 32 kHz Sub clock low power operation		
Flash Memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Erase-Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block Block protection by externally programmed voltage		

*1 : If the one clock system is used, equip X0A and X1A with clocks from the tool side.

2. Pin Assignment



3. Pin Description

Pin No.		Pin name	Circuit type	Function
LQFP ^{*2}	QFP ^{*1}			
80 81	82 83	X0 X1	A (Oscillation)	High speed crystal oscillator input pins
78	80	X0A	A (Oscillation)	Low speed crystal oscillator input pins. For the one clock system parts, perform external pull-down processing.
77	79	X1A		Low speed crystal oscillator input pins. For the one clock system parts, leave it open.
75	77	$\overline{\text{RST}}$	B	External reset request input pin
50	52	$\overline{\text{HST}}$	C	Hardware standby input pin
83 to 90	85 to 92	P00 to P07	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
91 to 98	93 to 100	P10 to P17	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		AD08 to AD15		I/O pins for 8 higher bits of the external address/data bus. This function is enabled when the external bus is enabled.
99 to 6	1 to 8	P20 to P27	I	General I/O port with programmable pullup. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to "1".
		A16 to A23		8-bit I/O pins for A16 to A23 at the external address/data bus. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to "0".
7	9	P30	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
8	10	P31	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		$\overline{\text{RD}}$		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.
10	12	P32	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the $\overline{\text{WR}}/\overline{\text{WRL}}$ pin output is disabled.
		$\overline{\text{WRL}}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{\text{WR}}/\overline{\text{WRL}}$ pin output are enabled. $\overline{\text{WRL}}$ is write-strobe output pin for the lower 8 bits of the data bus in 16-bit access.
		$\overline{\text{WR}}$		$\overline{\text{WR}}$ is write-strobe output pin for the 8 bits of the data bus in 8-bit access.

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Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
72	74	P95	D	General I/O port. This function is always enabled.
		RX0		RX input pin for CAN0 Interface. When the CAN function is used, output from the other functions must be stopped.
73	75	P96	D	General I/O port. This function is enabled when CAN1 disables the output.
		TX1		TX output pin for CAN1. This function is enabled when CAN1 enables the output (only MB90540G series) .
74	76	P97	D	General I/O port. This function is always enabled.
		RX1		RX input pin for CAN1 Interface. When the CAN function is used, output from the other functions must be stopped (only MB90540G series) .
76	78	PA0	D	General I/O port. This function is always enabled.
32	34	AV _{CC}	Power supply	Power supply pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AV _{CC} is applied to V _{CC} .
35	37	AV _{SS}	Power supply	Power supply pin for the A/D Converter.
33	35	AVRH	Power supply	External reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV _{CC} .
34	36	AVRL	Power supply	External reference voltage input pin for the A/D Converter.
47, 48	49, 50	MD0, MD1	C	Input pins for specifying the operating mode. The pins must be directly connected to V _{CC} or V _{SS} .
49	51	MD2	F	Input pin for specifying the operating mode. The pin must be directly connected to V _{CC} or V _{SS} .
25	27	C	—	Power supply stabilization capacitor pin. It should be connected externally to an 0.1 μF ceramic capacitor.
21, 82	23, 84	V _{CC}	Power supply	Input pin for power supply (5.0 V) .
9, 40, 79	11, 42, 81	V _{SS}	Power supply	Input pin for power supply (0.0 V) .

*1 : FPT-100P-M06

*2 : FPT-100P-M20

5. Handling Devices

(1) Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} .
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, care must also be taken in not allowing the analog power-supply voltage (AV_{CC} , $AVRH$) to exceed the digital power-supply voltage.

(2) Handling unused pins

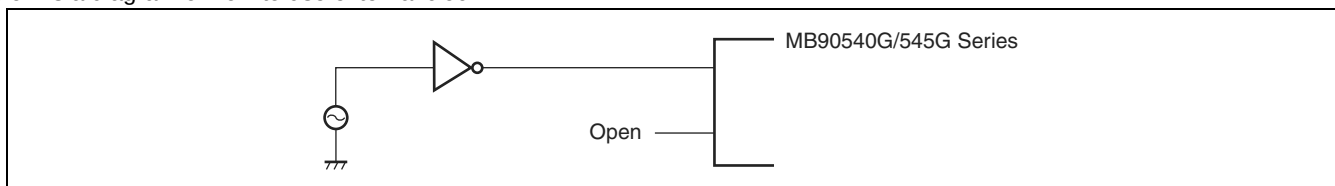
Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 k Ω .

Unused bi-directional pins should be set to the output state and can be left open, or the input state with the above described connection.

(3) Using external clock

To use external clock, drive X0 pin only and leave X1 pin unconnected.

Below is a diagram of how to use external clock.



(4) Use of the sub-clock

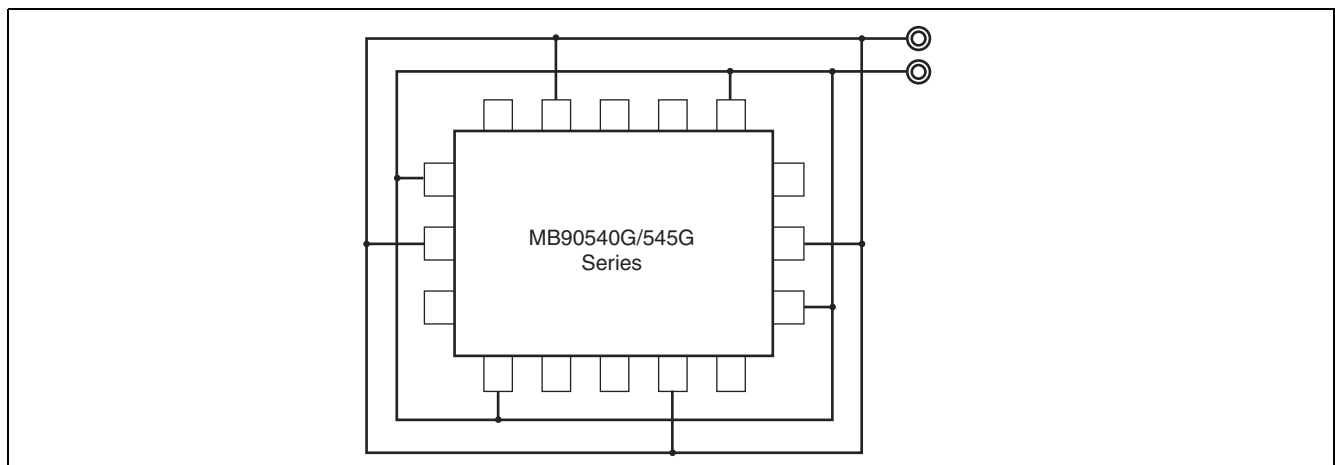
Use one clock system parts when the sub-clock is not used. In that case, pull-down the pin X0A and leave the pin X1A open. When using two clock system parts, a 32 kHz oscillator has to be connected to the X0A and X1A pins.

(5) Power supply pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to an external power and a ground line to lower the electromagnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect V_{CC} and V_{SS} pins via the lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 μF between V_{CC} and V_{SS} pins near the device.



8. I/O Map

Address	Register	Abbreviation	Access	Resource name	Initial value
00 _H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX _B
01 _H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX _B
02 _H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX _B
03 _H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX _B
04 _H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX _B
05 _H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX _B
06 _H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX _B
07 _H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXX _B
08 _H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX _B
09 _H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX _B
0A _H	Port A data register	PDRA	R/W	Port A	_____X _B
0B _H to 0F _H	Reserved				
10 _H	Port 0 direction register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0 _B
11 _H	Port 1 direction register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0 _B
12 _H	Port 2 direction register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0 _B
13 _H	Port 3 direction register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0 _B
14 _H	Port 4 direction register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0 _B
15 _H	Port 5 direction register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0 _B
16 _H	Port 6 direction register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0 _B
17 _H	Port 7 direction register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0 _B
18 _H	Port 8 direction register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0 _B
19 _H	Port 9 direction register	DDR9	R/W	Port 9	0 0 0 0 0 0 0 0 _B
1A _H	Port A direction register	DDRA	R/W	Port A	_____0 _B
1B _H	Analog Input Enable register	ADER	R/W	Port 6, A/D	1 1 1 1 1 1 1 1 _B
1C _H	Port 0 Pullup control register	PUCR0	R/W	Port 0	0 0 0 0 0 0 0 0 _B
1D _H	Port 1 Pullup control register	PUCR1	R/W	Port 1	0 0 0 0 0 0 0 0 _B
1E _H	Port 2 Pullup control register	PUCR2	R/W	Port 2	0 0 0 0 0 0 0 0 _B
1F _H	Port 3 Pullup control register	PUCR3	R/W	Port 3	0 0 0 0 0 0 0 0 _B
20 _H	Serial Mode Control Register 0	UMC0	R/W	UART0	0 0 0 0 0 1 0 0 _B
21 _H	Serial Status Register 0	USR0	R/W		0 0 0 1 0 0 0 0 _B
22 _H	Serial input data register 0/ Serial output data register 0	UIDR0/UODR0	R/W		XXXXXXXX _B
23 _H	Rate and data register 0	URD0	R/W		0 0 0 0 0 0 0 X _B

(Continued)

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A88 _H to 003A8F _H	003C88 _H to 003C8F _H	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
003A90 _H to 003A97 _H	003C90 _H to 003C97 _H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
003A98 _H to 003A9F _H	003C98 _H to 003C9F _H	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
003AA0 _H to 003AA7 _H	003CA0 _H to 003CA7 _H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
003AA8 _H to 003AAF _H	003CA8 _H to 003CAF _H	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
003AB0 _H to 003AB7 _H	003CB0 _H to 003CB7 _H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
003AB8 _H to 003ABF _H	003CB8 _H to 003CBF _H	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
003AC0 _H to 003AC7 _H	003CC0 _H to 003CC7 _H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
003AC8 _H to 003ACF _H	003CC8 _H to 003CCF _H	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
003AD0 _H to 003AD7 _H	003CD0 _H to 003CD7 _H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
003AD8 _H to 003ADF _H	003CD8 _H to 003CDF _H	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
003AE0 _H to 003AE7 _H	003CE0 _H to 003CE7 _H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
003AE8 _H to 003AEF _H	003CE8 _H to 003CEF _H	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B
003AF0 _H to 003AF7 _H	003CF0 _H to 003CF7 _H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
003AF8 _H to 003AFF _H	003CF8 _H to 003CFF _H	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

10. Interrupt Map

Interrupt cause	EI ² OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC _H	—	—
INT9 instruction	N/A	#09	FFFFD8 _H	—	—
Exception	N/A	#10	FFFFD4 _H	—	—
CAN 0 RX	N/A	#11	FFFFD0 _H	ICR00	0000B0 _H
CAN 0 TX/NS	N/A	#12	FFFFCC _H		
CAN 1 RX	N/A	#13	FFFFC8 _H	ICR01	0000B1 _H
CAN 1 TX/NS	N/A	#14	FFFFC4 _H		
External Interrupt INT0/INT1	*1	#15	FFFFC0 _H	ICR02	0000B2 _H
Time Base Timer	N/A	#16	FFFFBC _H		
16-bit Reload Timer 0	*1	#17	FFFFB8 _H	ICR03	0000B3 _H
8/10-bit A/D Converter	*1	#18	FFFFB4 _H		
16-bit Free-run Timer	N/A	#19	FFFFB0 _H	ICR04	0000B4 _H
External Interrupt INT2/INT3	*1	#20	FFFFAC _H		
Serial I/O	*1	#21	FFFFA8 _H	ICR05	0000B5 _H
8/16-bit PPG 0/1	N/A	#22	FFFFA4 _H		
Input Capture 0	*1	#23	FFFFA0 _H	ICR06	0000B6 _H
External Interrupt INT4/INT5	*1	#24	FFFF9C _H		
Input Capture 1	*1	#25	FFFF98 _H	ICR07	0000B7 _H
8/16-bit PPG 2/3	N/A	#26	FFFF94 _H		
External Interrupt INT6/INT7	*1	#27	FFFF90 _H	ICR08	0000B8 _H
Watch Timer	N/A	#28	FFFF8C _H		
8/16-bit PPG 4/5	N/A	#29	FFFF88 _H	ICR09	0000B9 _H
Input Capture 2/3	*1	#30	FFFF84 _H		
8/16-bit PPG 6/7	N/A	#31	FFFF80 _H	ICR10	0000BA _H
Output Compare 0	*1	#32	FFFF7C _H		
Output Compare 1	*1	#33	FFFF78 _H	ICR11	0000BB _H
Input Capture 4/5	*1	#34	FFFF74 _H		
Output Compare 2/3 - Input Capture 6/7	*1	#35	FFFF70 _H	ICR12	0000BC _H
16-bit Reload Timer 1	*1	#36	FFFF6C _H		
UART 0 RX	*2	#37	FFFF68 _H	ICR13	0000BD _H
UART 0 TX	*1	#38	FFFF64 _H		
UART 1 RX	*2	#39	FFFF60 _H	ICR14	0000BE _H
UART 1 TX	*1	#40	FFFF5C _H		
Flash Memory	N/A	#41	FFFF58 _H	ICR15	0000BF _H
Delayed interrupt	N/A	#42	FFFF54 _H		

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11.4 AC Characteristics

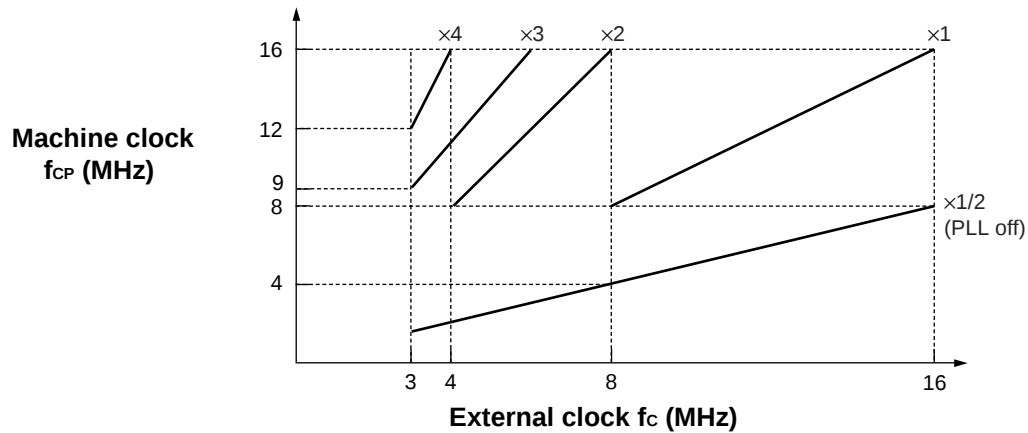
11.4.1 Clock Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ °C to }+105\text{ °C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ °C to }+105\text{ °C}$)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Oscillation frequency	f_c	X0, X1	3	—	16	MHz	No multiplier When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			8	—	16	MHz	PLL multiplied by 1 When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			4	—	8	MHz	PLL multiplied by 2 When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			3	—	5.33	MHz	PLL multiplied by 3 When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			3	—	4	MHz	PLL multiplied by 4 When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			3	—	5	MHz	When using an oscillator circuit $V_{CC} < 4.5\text{ V}$ (MB90F548GL(S)/543G(S)/ 547G(S)/548G(S))
			3	—	16	MHz	No multiplier When using an external clock
			8	—	16	MHz	PLL multiplied by 1 When using an external clock
			4	—	8	MHz	PLL multiplied by 2 When using an external clock
			3	—	5.33	MHz	PLL multiplied by 3 When using an external clock
			3	—	4	MHz	PLL multiplied by 4 When using an external clock
	f_{CL}	X0A, X1A	—	32.768	—	kHz	

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■ External clock frequency and Machine clock frequency


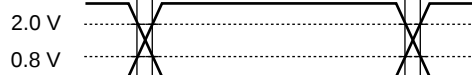
AC characteristics are set to the measured reference voltage values below.

■ Input signal waveform

Hysteresis Input Pin



TTL Input Pin


■ Output signal waveform

Output Pin

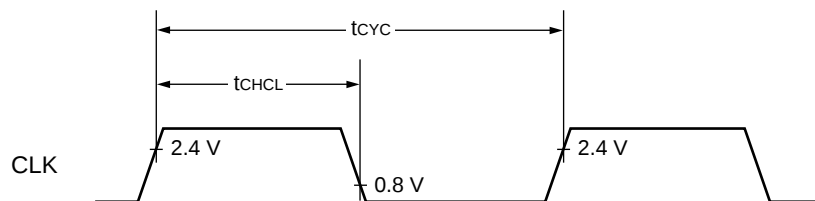


11.4.2 Clock Output Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	$V_{CC} = 5\text{ V} \pm 10\%$	62.5	—	ns	
CLK $\uparrow$ → CLK $\downarrow$	t_{CHCL}			20	—	ns	



11.4.3 Reset and Hardware Standby Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value		Units	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	$4\ t_{CP}$	—	ns	Under normal operation
			Oscillation time of oscillator + $4\ t_{CP}$	—	ms	In stop mode
			100	—	μs	In pseudo timer mode (MB90543G (S) /547G (S) /548G (S))
			$4\ t_{CP}$	—	ns	In pseudo timer mode (Other than MB90543G (S) /547G (S) /548G (S))
			$2\ t_{LCP}$	—	μs	In sub-clock mode, sub-sleep mode, timer mode
Hardware standby input time	t_{HSTL}	HST	$4\ t_{CP}$	—	ns	Under normal operation

Note : " t_{CP} " represents one cycle time of the machine clock.

Oscillation time of oscillator is time that amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ns.

Any reset can not fully initialize the Flash Memory if it is performing the automatic algorithm.

11.4.4 Power On Reset

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

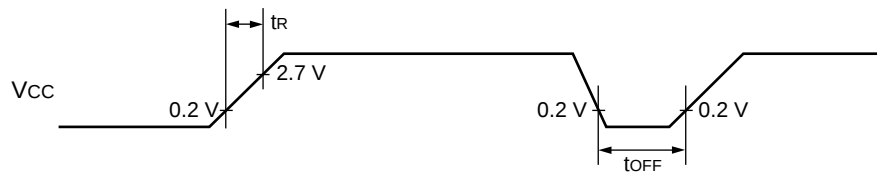
(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	*
Power off time	t_{OFF}	V_{CC}	—	50	—	ms	Waiting time until power-on

* : V_{CC} must be kept lower than 0.2 V before power-on.

Notes : ■ The above values are used for creating a power-on reset.

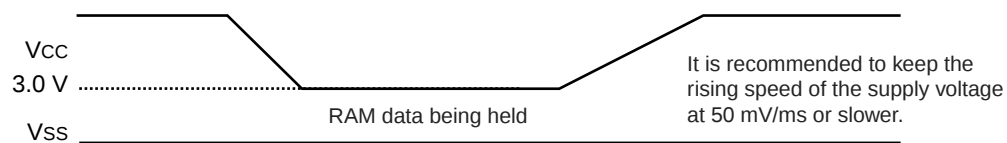
■ Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset.

To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.

In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.

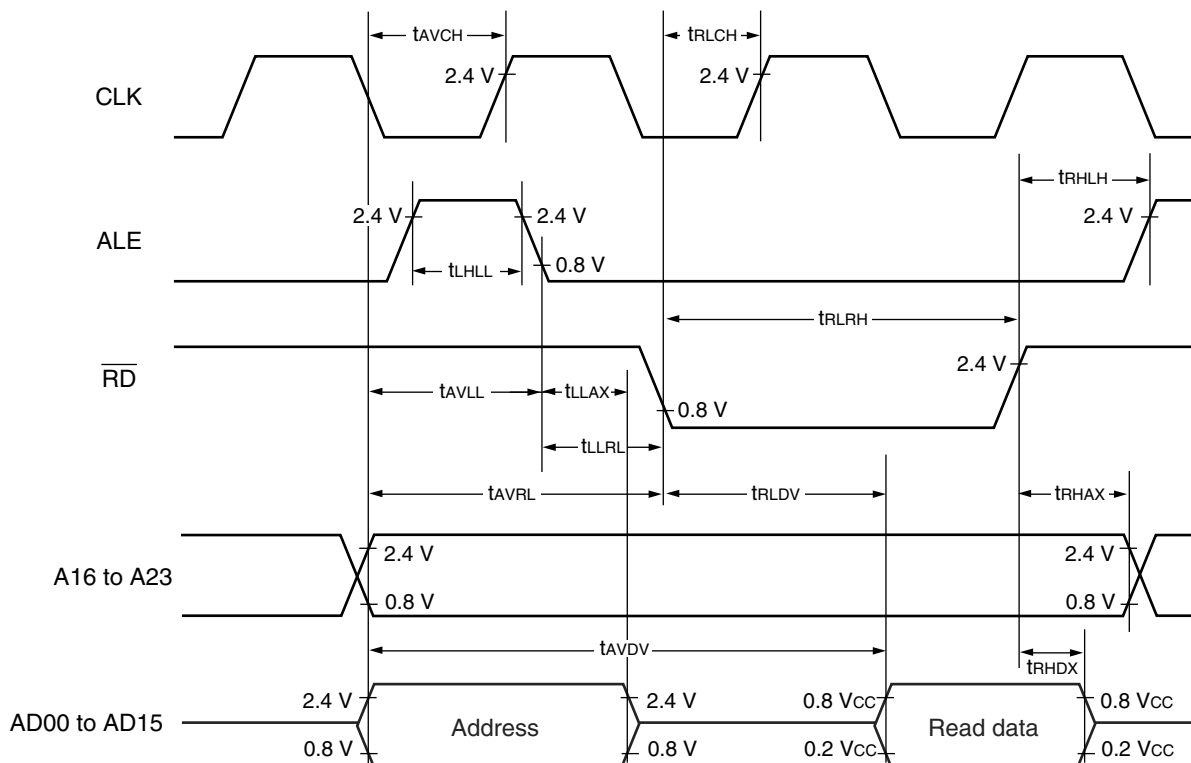


11.4.5 Bus Timing (Read)

 (MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

 (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 20$	—	ns	
Valid address → ALE↓ time	t_{AVLL}	ALE, A16 to A23, AD00 to AD15		$t_{CP}/2 - 20$	—	ns	
ALE↓ → Address valid time	t_{LLAX}	ALE, AD00 to AD15		$t_{CP}/2 - 15$	—	ns	
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	A16 to A23, AD00 to AD15, RD		$t_{CP} - 15$	—	ns	
Valid address → Valid data input	t_{AVDV}	A16 to A23, AD00 to AD15		—	$5 t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	RD		$3 t_{CP}/2 - 20$	—	ns	
$\overline{RD}$ ↓ → Valid data input	t_{RLDV}	$\overline{RD}$, AD00 to AD15		—	$3 t_{CP}/2 - 60$	ns	
$\overline{RD}$ ↑ → Data hold time	t_{RHDX}	$\overline{RD}$, AD00 to AD15		0	—	ns	
$\overline{RD}$ ↑ → ALE↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{RD}$ ↑ → Address valid time	t_{RHAX}	$\overline{RD}$, A16 to A23		$t_{CP}/2 - 10$	—	ns	
Valid address → CLK↑ time	t_{AVCH}	A16 to A23, AD00 to AD15, CLK		$t_{CP}/2 - 20$	—	ns	
$\overline{RD}$ ↓ → CLK↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 20$	—	ns	
ALE↓ → $\overline{RD}$ ↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	—	ns	

■ Bus Timing (Read)


11.5 A/D Converter

11.5.1 Electrical Characteristics

($V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $3.0 \text{ V} \leq AV_{RH} - AV_{RL}$, $T_A = -40 \text{ }^\circ\text{C}$ to $+105 \text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Conversion error	—	—	—	—	± 5.0	LSB	
Nonlinearity error	—	—	—	—	± 2.5	LSB	
Differential nonlinearity error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	$AV_{RL} - 3.5 \text{ LSB}$	$AV_{RL} + 0.5 \text{ LSB}$	$AV_{RL} + 4.5 \text{ LSB}$	V	
Full scale transition voltage	V_{FST}	AN0 to AN7	$AV_{RH} - 6.5 \text{ LSB}$	$AV_{RH} - 1.5 \text{ LSB}$	$AV_{RH} + 1.5 \text{ LSB}$	V	
Compare time	—	—	$352 \text{ } t_{CP}$	—	—	ns	Internal frequency : 16 MHz
Sampling time	—	—	$64 \text{ } t_{CP}$	—	—	ns	Internal frequency : 16 MHz
Analog port input current	I_{AIN}	AN0 to AN7	-1	—	1	μA	$V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 1\%$
Analog input voltage range	V_{AIN}	AN0 to AN7	AV_{RL}	—	AV_{RH}	V	
Reference voltage range	—	AV_{RH}	$AV_{RL} + 2.7$	—	AV_{CC}	V	
	—	AV_{RL}	0	—	$AV_{RH} - 2.7$	V	
Power supply current	I_A	AV_{CC}	—	5	—	mA	
	I_{AH}	AV_{CC}	—	—	5	μA	*
Reference voltage supply current	I_R	AV_{RH}	—	400	600	μA	Flash device
			—	140	260	μA	MASK ROM
	I_{RH}	AV_{RH}	—	—	5	μA	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

* : When not using an A/D converter, this is the current ($V_{CC} = AV_{CC} = AV_{RH} = 5.0 \text{ V}$) when the CPU is stopped.

Note: The functionality of the A/D converter is only guaranteed for $V_{CC} = 5.0 \text{ V} \pm 10\%$ (also for MB90543G(S)/547G(S)/548G(S)/F548G(S)/F548GL(S)).

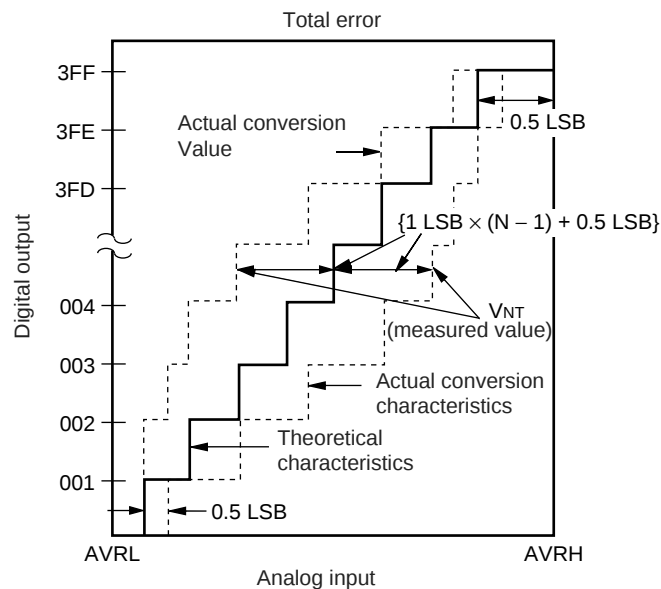
11.5.2 A/D Converter Glossary

Resolution : Analog changes that are identifiable with the A/D converter

Linearity error : The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ↔ "11 1111 1111") from actual conversion characteristics

Differential linearity error : The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error : The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1 \text{ LSB} = (\text{Theoretical value}) \frac{AVRH - AVRL}{1024} [\text{V}]$$

$$V_{OT} (\text{Theoretical value}) = AVRL + 0.5 \text{ LSB} [\text{V}]$$

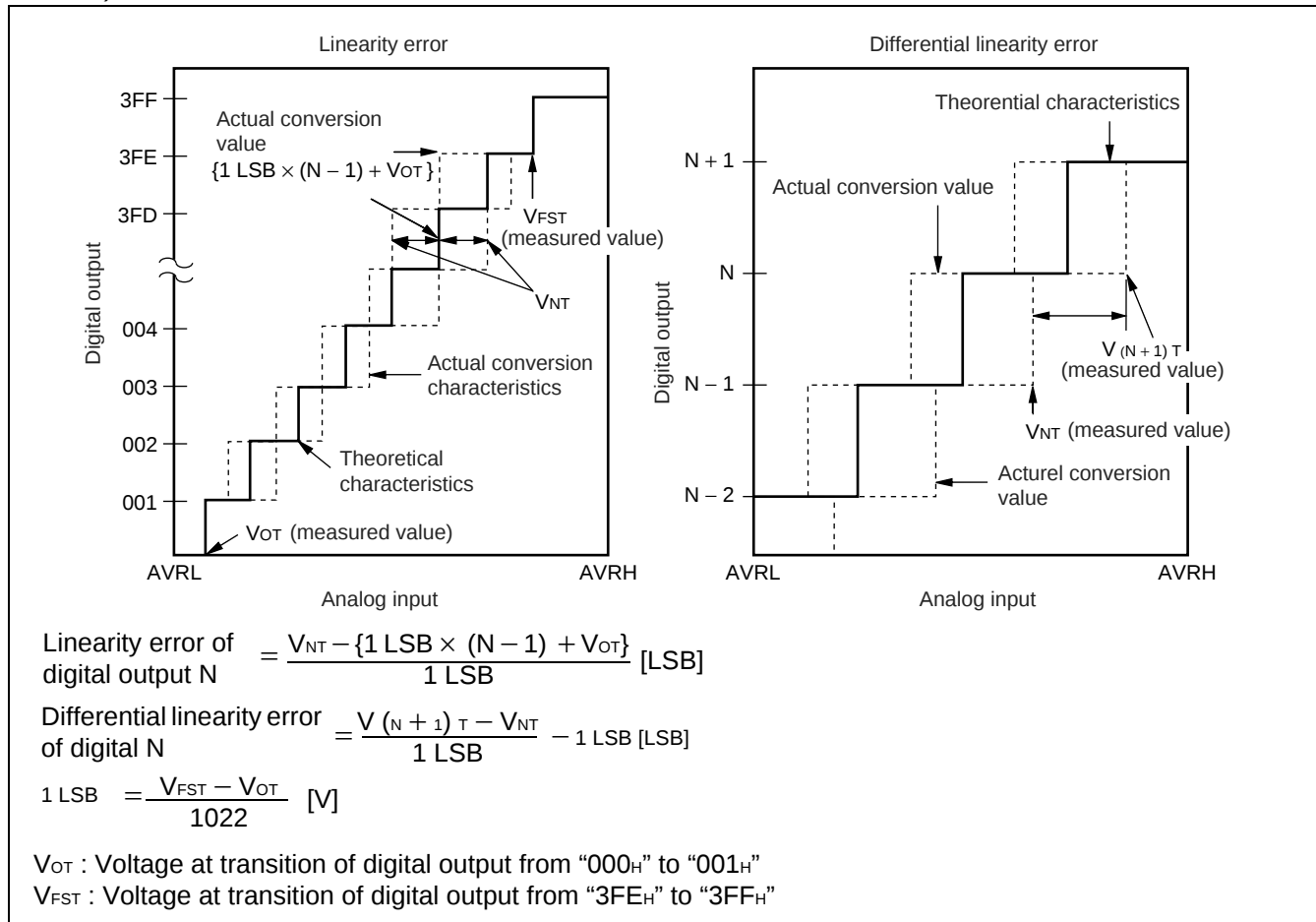
$$V_{FST} (\text{Theoretical value}) = AVRH - 1.5 \text{ LSB} [\text{V}]$$

$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} [\text{LSB}]$$

V_{NT} : Voltage at a transition of digital output from $(N - 1)$ to N

(Continued)

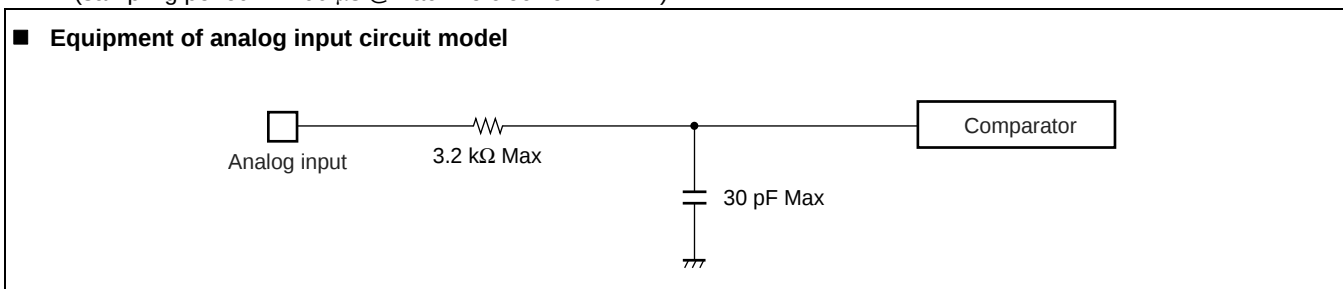
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11.5.3 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions, :

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
 - When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.
- Note : When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz) .



11.5.4 Error

The smaller the | AVRH – AVRL |, the greater the error would become relatively.

(Continued)

