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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gpmc-g

Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
20	22	P44	G	General I/O port. This function is enabled when UART1 disables the clock output.
		SCK1		Serial clock pulse I/O pin for UART1. This function is enabled when UART1 enables the serial clock output.
22	24	P45	G	General I/O port. This function is enabled when UART1 disables the serial data output.
		SOT1		Serial data output pin for UART1. This function is enabled when UART1 enables the serial data output.
23	25	P46	G	General I/O port. This function is enabled when the Extended I/O serial interface disables the serial data output.
		SOT2		Serial data output pin for the Extended I/O serial interface. This function is enabled when the Extended I/O serial interface enables the serial data output.
24	26	P47	G	General I/O port. This function is enabled when the Extended I/O serial interface disables the clock output.
		SCK2		Serial clock pulse I/O pin for the Extended I/O serial interface . This function is enabled when the Extended I/O serial interface enables the Serial clock output.
26	28	P50	D	General I/O port. This function is always enabled.
		SIN2		Serial data input pin for the Extended I/O serial interface . Set the corresponding Port Direction Register to input if this function is used.
27 to 30	29 to 32	P51 to P54	D	General I/O port. This function is always enabled.
		INT4 to INT7		External interrupt request input pins for INT4 to INT7. Set the corresponding Port Direction Register to input if this function is used.
31	33	P55	D	General I/O port. This function is always enabled.
		ADTG		Trigger input pin for the A/D converter. Set the corresponding Port Direction Register to input if this function is used.
36 to 39	38 to 41	P60 to P63	E	General I/O port. This function is enabled when the analog input enable register specifies a port.
		AN0 to AN3		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.
41 to 44	43 to 46	P64 to P67	E	General I/O port. The function is enabled when the analog input enable register specifies a port.
		AN4 to AN7		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.
45	47	P56	D	General I/O port. This function is always enabled.
		TIN0		Event input pin for the 16-bit reload timers 0. Set the corresponding Port Direction Register to input if this function is used.

(Continued)

Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
46	48	P57	D	General I/O port. This function is enabled when the 16-bit reload timers 0 disables the output.
		TOT0		Output pin for the 16-bit reload timers 0. This function is enabled when the 16-bit reload timers 0 enables the output.
51 to 56	53 to 58	P70 to P75	D	General I/O ports. This function is always enabled.
		IN0 to IN5		Trigger input pins for input captures ICU0 to ICU5. Set the corresponding Port Direction Register to input if this function is used.
57 , 58	59 , 60	P76 , P77	D	General I/O ports. This function is enabled when the OCU disables the waveform output.
		OUT2 , OUT3		Event output pins for output compares OCU2 and OCU3. This function is enabled when the OCU enables the waveform output.
		IN6 , IN7		Trigger input pins for input captures ICU6 and ICU7. Set the corresponding Port Direction Register to input and disable the OCU waveform output if this function is used.
59 to 62	61 to 64	P80 to P83	D	General I/O ports. This function is enabled when 8/16-bit PPG disables the waveform output.
		PPG0 to PPG3		Output pins for 8/16-bit PPGs. This function is enabled when 8/16-bit PPG enables the waveform output.
63 , 64	65 , 66	P84 , P85	D	General I/O ports. This function is enabled when the OCU disables the waveform output.
		OUT0 , OUT1		Waveform output pins for output compares OCU0 and OCU1. This function is enabled when the OCU enables the waveform output.
65	67	P86	D	General I/O port. This function is always enabled.
		TIN1		Input pin for the 16-bit reload timers 1. Set the corresponding Port Direction Register to input if this function is used.
66	68	P87	D	General I/O port. This function is enabled when the 16-bit reload timers 1 disables the output.
		TOT1		Output pin for the 16-bit reload timers 1.This function is enabled when the 16-bit reload timers 1 enables the output.
67 to 70	69 to 72	P90 to P93	D	General I/O port. This function is always enabled.
		INT0 to INT3		External interrupt request input pins for INT0 to INT3. Set the corresponding Port Direction Register to input if this function is used.
71	73	P94	D	General I/O port. This function is enabled when CAN0 disables the output.
		TX0		TX output pin for CAN0. This function is enabled when CAN0 enables the output.

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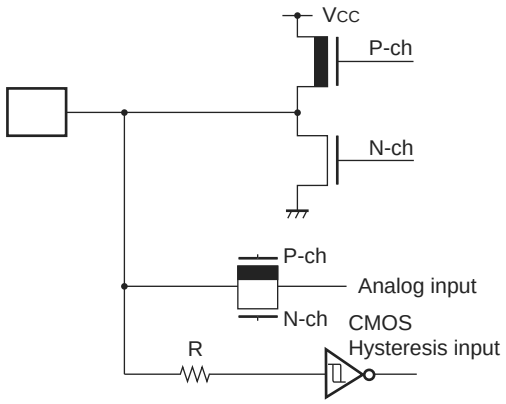
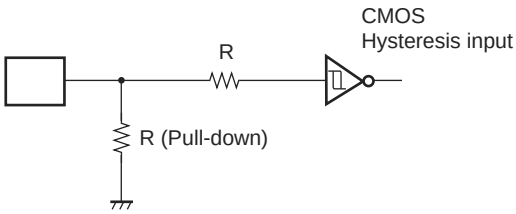
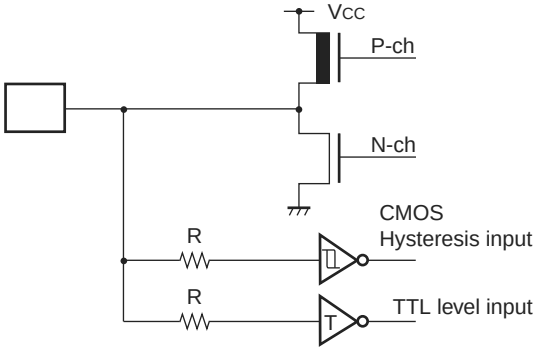
Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
72	74	P95	D	General I/O port. This function is always enabled.
		RX0		RX input pin for CAN0 Interface. When the CAN function is used, output from the other functions must be stopped.
73	75	P96	D	General I/O port. This function is enabled when CAN1 disables the output.
		TX1		TX output pin for CAN1. This function is enabled when CAN1 enables the output (only MB90540G series) .
74	76	P97	D	General I/O port. This function is always enabled.
		RX1		RX input pin for CAN1 Interface. When the CAN function is used, output from the other functions must be stopped (only MB90540G series) .
76	78	PA0	D	General I/O port. This function is always enabled.
32	34	AV_{CC}	Power supply	Power supply pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AV_{CC} is applied to V_{CC}.
35	37	AV_{SS}	Power supply	Power supply pin for the A/D Converter.
33	35	AVRH	Power supply	External reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV_{CC}.
34	36	AVRL	Power supply	External reference voltage input pin for the A/D Converter.
47, 48	49, 50	MD0, MD1	C	Input pins for specifying the operating mode. The pins must be directly connected to V_{CC} or V_{SS}.
49	51	MD2	F	Input pin for specifying the operating mode. The pin must be directly connected to V_{CC} or V_{SS}.
25	27	C	—	Power supply stabilization capacitor pin. It should be connected externally to an 0.1 µF ceramic capacitor.
21, 82	23, 84	V_{CC}	Power supply	Input pin for power supply (5.0 V) .
9, 40, 79	11, 42, 81	V_{SS}	Power supply	Input pin for power supply (0.0 V) .

*1 : FPT-100P-M06

*2 : FPT-100P-M20

Circuit type	Diagram	Remarks
E		■ CMOS level output ■ CMOS Hysteresis input ■ Analog input
F		■ CMOS Hysteresis input ■ Pull-down Resistor : 50 kΩ approx. (except Flash devices)
G		■ CMOS level output ■ CMOS Hysteresis input ■ TTL level input (Flash devices in Flash writer mode only)

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5. Handling Devices

(1) Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS}.
- The AVcc power supply is applied before the V_{CC} voltage.

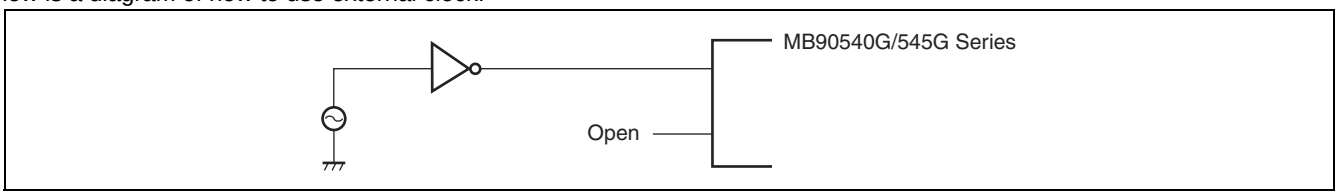
Latch-up may increase the power supply current drastically, causing thermal damage to the device.
For the same reason, care must also be taken in not allowing the analog power-supply voltage (AV_{CC}, AVRH) to exceed the digital power-supply voltage.

(2) Handling unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefor they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.
Unused bi-directional pins should be set to the output state and can be left open, or the input state with the above described connection.

(3) Using external clock

To use external clock, drive X0 pin only and leave X1 pin unconnected.
Below is a diagram of how to use external clock.

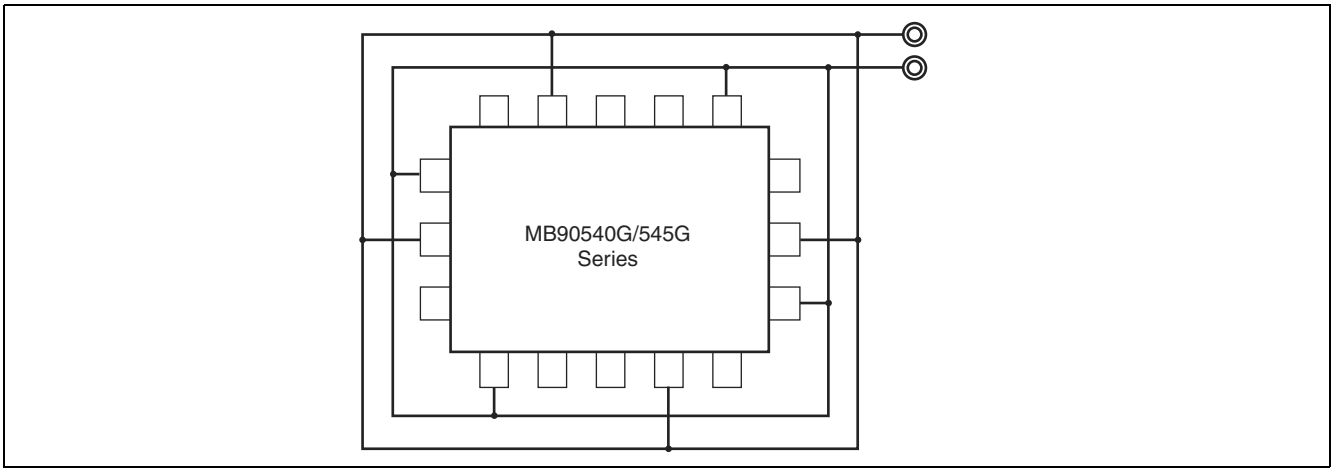


(4) Use of the sub-clock

Use one clock system parts when the sub-clock is not used. In that case, pull-down the pin X0A and leave the pin X1A open. When using two clock system parts, a 32 kHz oscillator has to be connected to the X0A and X1A pins.

(5) Power supply pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.
Make sure to connect V_{CC} and V_{SS} pins via the lowest impedance to power lines.
It is recommended to provide a bypass capacitor of around 0.1 μF between V_{CC} and V_{SS} pins near the device.



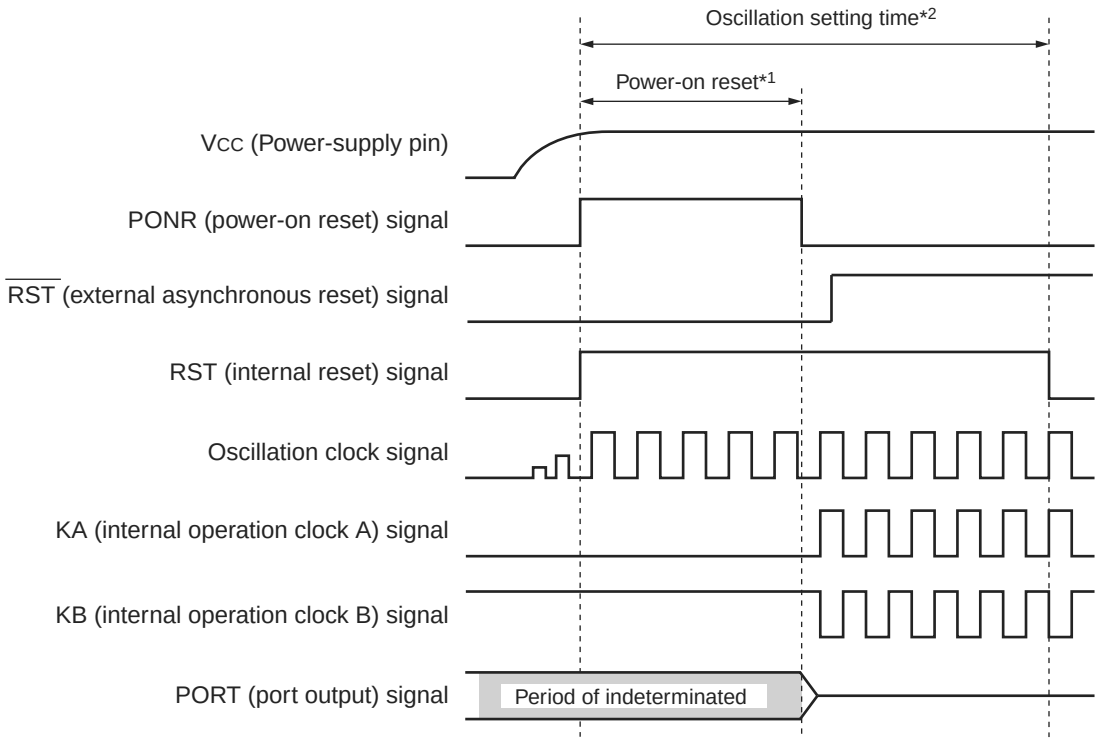
(12) Indeterminate outputs from ports 0 and 1 (MB90V540G only)

During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

- If $\overline{RST}$ pin is “H”, the outputs become indeterminate.
- If $\overline{RST}$ pin is “L”, the outputs become high-impedance.

Pay attention to the port output timing shown as follow.

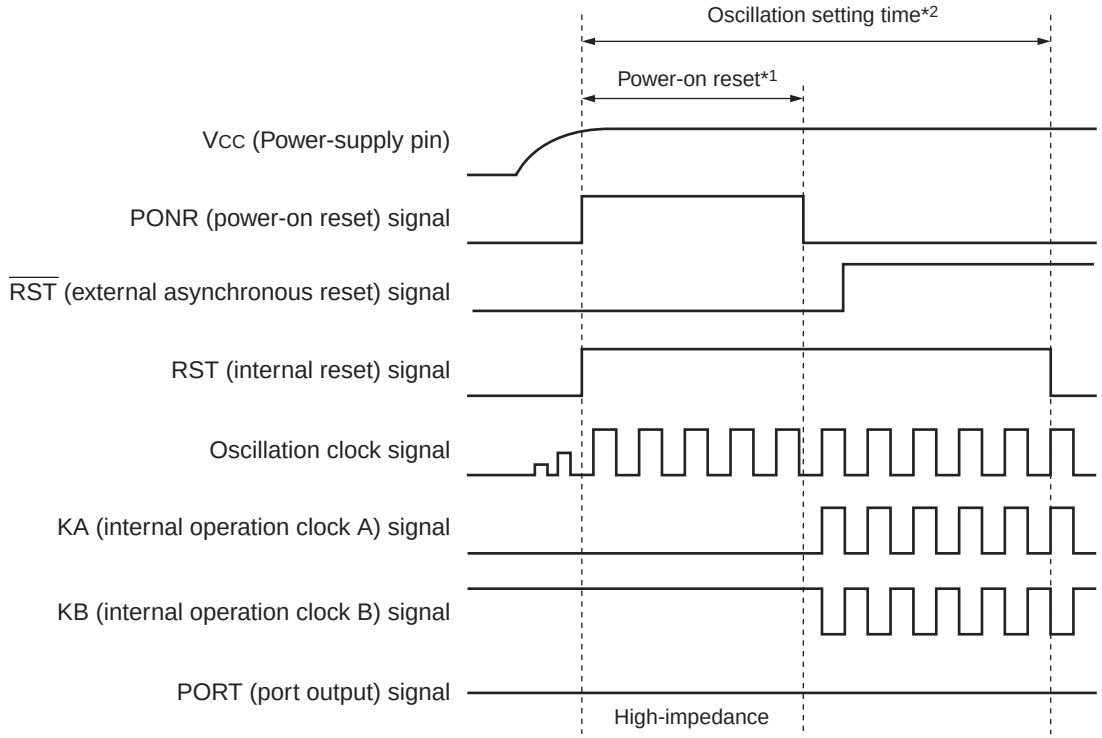
- $\overline{RST}$ pin is “H”



*1 : Power-on reset time : “Period of clock frequency” × 2^{17} (Clock frequency of 16 MHz : 8.19 ms)

*2 : Oscillation setting time : “Period of clock frequency” × 2^{18} (Clock frequency of 16 MHz : 16.38 ms)

■ $\overline{\text{RST}}$ pin is “L”



*1 : Power-on reset time : “Period of clock frequency” × 2^{17} (Clock frequency of 16 MHz : 8.19 ms)

*2 : Oscillation setting time : “Period of clock frequency” × 2^{18} (Clock frequency of 16 MHz : 16.38 ms)

(13) Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(14) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions

In the Signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”) , the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00_H”.

If the values of the corresponding bank registers (DTB, ADB, USB, SSB) are set to other than “00_H”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

(15) Using REALOS

The use of EI²OS is not possible with the REALOS real time operating system.

(16) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

Address	Register	Abbreviation	Access	Resource name	Initial value
3900H	Reload L	PRLL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXXB
3901H	Reload H	PRLH0	R/W		XXXXXXXXB
3902H	Reload L	PRLL1	R/W		XXXXXXXXB
3903H	Reload H	PRLH1	R/W		XXXXXXXXB
3904H	Reload L	PRLL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXXB
3905H	Reload H	PRLH2	R/W		XXXXXXXXB
3906H	Reload L	PRLL3	R/W		XXXXXXXXB
3907H	Reload H	PRLH3	R/W		XXXXXXXXB
3908H	Reload L	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXXB
3909H	Reload H	PRLH4	R/W		XXXXXXXXB
390AH	Reload L	PRLL5	R/W		XXXXXXXXB
390BH	Reload H	PRLH5	R/W		XXXXXXXXB
390CH	Reload L	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXXB
390DH	Reload H	PRLH6	R/W		XXXXXXXXB
390EH	Reload L	PRLL7	R/W		XXXXXXXXB
390FH	Reload H	PRLH7	R/W		XXXXXXXXB
3910H to 3917H	Reserved				
3918H	Input Capture Register 0	IPCP0	R	Input Capture 0/1	XXXXXXXXB
3919H	Input Capture Register 0	IPCP0	R		XXXXXXXXB
391AH	Input Capture Register 1	IPCP1	R		XXXXXXXXB
391BH	Input Capture Register 1	IPCP1	R		XXXXXXXXB
391CH	Input Capture Register 2	IPCP2	R	Input Capture 2/3	XXXXXXXXB
391DH	Input Capture Register 2	IPCP2	R		XXXXXXXXB
391EH	Input Capture Register 3	IPCP3	R		XXXXXXXXB
391FH	Input Capture Register 3	IPCP3	R		XXXXXXXXB
3920H	Input Capture Register 4	IPCP4	R	Input Capture 4/5	XXXXXXXXB
3921H	Input Capture Register 4	IPCP4	R		XXXXXXXXB
3922H	Input Capture Register 5	IPCP5	R		XXXXXXXXB
3923H	Input Capture Register 5	IPCP5	R		XXXXXXXXB
3924H	Input Capture Register 6	IPCP6	R	Input Capture 6/7	XXXXXXXXB
3925H	Input Capture Register 6	IPCP6	R		XXXXXXXXB
3926H	Input Capture Register 7	IPCP7	R		XXXXXXXXB
3927H	Input Capture Register 7	IPCP7	R		XXXXXXXXB

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Address	Register	Abbreviation	Access	Resource name	Initial value
3928H	Output Compare Register 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
3929H	Output Compare Register 0	OCCP0	R/W		XXXXXXXXB
392AH	Output Compare Register 1	OCCP1	R/W		XXXXXXXXB
392BH	Output Compare Register 1	OCCP1	R/W		XXXXXXXXB
392CH	Output Compare Register 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXXB
392DH	Output Compare Register 2	OCCP2	R/W		XXXXXXXXB
392EH	Output Compare Register 3	OCCP3	R/W		XXXXXXXXB
392FH	Output Compare Register 3	OCCP3	R/W		XXXXXXXXB
3930H to 39FFH	Reserved				
3A00H to 3AFFH	Reserved for CAN 0 Interface.				
3B00H to 3BFFH	Reserved for CAN 0 Interface.				
3C00H to 3CFFH	Reserved for CAN 1 Interface.				
3D00H to 3DFFH	Reserved for CAN 1 Interface.				
3E00H to 3FFFH	Reserved				

- Read/write notation
  - R/W : Reading and writing permitted
  - R : Read-only
  - W : Write-only

- Initial value notation
  - 0 : Initial value is “0”.
  - 1 : Initial value is “1”.
  - X : Initial value is undefined.
  - _ : Initial value is unused.

Note: Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

(Continued)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003B00H	003D00H	Control status register	CSR	R/W, R	00---000 0----0-1B
003B01H	003D01H				
003B02H	003D02H	Last event indicator register	LEIR	R/W	-------- 000-0000B
003B03H	003D03H				
003B04H	003D04H	Receive/transmit error counter register	RTEC	R	00000000 00000000B
003B05H	003D05H				
003B06H	003D06H	Bit timing register	BTR	R/W	-1111111 11111111B
003B07H	003D07H				
003B08H	003D08H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXXB
003B09H	003D09H				
003B0AH	003D0AH	Transmit RTR register	TRTRR	R/W	00000000 00000000B
003B0BH	003D0BH				
003B0CH	003D0CH	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXXB
003B0DH	003D0DH				
003B0EH	003D0EH	Transmit request enable register	TIER	R/W	00000000 00000000B
003B0FH	003D0FH				
003B10H	003D10H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXXB
003B11H	003D11H				
003B12H	003D12H				XXXXXXXX XXXXXXXXB
003B13H	003D13H				
003B14H	003D14H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXXB
003B15H	003D15H				
003B16H	003D16H				XXXXX--- XXXXXXXXB
003B17H	003D17H				
003B18H	003D18H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXXB
003B19H	003D19H				
003B1AH	003D1AH				XXXXX--- XXXXXXXXB
003B1BH	003D1BH				

List of Message Buffers (ID Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A00H to 003A1FH	003C00H to 003C1FH	General-purpose RAM	—	R/W	XXXXXXXXB to XXXXXXXXB
003A20H	003C20H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXXB
003A21H	003C21H				
003A22H	003C22H				XXXXX--- XXXXXXXXB
003A23H	003C23H				

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A24H	003C24H	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXXB
003A25H	003C25H				
003A26H	003C26H				XXXXX--- XXXXXXXXB
003A27H	003C27H				
003A28H	003C28H	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXXB
003A29H	003C29H				
003A2AH	003C2AH				XXXXX--- XXXXXXXXB
003A2BH	003C2BH				
003A2CH	003C2CH	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXXB
003A2DH	003C2DH				
003A2EH	003C2EH				XXXXX--- XXXXXXXXB
003A2FH	003C2FH				
003A30H	003C30H	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXXB
003A31H	003C31H				
003A32H	003C32H				XXXXX--- XXXXXXXXB
003A33H	003C33H				
003A34H	003C34H	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXXB
003A35H	003C35H				
003A36H	003C36H				XXXXX--- XXXXXXXXB
003A37H	003C37H				
003A38H	003C38H	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXXB
003A39H	003C39H				
003A3AH	003C3AH				XXXXX--- XXXXXXXXB
003A3BH	003C3BH				

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A3C$_H$	003C3C$_H$	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX$_B$
003A3D$_H$	003C3D$_H$				
003A3E$_H$	003C3E$_H$				XXXXX--- XXXXXXXX$_B$
003A3F$_H$	003C3F$_H$				
003A40$_H$	003C40$_H$	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX$_B$
003A41$_H$	003C41$_H$				
003A42$_H$	003C42$_H$				XXXXX--- XXXXXXXX$_B$
003A43$_H$	003C43$_H$				
003A44$_H$	003C44$_H$	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX$_B$
003A45$_H$	003C45$_H$				
003A46$_H$	003C46$_H$				XXXXX--- XXXXXXXX$_B$
003A47$_H$	003C47$_H$				
003A48$_H$	003C48$_H$	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX$_B$
003A49$_H$	003C49$_H$				
003A4A$_H$	003C4A$_H$				XXXXX--- XXXXXXXX$_B$
003A4B$_H$	003C4B$_H$				
003A4C$_H$	003C4C$_H$	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX$_B$
003A4D$_H$	003C4D$_H$				
003A4E$_H$	003C4E$_H$				XXXXX--- XXXXXXXX$_B$
003A4F$_H$	003C4F$_H$				
003A50$_H$	003C50$_H$	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX$_B$
003A51$_H$	003C51$_H$				
003A52$_H$	003C52$_H$				XXXXX--- XXXXXXXX$_B$
003A53$_H$	003C53$_H$				
003A54$_H$	003C54$_H$	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX$_B$
003A55$_H$	003C55$_H$				
003A56$_H$	003C56$_H$				XXXXX--- XXXXXXXX$_B$
003A57$_H$	003C57$_H$				
003A58$_H$	003C58$_H$	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX$_B$
003A59$_H$	003C59$_H$				
003A5A$_H$	003C5A$_H$				XXXXX--- XXXXXXXX$_B$
003A5B$_H$	003C5B$_H$				
003A5C$_H$	003C5C$_H$	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX$_B$
003A5D$_H$	003C5D$_H$				
003A5E$_H$	003C5E$_H$				XXXXX--- XXXXXXXX$_B$
003A5F$_H$	003C5F$_H$				

List of Message Buffers (DLC Registers and Data Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A60H	003C60H	DLC register 0	DLCR0	R/W	----XXXXB
003A61H	003C61H				
003A62H	003C62H	DLC register 1	DLCR1	R/W	----XXXXB
003A63H	003C63H				
003A64H	003C64H	DLC register 2	DLCR2	R/W	----XXXXB
003A65H	003C65H				
003A66H	003C66H	DLC register 3	DLCR3	R/W	----XXXXB
003A67H	003C67H				
003A68H	003C68H	DLC register 4	DLCR4	R/W	----XXXXB
003A69H	003C69H				
003A6AH	003C6AH	DLC register 5	DLCR5	R/W	----XXXXB
003A6BH	003C6BH				
003A6CH	003C6CH	DLC register 6	DLCR6	R/W	----XXXXB
003A6DH	003C6DH				
003A6EH	003C6EH	DLC register 7	DLCR7	R/W	----XXXXB
003A6FH	003C6FH				
003A70H	003C70H	DLC register 8	DLCR8	R/W	----XXXX
003A71H	003C71H				
003A72H	003C72H	DLC register 9	DLCR9	R/W	----XXXXB
003A73H	003C73H				
003A74H	003C74H	DLC register 10	DLCR10	R/W	----XXXXB
003A75H	003C75H				
003A76H	003C76H	DLC register 11	DLCR11	R/W	----XXXXB
003A77H	003C77H				
003A78H	003C78H	DLC register 12	DLCR12	R/W	----XXXXB
003A79H	003C79H				
003A7AH	003C7AH	DLC register 13	DLCR13	R/W	----XXXXB
003A7BH	003C7BH				
003A7CH	003C7CH	DLC register 14	DLCR14	R/W	----XXXXB
003A7DH	003C7DH				
003A7EH	003C7EH	DLC register 15	DLCR15	R/W	----XXXXB
003A7FH	003C7FH				
003A80H to 003A87H	003C80H to 003C87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB

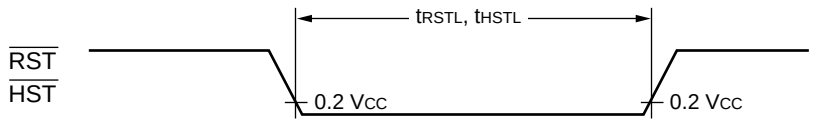
(Continued)

10. Interrupt Map

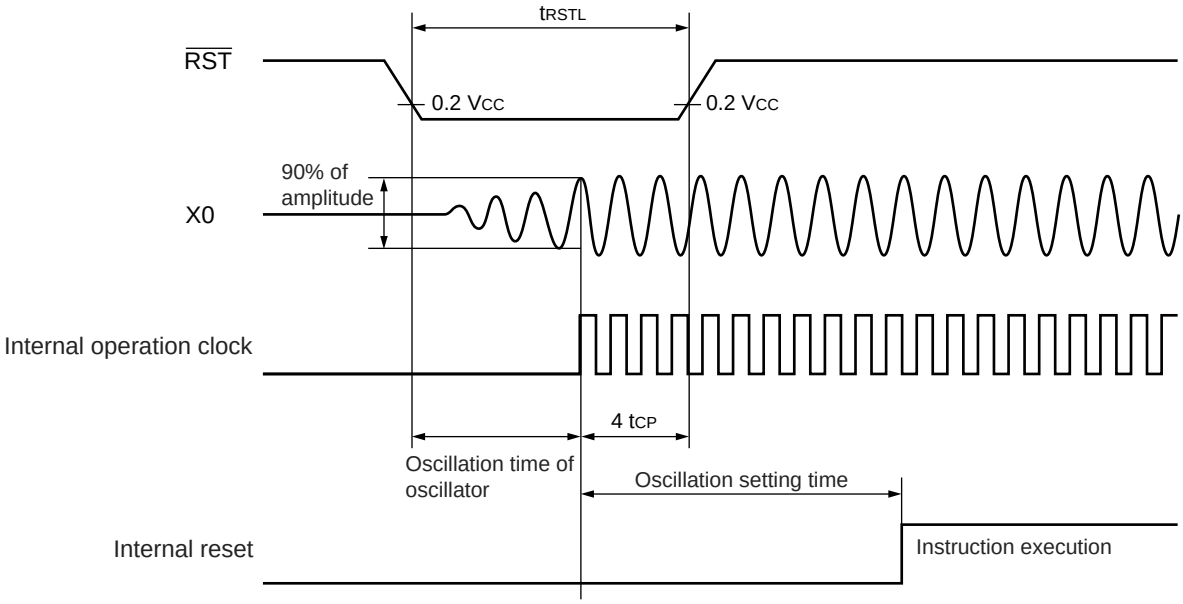
Interrupt cause	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC$_H$	—	—
INT9 instruction	N/A	#09	FFFFD8$_H$	—	—
Exception	N/A	#10	FFFFD4$_H$	—	—
CAN 0 RX	N/A	#11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN 0 TX/NS	N/A	#12	FFFFCC$_H$		
CAN 1 RX	N/A	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 1 TX/NS	N/A	#14	FFFFC4$_H$		
External Interrupt INT0/INT1	*1	#15	FFFFC0$_H$	ICR02	0000B2$_H$
Time Base Timer	N/A	#16	FFFFBC$_H$		
16-bit Reload Timer 0	*1	#17	FFFFB8$_H$	ICR03	0000B3$_H$
8/10-bit A/D Converter	*1	#18	FFFFB4$_H$		
16-bit Free-run Timer	N/A	#19	FFFFB0$_H$	ICR04	0000B4$_H$
External Interrupt INT2/INT3	*1	#20	FFFFAC$_H$		
Serial I/O	*1	#21	FFFFA8$_H$	ICR05	0000B5$_H$
8/16-bit PPG 0/1	N/A	#22	FFFFA4$_H$		
Input Capture 0	*1	#23	FFFFA0$_H$	ICR06	0000B6$_H$
External Interrupt INT4/INT5	*1	#24	FFFF9C$_H$		
Input Capture 1	*1	#25	FFFF98$_H$	ICR07	0000B7$_H$
8/16-bit PPG 2/3	N/A	#26	FFFF94$_H$		
External Interrupt INT6/INT7	*1	#27	FFFF90$_H$	ICR08	0000B8$_H$
Watch Timer	N/A	#28	FFFF8C$_H$		
8/16-bit PPG 4/5	N/A	#29	FFFF88$_H$	ICR09	0000B9$_H$
Input Capture 2/3	*1	#30	FFFF84$_H$		
8/16-bit PPG 6/7	N/A	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 0	*1	#32	FFFF7C$_H$		
Output Compare 1	*1	#33	FFFF78$_H$	ICR11	0000BB$_H$
Input Capture 4/5	*1	#34	FFFF74$_H$		
Output Compare 2/3 - Input Capture 6/7	*1	#35	FFFF70$_H$	ICR12	0000BC$_H$
16-bit Reload Timer 1	*1	#36	FFFF6C$_H$		
UART 0 RX	*2	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 0 TX	*1	#38	FFFF64$_H$		
UART 1 RX	*2	#39	FFFF60$_H$	ICR14	0000BE$_H$
UART 1 TX	*1	#40	FFFF5C$_H$		
Flash Memory	N/A	#41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed interrupt	N/A	#42	FFFF54$_H$		

(Continued)

■ In under normal operation, pseudo timer mode, sub-clock mode, sub-sleep mode, timer mode



■ In stop mode



11.4.4 Power On Reset

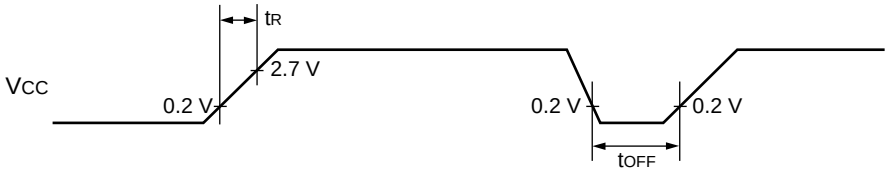
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

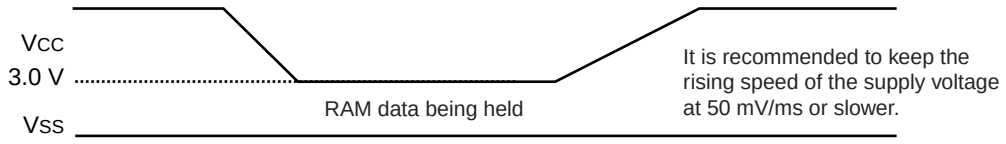
Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	*
Power off time	t_{OFF}	V_{CC}		50	—	ms	Waiting time until power-on

* : V_{CC} must be kept lower than 0.2 V before power-on.

Notes : ■ The above values are used for creating a power-on reset.
■ Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.



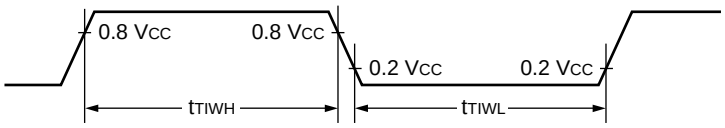
11.4.10 Timer Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	4 t_{CP}	—	ns	
	t_{TIWL}	IN0 to IN7					

■ **Timer Input Timing**



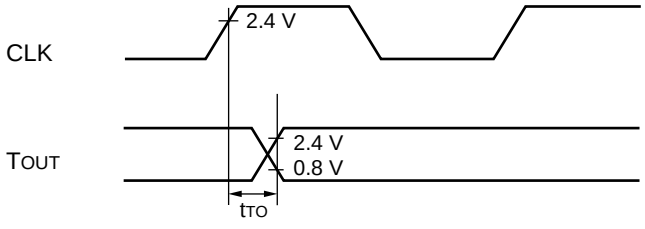
11.4.11 Timer Output Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
CLK↑ → T_{OUT} change time	t_{TO}	TOT0 , TOT1, PPG0 to PPG3	—	30	—	ns	

■ **Timer Output Timing**



11.5 A/D Converter

11.5.1 Electrical Characteristics

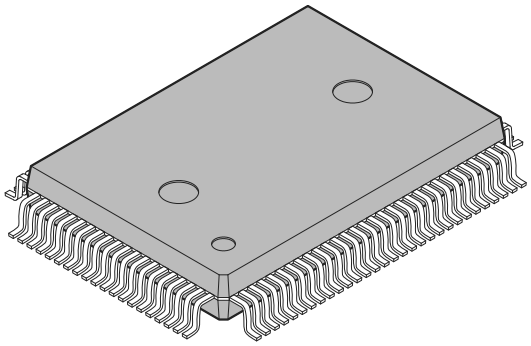
($V_{CC} = AV_{CC} = 5.0\ V \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\ V$, $3.0\ V \leq AVRH - AVRL$, $T_A = -40\ °C$ to $+105\ °C$)

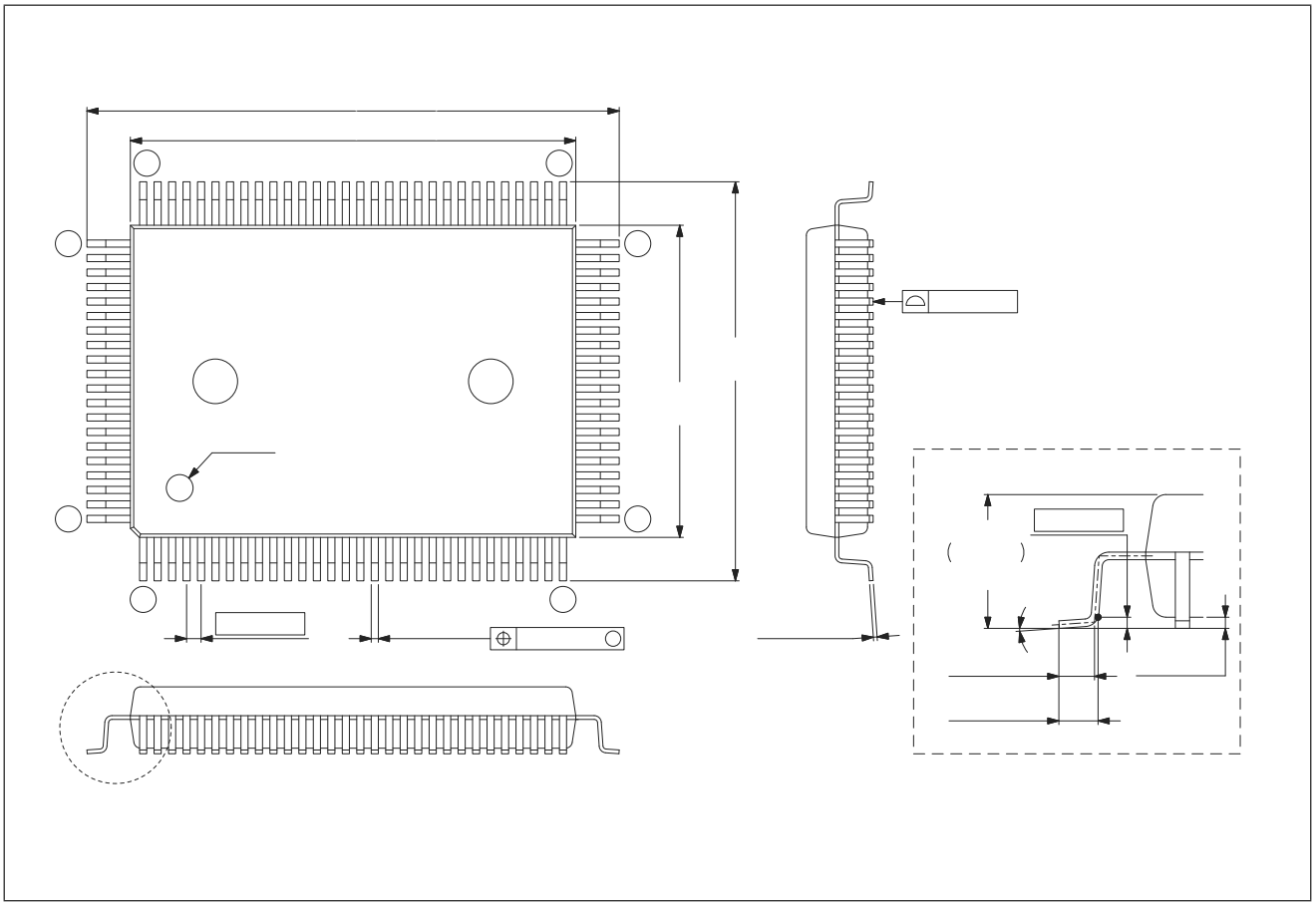
Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Conversion error	—	—	—	—	±5.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AVRL − 3.5 LSB	AVRL + 0.5 LSB	AVRL + 4.5 LSB	V	
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH − 6.5 LSB	AVRH − 1.5 LSB	AVRH + 1.5 LSB	V	
Compare time	—	—	352 t_{CP}	—	—	ns	Internal frequency : 16 MHz
Sampling time	—	—	64 t_{CP}	—	—	ns	Internal frequency : 16 MHz
Analog port input current	I_{AIN}	AN0 to AN7	−1	—	1	µA	$V_{CC} = AV_{CC} = 5.0\ V \pm 1\%$
Analog input voltage range	V_{AIN}	AN0 to AN7	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	AVRL + 2.7	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH − 2.7	V	
Power supply current	I_A	AV_{CC}	—	5	—	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage supply current	I_R	AVRH	—	400	600	µA	Flash device
			—	140	260	µA	MASK ROM
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

* : When not using an A/D converter, this is the current ($V_{CC} = AV_{CC} = AVRH = 5.0\ V$) when the CPU is stopped.

Note: The functionality of the A/D converter is only guaranteed for VCC = 5.0 V ± 10 % (also for MB90543G(S)/547G(S)/548G(S)/F548G(S)/F548GL(S)).

14. Package Dimensions



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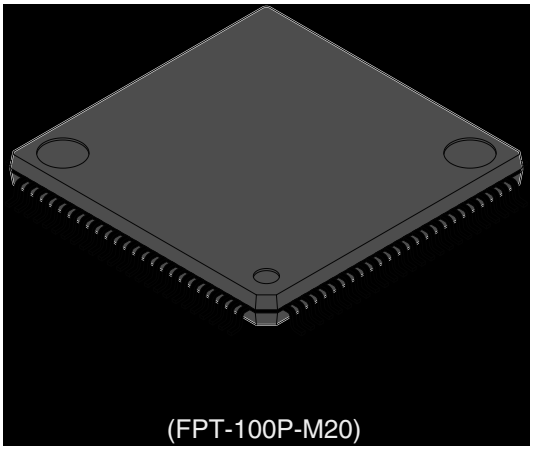

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