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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gpmc-gse1

Starting by an external trigger input.
Conversion time : 26.3 μs

- FULL-CAN interfaces
  MB90540G series : 2 channels
  MB90545G series : 1 channel
  Conforming to Version 2.0 Part A and Part B
  Flexible message buffering (mailbox and FIFO buffering can be mixed)
- External bus interface : Maximum address space 16 Mbytes
- Package: QFP-100, LQFP-100

Features	MB90F543G (S) /F548G (S) MB90F549G (S) /F546G (S) MB90F548GL(S)	MB90543G (S) MB90547G (S) MB90548G (S) MB90549G (S)	MB90V540G
16-bit Reload Timer (2 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = System clock frequency) Supports External Event Count function Signals an interrupt when overflow		
16-bit Free-run Timer	Supports Timer Clear when a match with Output Compare (Channel 0) Operation clock freq. : fsys/2^2, fsys/2^4, fsys/2^6, fsys/2^8 (fsys = System clock freq.)		
16-bit Output Compare (4 channels)	Signals an interrupt when a match with 16-bit Free-run Timer Four 16-bit compare registers A pair of compare registers can be used to generate an output signal		
16-bit Input Capture (8 channels)	Rising edge, falling edge or rising & falling edge sensitive Four 16-bit Capture registers Signals an interrupt upon external event		
8/16-bit Programmable Pulse Generator (4 channels)	Supports 8-bit and 16-bit operation modes Eight 8-bit reload counters Eight 8-bit reload registers for L pulse width Eight 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter 4 output pins Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 µs@fosc = 4 MHz (fsys = System clock frequency, fosc = Oscillation clock frequency)		
CAN Interface MB90540G series : 2 channels MB90545G series : 1 channel	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 massage buffers for data and ID's supports multipe massages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps		
32 kHz Sub-clock	Sub-clock for low power operation		
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive		
External bus interface	External access using the selectable 8-bit or 16-bit bus is enabled (external bus mode.)		
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs and schmitt trigger inputs Bit-wise programmable as input/output or peripheral signal Sub-clock for 32 kHz Sub clock low power operation		
Flash Memory	Supports automatic programming, Embeded Algorithm Write/Erase/Erase-Suspend/Erase-Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block Block protection by externally programmed voltage		

*1 : If the one clock system is used, equip X0A and X1A with clocks from the tool side.

3. Pin Description

Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
80 81	82 83	X0 X1	A (Oscillation)	High speed crystal oscillator input pins
78	80	X0A	A (Oscillation)	Low speed crystal oscillator input pins. For the one clock system parts, perfom external pull-down processing.
77	79	X1A		Low speed crystal oscillator input pins. For the one clock system parts, leave it open.
75	77	$\overline{\text{RST}}$	B	External reset request input pin
50	52	$\overline{\text{HST}}$	C	Hardware standby input pin
83 to 90	85 to 92	P00 to P07	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
91 to 98	93 to 100	P10 to P17	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		AD08 to AD15		I/O pins for 8 higher bits of the external address/data bus. This function is enabled when the external bus is enabled.
99 to 6	1 to 8	P20 to P27	I	General I/O port with programmable pullup. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to “1”.
		A16 to A23		8-bit I/O pins for A16 to A23 at the external address/data bus. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to “0”.
7	9	P30	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
8	10	P31	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		$\overline{\text{RD}}$		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.
10	12	P32	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the $\overline{\text{WR}}$/$\overline{\text{WRL}}$ pin output is disabled.
		$\overline{\text{WRL}}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{\text{WR}}$/$\overline{\text{WRL}}$ pin output are enabled. $\overline{\text{WRL}}$ is write-strobe output pin for the lower 8 bits of the data bus in 16-bit access. $\overline{\text{WR}}$ is write-strobe output pin for the 8 bits of the data bus in 8-bit access.
		$\overline{\text{WR}}$		

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Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
11	13	P33	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode, external bus 8-bit mode or when WRH pin output is disabled.
		$\overline{\text{WRH}}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{\text{WRH}}$ output pin is enabled.
12	14	P34	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.
13	15	P35	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.
14	16	P36	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.
		RDY		Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.
15	17	P37	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the CLK output is disabled.
		CLK		CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled.
16	18	P40	G	General I/O port. This function is enabled when UART0 disables the serial data output.
		SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.
17	19	P41	G	General I/O port. This function is enabled when UART0 disables serial clock output.
		SCK0		Serial clock I/O pin for UART0. This function is enabled when UART0 enables the serial clock output.
18	20	P42	G	General I/O port. This function is always enabled.
		SIN0		Serial data input pin for UART0. Set the corresponding Port Direction Register to input if this function is used.
19	21	P43	G	General I/O port. This function is always enabled.
		SIN1		Serial data input pin for UART1. Set the corresponding Port Direction Register to input if this function is used.

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Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
72	74	P95	D	General I/O port. This function is always enabled.
		RX0		RX input pin for CAN0 Interface. When the CAN function is used, output from the other functions must be stopped.
73	75	P96	D	General I/O port. This function is enabled when CAN1 disables the output.
		TX1		TX output pin for CAN1. This function is enabled when CAN1 enables the output (only MB90540G series) .
74	76	P97	D	General I/O port. This function is always enabled.
		RX1		RX input pin for CAN1 Interface. When the CAN function is used, output from the other functions must be stopped (only MB90540G series) .
76	78	PA0	D	General I/O port. This function is always enabled.
32	34	AV_{CC}	Power supply	Power supply pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AV_{CC} is applied to V_{CC}.
35	37	AV_{SS}	Power supply	Power supply pin for the A/D Converter.
33	35	AVRH	Power supply	External reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV_{CC}.
34	36	AVRL	Power supply	External reference voltage input pin for the A/D Converter.
47, 48	49, 50	MD0, MD1	C	Input pins for specifying the operating mode. The pins must be directly connected to V_{CC} or V_{SS}.
49	51	MD2	F	Input pin for specifying the operating mode. The pin must be directly connected to V_{CC} or V_{SS}.
25	27	C	—	Power supply stabilization capacitor pin. It should be connected externally to an 0.1 µF ceramic capacitor.
21, 82	23, 84	V_{CC}	Power supply	Input pin for power supply (5.0 V) .
9, 40, 79	11, 42, 81	V_{SS}	Power supply	Input pin for power supply (0.0 V) .

*1 : FPT-100P-M06

*2 : FPT-100P-M20

5. Handling Devices

(1) Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS}.
- The AVcc power supply is applied before the V_{CC} voltage.

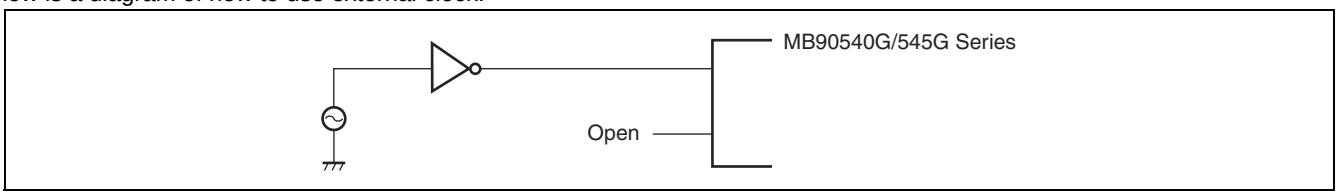
Latch-up may increase the power supply current drastically, causing thermal damage to the device.
For the same reason, care must also be taken in not allowing the analog power-supply voltage (AV_{CC}, AVRH) to exceed the digital power-supply voltage.

(2) Handling unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefor they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.
Unused bi-directional pins should be set to the output state and can be left open, or the input state with the above described connection.

(3) Using external clock

To use external clock, drive X0 pin only and leave X1 pin unconnected.
Below is a diagram of how to use external clock.

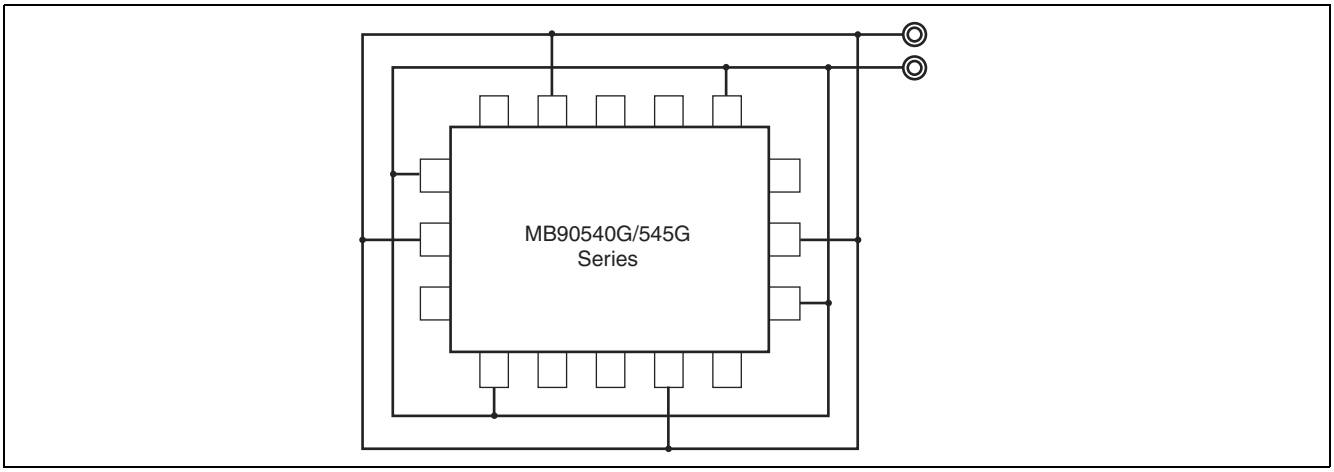


(4) Use of the sub-clock

Use one clock system parts when the sub-clock is not used. In that case, pull-down the pin X0A and leave the pin X1A open. When using two clock system parts, a 32 kHz oscillator has to be connected to the X0A and X1A pins.

(5) Power supply pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.
Make sure to connect V_{CC} and V_{SS} pins via the lowest impedance to power lines.
It is recommended to provide a bypass capacitor of around 0.1 μF between V_{CC} and V_{SS} pins near the device.



(6) Pull-up/down resistors

The MB90540G/545G Series does not support internal pull-up/down resistors (except Port0 − Port3 : pull-up resistors) . Use external components where needed.

(7) Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via the shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuits do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation.

(8) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}) .

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable) .

(9) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

(10) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

(11) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μs or more (0.2 V to 2.7 V) .

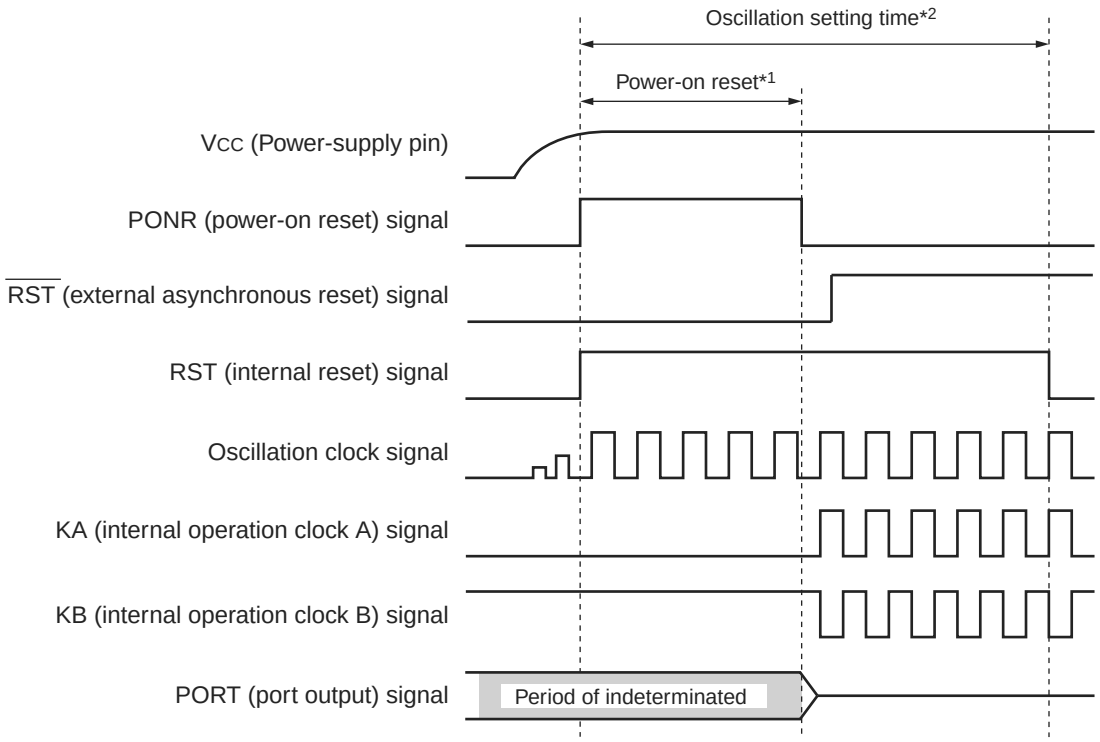
(12) Indeterminate outputs from ports 0 and 1 (MB90V540G only)

During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

- If $\overline{RST}$ pin is “H”, the outputs become indeterminate.
- If $\overline{RST}$ pin is “L”, the outputs become high-impedance.

Pay attention to the port output timing shown as follow.

- $\overline{RST}$ pin is “H”



*1 : Power-on reset time : “Period of clock frequency” × 2^{17} (Clock frequency of 16 MHz : 8.19 ms)

*2 : Oscillation setting time : “Period of clock frequency” × 2^{18} (Clock frequency of 16 MHz : 16.38 ms)

8. I/O Map

Address	Register	Abbreviation	Access	Resource name	Initial value
00_H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX$_B$
01_H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX$_B$
02_H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX$_B$
03_H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX$_B$
04_H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX$_B$
05_H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX$_B$
06_H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX$_B$
07_H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXX$_B$
08_H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX$_B$
09_H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX$_B$
$0A_H$	Port A data register	PDRA	R/W	Port A	_ _ _ _ _ _ _X$_B$
$0B_H$ to $0F_H$	Reserved				
10_H	Port 0 direction register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0$_B$
11_H	Port 1 direction register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0$_B$
12_H	Port 2 direction register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0$_B$
13_H	Port 3 direction register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0$_B$
14_H	Port 4 direction register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0$_B$
15_H	Port 5 direction register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0$_B$
16_H	Port 6 direction register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0$_B$
17_H	Port 7 direction register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0$_B$
18_H	Port 8 direction register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0$_B$
19_H	Port 9 direction register	DDR9	R/W	Port 9	0 0 0 0 0 0 0 0$_B$
$1A_H$	Port A direction register	DDRA	R/W	Port A	_ _ _ _ _ _ _0$_B$
$1B_H$	Analog Input Enable register	ADER	R/W	Port 6, A/D	1 1 1 1 1 1 1 1$_B$
$1C_H$	Port 0 Pullup control register	PUCR0	R/W	Port 0	0 0 0 0 0 0 0 0$_B$
$1D_H$	Port 1 Pullup control register	PUCR1	R/W	Port 1	0 0 0 0 0 0 0 0$_B$
$1E_H$	Port 2 Pullup control register	PUCR2	R/W	Port 2	0 0 0 0 0 0 0 0$_B$
$1F_H$	Port 3 Pullup control register	PUCR3	R/W	Port 3	0 0 0 0 0 0 0 0$_B$
20_H	Serial Mode Control Register 0	UMC0	R/W	UART0	0 0 0 0 0 1 0 0$_B$
21_H	Serial Status Register 0	USR0	R/W		0 0 0 1 0 0 0 0$_B$
22_H	Serial input data register 0/ Serial output data register 0	UIDR0/UODR0	R/W		XXXXXXXX$_B$
23_H	Rate and data register 0	URD0	R/W		0 0 0 0 0 0 0X$_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
$A2_H$ to $A4_H$	Prohibited				
$A5_H$	Automatic ready function select register	ARSR	W	External Memory Access	0 0 1 1 _ _ 0 0_B
$A6_H$	External address output control register	HACR	W		0 0 0 0 0 0 0 0_B
$A7_H$	Bus control signal selection register	ECSR	W		0 0 0 0 0 0 0 $_B$
$A8_H$	Watchdog Timer control register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1_B
$A9_H$	Time Base Timer Control register	TBTC	R/W	Time Base Timer	1 - - 0 0 1 0 0_B
AA_H	Watch timer control register	WTC	R/W	Watch Timer	1 X 0 0 0 0 0 0_B
AB_H to AD_H	Prohibited				
AE_H	Flash memory control status register (Flash only, otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0_B
AF_H	Prohibited				
$B0_H$	Interrupt control register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1_B
$B1_H$	Interrupt control register 01	ICR01	R/W		0 0 0 0 0 1 1 1_B
$B2_H$	Interrupt control register 02	ICR02	R/W		0 0 0 0 0 1 1 1_B
$B3_H$	Interrupt control register 03	ICR03	R/W		0 0 0 0 0 1 1 1_B
$B4_H$	Interrupt control register 04	ICR04	R/W		0 0 0 0 0 1 1 1_B
$B5_H$	Interrupt control register 05	ICR05	R/W		0 0 0 0 0 1 1 1_B
$B6_H$	Interrupt control register 06	ICR06	R/W		0 0 0 0 0 1 1 1_B
$B7_H$	Interrupt control register 07	ICR07	R/W		0 0 0 0 0 1 1 1_B
$B8_H$	Interrupt control register 08	ICR08	R/W		0 0 0 0 0 1 1 1_B
$B9_H$	Interrupt control register 09	ICR09	R/W		0 0 0 0 0 1 1 1_B
BA_H	Interrupt control register 10	ICR10	R/W		0 0 0 0 0 1 1 1_B
BB_H	Interrupt control register 11	ICR11	R/W		0 0 0 0 0 1 1 1_B
BC_H	Interrupt control register 12	ICR12	R/W		0 0 0 0 0 1 1 1_B
BD_H	Interrupt control register 13	ICR13	R/W		0 0 0 0 0 1 1 1_B
BE_H	Interrupt control register 14	ICR14	R/W		0 0 0 0 0 1 1 1_B
BF_H	Interrupt control register 15	ICR15	R/W		0 0 0 0 0 1 1 1_B
$C0_H$ to FF_H	External				

Address	Register	Abbreviation	Access	Resource name	Initial value
$1FF0_H$	Program address detection register 0	PADR0	R/W	Address Match Detection Function	$XXXXXXXX_B$
$1FF1_H$	Program address detection register 0	PADR0	R/W		$XXXXXXXX_B$
$1FF2_H$	Program address detection register 0	PADR0	R/W		$XXXXXXXX_B$
$1FF3_H$	Program address detection register 1	PADR1	R/W		$XXXXXXXX_B$
$1FF4_H$	Program address detection register 1	PADR1	R/W		$XXXXXXXX_B$
$1FF5_H$	Program address detection register 1	PADR1	R/W		$XXXXXXXX_B$

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A3C$_H$	003C3C$_H$	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX$_B$
003A3D$_H$	003C3D$_H$				
003A3E$_H$	003C3E$_H$				XXXXX--- XXXXXXXX$_B$
003A3F$_H$	003C3F$_H$				
003A40$_H$	003C40$_H$	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX$_B$
003A41$_H$	003C41$_H$				
003A42$_H$	003C42$_H$				XXXXX--- XXXXXXXX$_B$
003A43$_H$	003C43$_H$				
003A44$_H$	003C44$_H$	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX$_B$
003A45$_H$	003C45$_H$				
003A46$_H$	003C46$_H$				XXXXX--- XXXXXXXX$_B$
003A47$_H$	003C47$_H$				
003A48$_H$	003C48$_H$	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX$_B$
003A49$_H$	003C49$_H$				
003A4A$_H$	003C4A$_H$				XXXXX--- XXXXXXXX$_B$
003A4B$_H$	003C4B$_H$				
003A4C$_H$	003C4C$_H$	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX$_B$
003A4D$_H$	003C4D$_H$				
003A4E$_H$	003C4E$_H$				XXXXX--- XXXXXXXX$_B$
003A4F$_H$	003C4F$_H$				
003A50$_H$	003C50$_H$	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX$_B$
003A51$_H$	003C51$_H$				
003A52$_H$	003C52$_H$				XXXXX--- XXXXXXXX$_B$
003A53$_H$	003C53$_H$				
003A54$_H$	003C54$_H$	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX$_B$
003A55$_H$	003C55$_H$				
003A56$_H$	003C56$_H$				XXXXX--- XXXXXXXX$_B$
003A57$_H$	003C57$_H$				
003A58$_H$	003C58$_H$	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX$_B$
003A59$_H$	003C59$_H$				
003A5A$_H$	003C5A$_H$				XXXXX--- XXXXXXXX$_B$
003A5B$_H$	003C5B$_H$				
003A5C$_H$	003C5C$_H$	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX$_B$
003A5D$_H$	003C5D$_H$				
003A5E$_H$	003C5E$_H$				XXXXX--- XXXXXXXX$_B$
003A5F$_H$	003C5F$_H$				

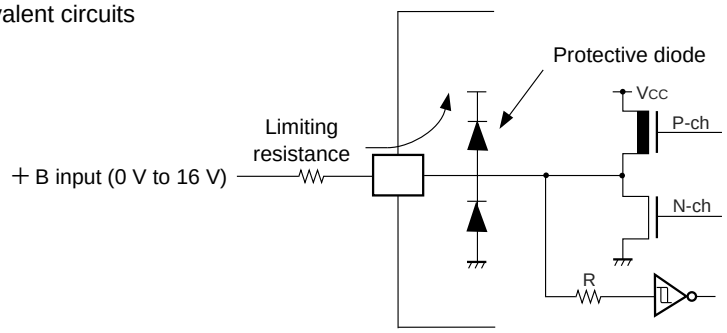
List of Message Buffers (DLC Registers and Data Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A60H	003C60H	DLC register 0	DLCR0	R/W	----XXXXB
003A61H	003C61H				
003A62H	003C62H	DLC register 1	DLCR1	R/W	----XXXXB
003A63H	003C63H				
003A64H	003C64H	DLC register 2	DLCR2	R/W	----XXXXB
003A65H	003C65H				
003A66H	003C66H	DLC register 3	DLCR3	R/W	----XXXXB
003A67H	003C67H				
003A68H	003C68H	DLC register 4	DLCR4	R/W	----XXXXB
003A69H	003C69H				
003A6AH	003C6AH	DLC register 5	DLCR5	R/W	----XXXXB
003A6BH	003C6BH				
003A6CH	003C6CH	DLC register 6	DLCR6	R/W	----XXXXB
003A6DH	003C6DH				
003A6EH	003C6EH	DLC register 7	DLCR7	R/W	----XXXXB
003A6FH	003C6FH				
003A70H	003C70H	DLC register 8	DLCR8	R/W	----XXXX
003A71H	003C71H				
003A72H	003C72H	DLC register 9	DLCR9	R/W	----XXXXB
003A73H	003C73H				
003A74H	003C74H	DLC register 10	DLCR10	R/W	----XXXXB
003A75H	003C75H				
003A76H	003C76H	DLC register 11	DLCR11	R/W	----XXXXB
003A77H	003C77H				
003A78H	003C78H	DLC register 12	DLCR12	R/W	----XXXXB
003A79H	003C79H				
003A7AH	003C7AH	DLC register 13	DLCR13	R/W	----XXXXB
003A7BH	003C7BH				
003A7CH	003C7CH	DLC register 14	DLCR14	R/W	----XXXXB
003A7DH	003C7DH				
003A7EH	003C7EH	DLC register 15	DLCR15	R/W	----XXXXB
003A7FH	003C7FH				
003A80H to 003A87H	003C80H to 003C87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB

(Continued)

- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept + B signal input.
- Sample recommended circuits :

■ Input/Output Equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

11.2 Recommended Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value			Units	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.5	5.0	5.5	V	Under normal operation : Other than MB90F548GL(S)/543G(S)/547G(S)/548G(S)
						Under normal operation when A/D conveter is used : MB90F548GL(S)/543G(S)/547G(S)/548G(S)
		3.5	5.0	5.5	V	Under normal operation when A/D conveter is not used : MB90F548GL(S)/543G(S)/547G(S)/548G(S)
		3.0	−	5.5	V	Maintain RAM data in stop mode
Smooth capacitor	C_S	0.022	0.1	1.0	µF	*
Operating temperature	T_A	−40	−	+105	°C	

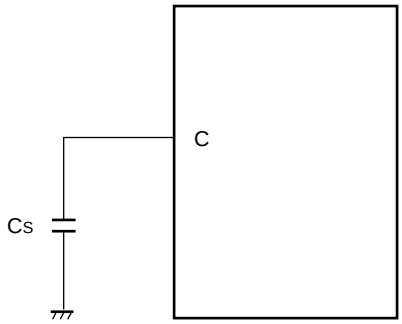
*: Use a ceramic capacitor or a capacitor of better 4. AC characteristics. The bypass capacitor should be greater than this capacitor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ **C Pin Connection Diagram**



11.4 AC Characteristics

11.4.1 Clock Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Oscillation frequency	f_C	X0, X1	3	—	16	MHz	No multiplier When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			8	—	16	MHz	PLL multiplied by 1 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			4	—	8	MHz	PLL multiplied by 2 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			3	—	5.33	MHz	PLL multiplied by 3 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			3	—	4	MHz	PLL multiplied by 4 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			3	—	5	MHz	When using an oscillator circuit V_{CC} < 4.5 V(MB90F548GL(S)/543G(S)/547G(S)/548G(S))
			3	—	16	MHz	No multiplier When using an external clock
			8	—	16	MHz	PLL multiplied by 1 When using an external clock
			4	—	8	MHz	PLL multiplied by 2 When using an external clock
			3	—	5.33	MHz	PLL multiplied by 3 When using an external clock
			3	—	4	MHz	PLL multiplied by 4 When using an external clock
	f_{CL}	X0A, X1A	—	32.768	—	kHz	

(Continued)

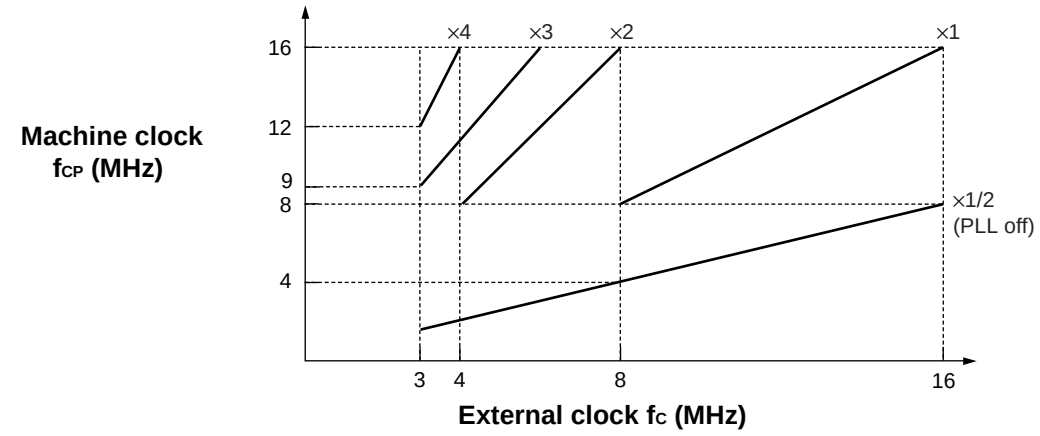
(Continued)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

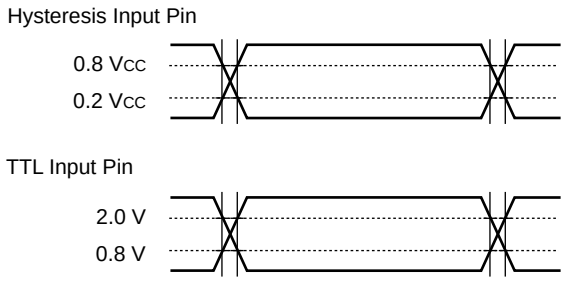
Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	No multiplier When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			62.5	—	125	ns	PLL multiplied by 1 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			125	—	250	ns	PLL multiplied by 2 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			187.5	—	333	ns	PLL multiplied by 3 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			250	—	333	ns	PLL multiplied by 4 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			200	—	333	ns	When using an oscillator circuit V_{CC} < 4.5 V(MB90F548GL(S)/543G(S)/547G(S)/548G(S))
			62.5	—	333	ns	No multiplier When using an external clock
			62.5	—	125	ns	PLL multiplied by 1 When using an external clock
			125	—	250	ns	PLL multiplied by 2 When using an external clock
			187.5	—	333	ns	PLL multiplied by 3 When using an external clock
			250	—	333	ns	PLL multiplied by 4 When using an external clock
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WLH}, P_{WLL}	X0A	—	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using an external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	When using main clock
	f_{LCP}	—	—	8.192	—	kHz	When using sub-clock
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	When using main clock
	t_{LCP}	—	—	122.1	—	µs	When using sub-clock

■ **External clock frequency and Machine clock frequency**

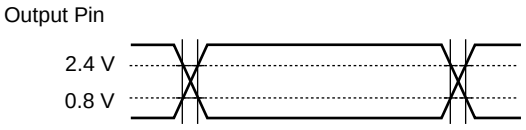


AC characteristics are set to the measured reference voltage values below.

■ **Input signal waveform**



■ **Output signal waveform**



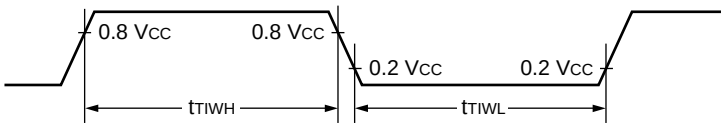
11.4.10 Timer Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	4 t_{CP}	—	ns	
	t_{TIWL}	IN0 to IN7					

■ **Timer Input Timing**



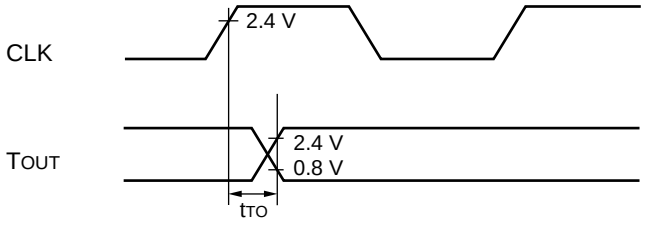
11.4.11 Timer Output Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
CLK↑ → T_{OUT} change time	t_{TO}	TOT0 , TOT1, PPG0 to PPG3	—	30	—	ns	

■ **Timer Output Timing**



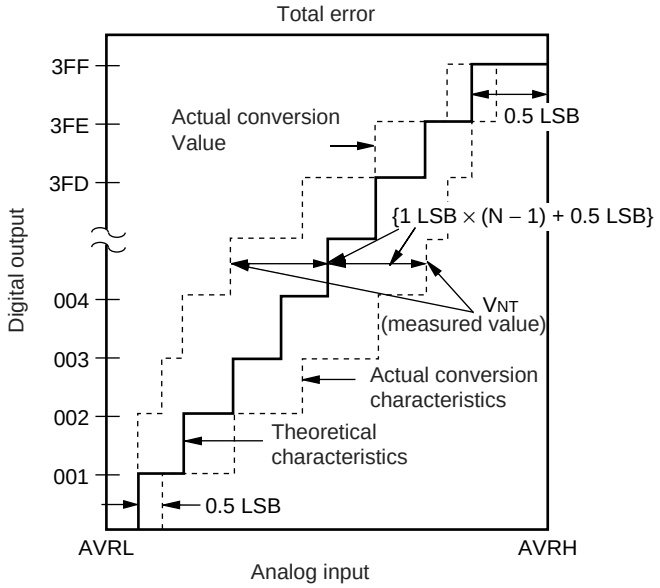
11.5.2 A/D Converter Glossary

Resolution : Analog changes that are identifiable with the A/D converter

Linearity error : The deviation of the straight line connecting the zero transition point (“00 0000 0000” ⟷ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ⟷ “11 1111 1111”) from actual conversion characteristics

Differential linearity error : The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error : The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1\,\text{LSB} = (\text{Theoretical value})\,\frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

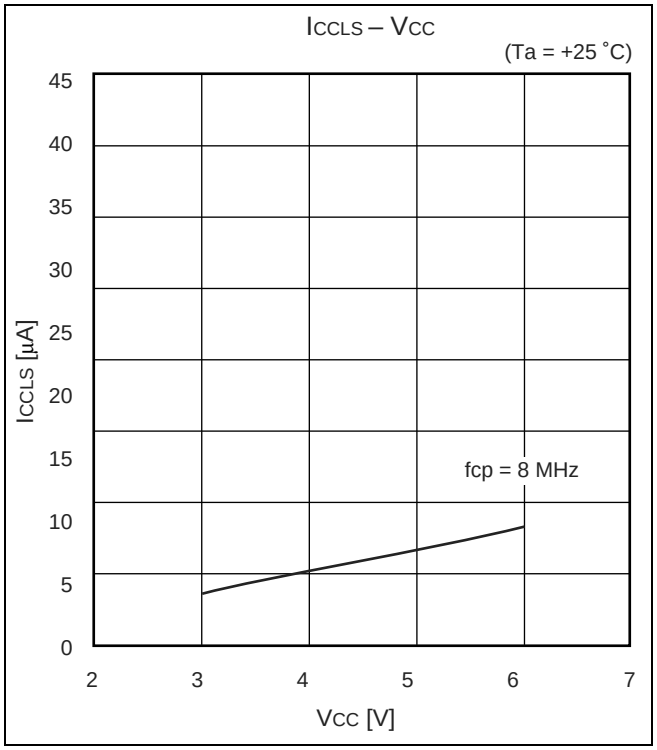
$$V_{OT}\ (\text{Theoretical value}) = \text{AVRL} + 0.5\ \text{LSB}\ [\text{V}]$$

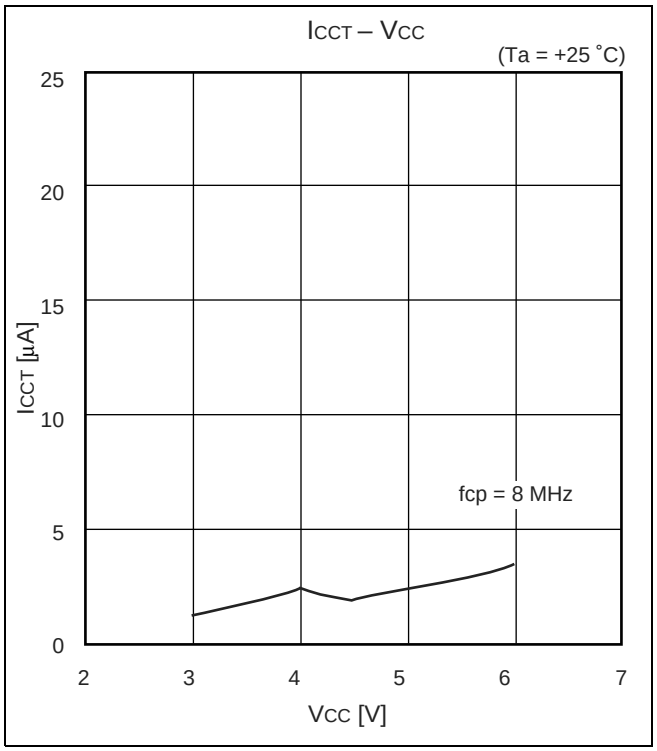
$$V_{FST}\ (\text{Theoretical value}) = \text{AVRH} - 1.5\ \text{LSB}\ [\text{V}]$$

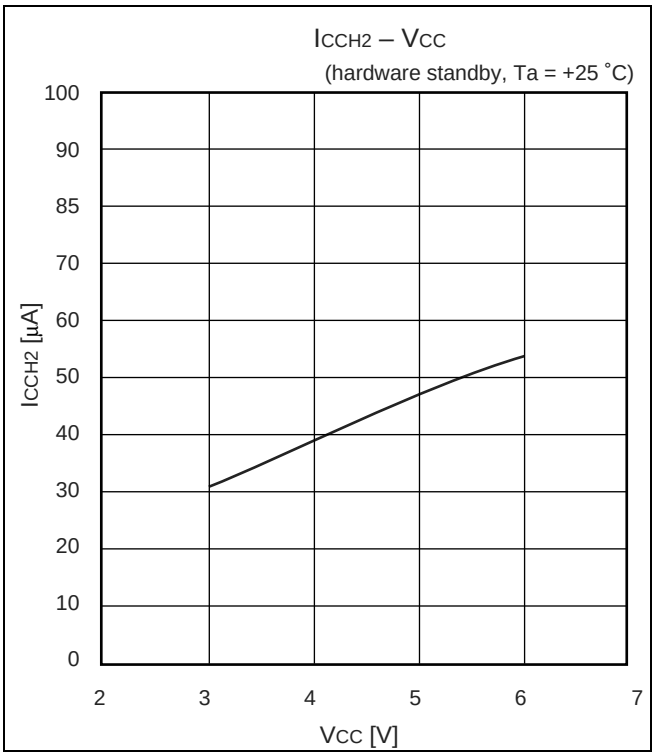
$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (\text{N} - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

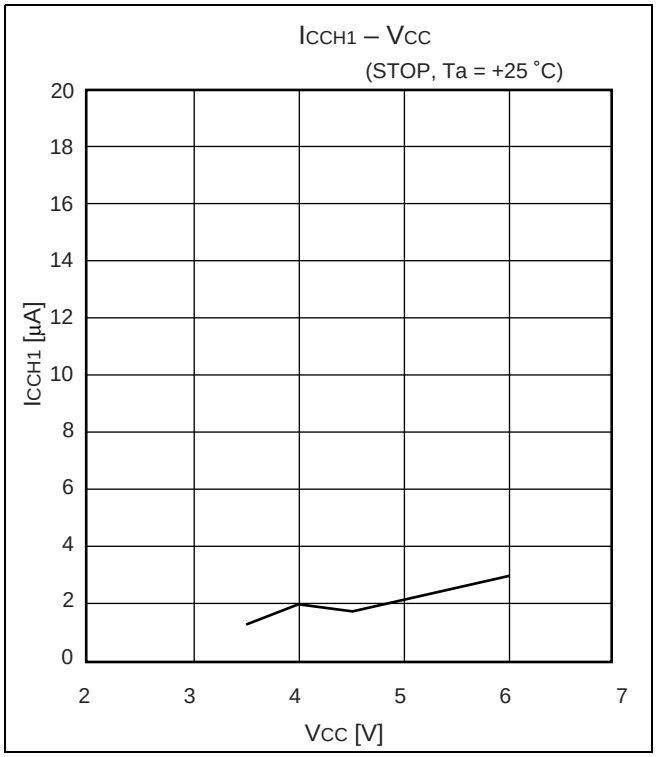
V_{NT} : Voltage at a transition of digital output from (N − 1) to N

(Continued)


ICCLS – VCC
(Ta = +25 ˚C)
ICCLS [µA]
45
40
35
30
25
20
15
10
5
0
fcp = 8 MHz
2
3
4
5
6
7
VCC [V]


ICCT – VCC
(Ta = +25 ˚C)
ICCT [µA]
25
20
15
10
5
0
fcp = 8 MHz
2
3
4
5
6
7
VCC [V]


ICCH2 – VCC
(hardware standby, Ta = +25 ˚C)
ICCH2 [µA]
100
90
85
70
60
50
40
30
20
10
0
2
3
4
5
6
7
VCC [V]


ICCH1 – VCC
(STOP, Ta = +25 ˚C)
ICCH1 [µA]
20
18
16
14
12
10
8
6
4
2
0
2
3
4
5
6
7
VCC [V]