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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspf-g

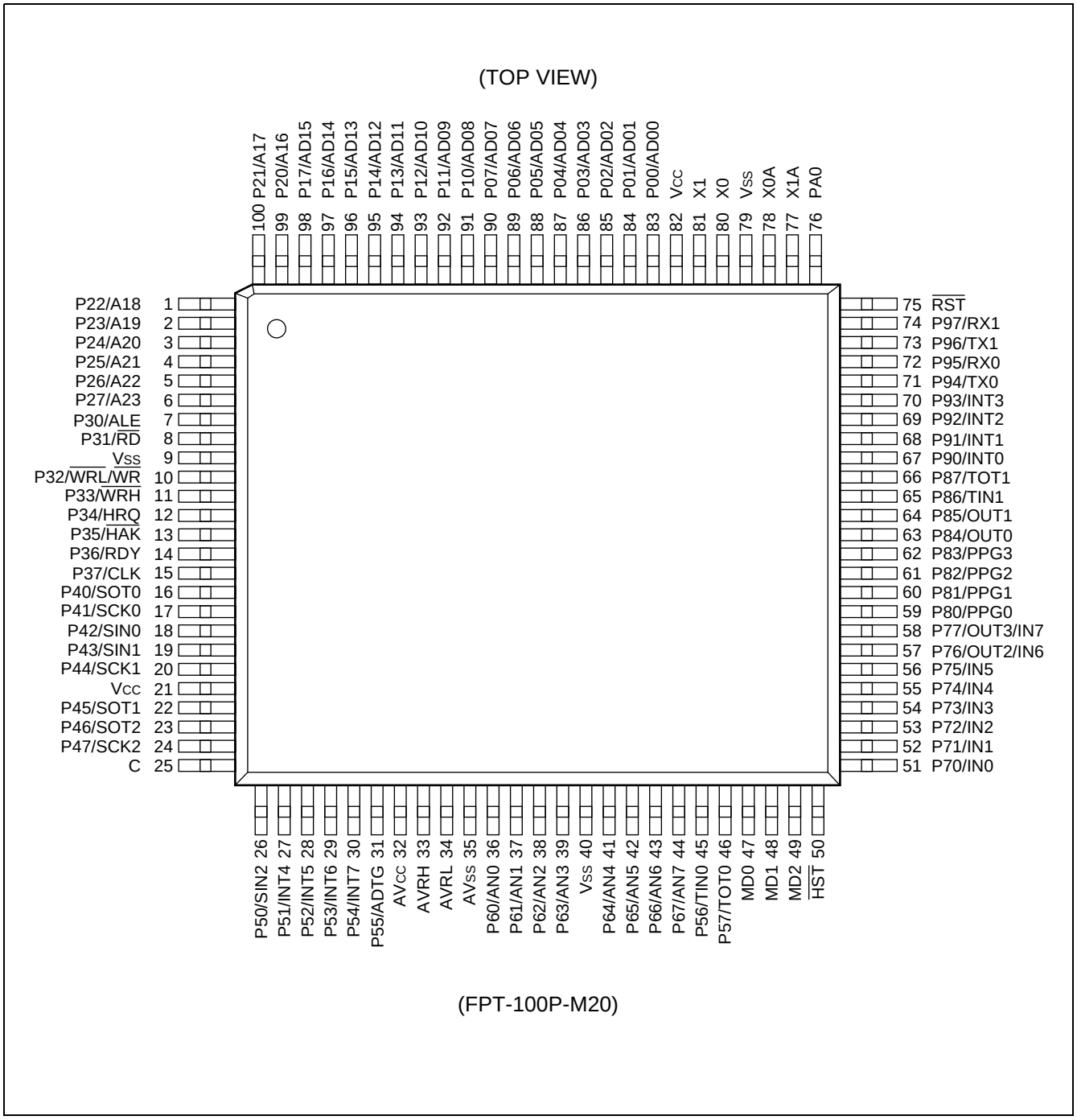
Starting by an external trigger input.
Conversion time : 26.3 μs

- FULL-CAN interfaces
  MB90540G series : 2 channels
  MB90545G series : 1 channel
  Conforming to Version 2.0 Part A and Part B
  Flexible message buffering (mailbox and FIFO buffering can be mixed)
- External bus interface : Maximum address space 16 Mbytes
- Package: QFP-100, LQFP-100

*2 : It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*3 : Operating Voltage Range

Products	Operation guarantee range
MB90F543G(S)/F546G(S)/F548G(S)/ MB90549G(S)/F549G(S)/V540/V540G	4.5 V to 5.5 V
MB90F548GL(S)/543G(S)/547G(S)/548G(S)	3.5 V to 5.5 V


(TOP VIEW)
100 P21/A17
99 P20/A16
98 P17/AD15
97 P16/AD14
96 P15/AD13
95 P14/AD12
94 P13/AD11
93 P12/AD10
92 P11/AD09
91 P10/AD08
90 P07/AD07
89 P06/AD06
88 P05/AD05
87 P04/AD04
86 P03/AD03
85 P02/AD02
84 P01/AD01
83 P00/AD00
82 VCC
81 X1
80 X0
79 VSS
78 X0A
77 X1A
76 PA0
P22/A18 1
P23/A19 2
P24/A20 3
P25/A21 4
P26/A22 5
P27/A23 6
P30/ALE 7
P31/RD 8
VSS 9
P32/WRL/WR 10
P33/WRH 11
P34/HRQ 12
P35/HAK 13
P36/RDY 14
P37/CLK 15
P40/SOT0 16
P41/SCK0 17
P42/SIN0 18
P43/SIN1 19
P44/SCK1 20
VCC 21
P45/SOT1 22
P46/SOT2 23
P47/SCK2 24
C 25
75 RST
74 P97/RX1
73 P96/TX1
72 P95/RX0
71 P94/TX0
70 P93/INT3
69 P92/INT2
68 P91/INT1
67 P90/INT0
66 P87/TOT1
65 P86/TIN1
64 P85/OUT1
63 P84/OUT0
62 P83/PPG3
61 P82/PPG2
60 P81/PPG1
59 P80/PPG0
58 P77/OUT3/IN7
57 P76/OUT2/IN6
56 P75/IN5
55 P74/IN4
54 P73/IN3
53 P72/IN2
52 P71/IN1
51 P70/IN0
P50/SIN2 26
P51/INT4 27
P52/INT5 28
P53/INT6 29
P54/INT7 30
P55/ADTG 31
AVCC 32
AVRH 33
AVRL 34
AVSS 35
P60/AN0 36
P61/AN1 37
P62/AN2 38
P63/AN3 39
VSS 40
P64/AN4 41
P65/AN5 42
P66/AN6 43
P67/AN7 44
P56/TIN0 45
P57/TOT0 46
MD0 47
MD1 48
MD2 49
HST 50

(FPT-100P-M20)

3. Pin Description

Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
80 81	82 83	X0 X1	A (Oscillation)	High speed crystal oscillator input pins
78	80	X0A	A (Oscillation)	Low speed crystal oscillator input pins. For the one clock system parts, perfom external pull-down processing.
77	79	X1A		Low speed crystal oscillator input pins. For the one clock system parts, leave it open.
75	77	$\overline{\text{RST}}$	B	External reset request input pin
50	52	$\overline{\text{HST}}$	C	Hardware standby input pin
83 to 90	85 to 92	P00 to P07	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
91 to 98	93 to 100	P10 to P17	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		AD08 to AD15		I/O pins for 8 higher bits of the external address/data bus. This function is enabled when the external bus is enabled.
99 to 6	1 to 8	P20 to P27	I	General I/O port with programmable pullup. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to “1”.
		A16 to A23		8-bit I/O pins for A16 to A23 at the external address/data bus. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to “0”.
7	9	P30	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
8	10	P31	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		$\overline{\text{RD}}$		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.
10	12	P32	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the $\overline{\text{WR}}$/$\overline{\text{WRL}}$ pin output is disabled.
		$\overline{\text{WRL}}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{\text{WR}}$/$\overline{\text{WRL}}$ pin output are enabled. $\overline{\text{WRL}}$ is write-strobe output pin for the lower 8 bits of the data bus in 16-bit access. $\overline{\text{WR}}$ is write-strobe output pin for the 8 bits of the data bus in 8-bit access.
		$\overline{\text{WR}}$		

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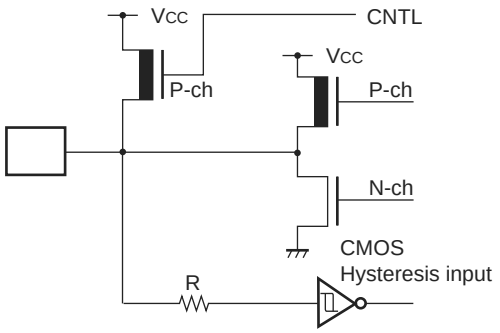
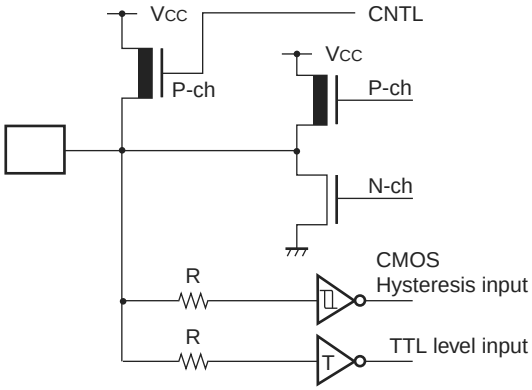
Circuit type	Diagram	Remarks
H		■ CMOS level output ■ CMOS Hysteresis input ■ Programmable pull-up resistor : 50 kΩ approx.
I		■ CMOS level output ■ CMOS Hysteresis input ■ TTL level input (Flash devices in Flash writer mode only) ■ Programmable pullup resistor : 50 kΩ approx.

(6) Pull-up/down resistors

The MB90540G/545G Series does not support internal pull-up/down resistors (except Port0 − Port3 : pull-up resistors) . Use external components where needed.

(7) Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via the shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuits do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation.

(8) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}) .

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable) .

(9) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

(10) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

(11) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μs or more (0.2 V to 2.7 V) .

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
3928H	Output Compare Register 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
3929H	Output Compare Register 0	OCCP0	R/W		XXXXXXXXB
392AH	Output Compare Register 1	OCCP1	R/W		XXXXXXXXB
392BH	Output Compare Register 1	OCCP1	R/W		XXXXXXXXB
392CH	Output Compare Register 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXXB
392DH	Output Compare Register 2	OCCP2	R/W		XXXXXXXXB
392EH	Output Compare Register 3	OCCP3	R/W		XXXXXXXXB
392FH	Output Compare Register 3	OCCP3	R/W		XXXXXXXXB
3930H to 39FFH	Reserved				
3A00H to 3AFFH	Reserved for CAN 0 Interface.				
3B00H to 3BFFH	Reserved for CAN 0 Interface.				
3C00H to 3CFFH	Reserved for CAN 1 Interface.				
3D00H to 3DFFH	Reserved for CAN 1 Interface.				
3E00H to 3FFFH	Reserved				

- Read/write notation
  - R/W : Reading and writing permitted
  - R : Read-only
  - W : Write-only

- Initial value notation
  - 0 : Initial value is “0”.
  - 1 : Initial value is “1”.
  - X : Initial value is undefined.
  - _ : Initial value is unused.

Note: Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

9. CAN Controller

The MB90540G series contains two CAN controllers (CAN0 and CAN1) , the MB90545G series contains only one (CAN0) . The Evaluation Chip MB90V540G also has two CAN controllers.

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 1 Mbps (when input clock is at 16 MHz)

List of Control Registers

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070_H	000080_H	Message buffer valid register	BVALR	R/W	$00000000\ 00000000_B$
000071_H	000081_H				
000072_H	000082_H	Transmit request register	TREQR	R/W	$00000000\ 00000000_B$
000073_H	000083_H				
000074_H	000084_H	Transmit cancel register	TCANR	W	$00000000\ 00000000_B$
000075_H	000085_H				
000076_H	000086_H	Transmit complete register	TCR	R/W	$00000000\ 00000000_B$
000077_H	000087_H				
000078_H	000088_H	Receive complete register	RCR	R/W	$00000000\ 00000000_B$
000079_H	000089_H				
$00007A_H$	$00008A_H$	Remote request receiving register	RRTRR	R/W	$00000000\ 00000000_B$
$00007B_H$	$00008B_H$				
$00007C_H$	$00008C_H$	Receive overrun register	ROVRR	R/W	$00000000\ 00000000_B$
$00007D_H$	$00008D_H$				
$00007E_H$	$00008E_H$	Receive interrupt enable register	RIER	R/W	$00000000\ 00000000_B$
$00007F_H$	$00008F_H$				

(Continued)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A24H	003C24H	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXXB
003A25H	003C25H				
003A26H	003C26H				XXXXX--- XXXXXXXXB
003A27H	003C27H				
003A28H	003C28H	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXXB
003A29H	003C29H				
003A2AH	003C2AH				XXXXX--- XXXXXXXXB
003A2BH	003C2BH				
003A2CH	003C2CH	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXXB
003A2DH	003C2DH				
003A2EH	003C2EH				XXXXX--- XXXXXXXXB
003A2FH	003C2FH				
003A30H	003C30H	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXXB
003A31H	003C31H				
003A32H	003C32H				XXXXX--- XXXXXXXXB
003A33H	003C33H				
003A34H	003C34H	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXXB
003A35H	003C35H				
003A36H	003C36H				XXXXX--- XXXXXXXXB
003A37H	003C37H				
003A38H	003C38H	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXXB
003A39H	003C39H				
003A3AH	003C3AH				XXXXX--- XXXXXXXXB
003A3BH	003C3BH				

(Continued)

List of Message Buffers (DLC Registers and Data Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A60H	003C60H	DLC register 0	DLCR0	R/W	----XXXXB
003A61H	003C61H				
003A62H	003C62H	DLC register 1	DLCR1	R/W	----XXXXB
003A63H	003C63H				
003A64H	003C64H	DLC register 2	DLCR2	R/W	----XXXXB
003A65H	003C65H				
003A66H	003C66H	DLC register 3	DLCR3	R/W	----XXXXB
003A67H	003C67H				
003A68H	003C68H	DLC register 4	DLCR4	R/W	----XXXXB
003A69H	003C69H				
003A6AH	003C6AH	DLC register 5	DLCR5	R/W	----XXXXB
003A6BH	003C6BH				
003A6CH	003C6CH	DLC register 6	DLCR6	R/W	----XXXXB
003A6DH	003C6DH				
003A6EH	003C6EH	DLC register 7	DLCR7	R/W	----XXXXB
003A6FH	003C6FH				
003A70H	003C70H	DLC register 8	DLCR8	R/W	----XXXX
003A71H	003C71H				
003A72H	003C72H	DLC register 9	DLCR9	R/W	----XXXXB
003A73H	003C73H				
003A74H	003C74H	DLC register 10	DLCR10	R/W	----XXXXB
003A75H	003C75H				
003A76H	003C76H	DLC register 11	DLCR11	R/W	----XXXXB
003A77H	003C77H				
003A78H	003C78H	DLC register 12	DLCR12	R/W	----XXXXB
003A79H	003C79H				
003A7AH	003C7AH	DLC register 13	DLCR13	R/W	----XXXXB
003A7BH	003C7BH				
003A7CH	003C7CH	DLC register 14	DLCR14	R/W	----XXXXB
003A7DH	003C7DH				
003A7EH	003C7EH	DLC register 15	DLCR15	R/W	----XXXXB
003A7FH	003C7FH				
003A80H to 003A87H	003C80H to 003C87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB

(Continued)

11.4 AC Characteristics

11.4.1 Clock Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Oscillation frequency	f_C	X0, X1	3	—	16	MHz	No multiplier When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			8	—	16	MHz	PLL multiplied by 1 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			4	—	8	MHz	PLL multiplied by 2 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			3	—	5.33	MHz	PLL multiplied by 3 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			3	—	4	MHz	PLL multiplied by 4 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			3	—	5	MHz	When using an oscillator circuit V_{CC} < 4.5 V(MB90F548GL(S)/543G(S)/547G(S)/548G(S))
			3	—	16	MHz	No multiplier When using an external clock
			8	—	16	MHz	PLL multiplied by 1 When using an external clock
			4	—	8	MHz	PLL multiplied by 2 When using an external clock
			3	—	5.33	MHz	PLL multiplied by 3 When using an external clock
			3	—	4	MHz	PLL multiplied by 4 When using an external clock
	f_{CL}	X0A, X1A	—	32.768	—	kHz	

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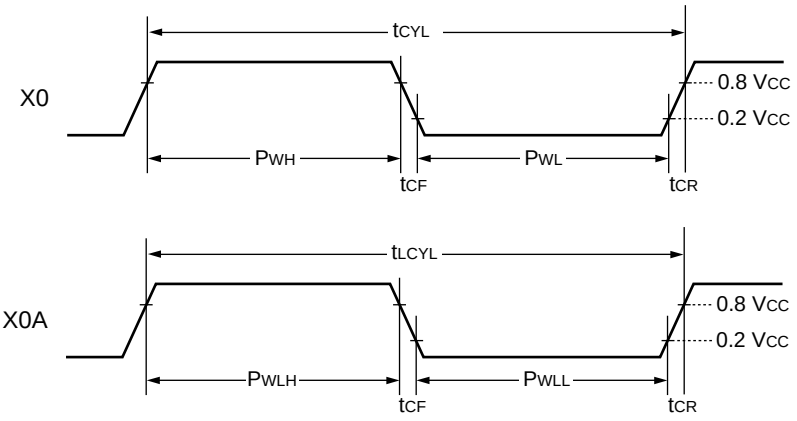
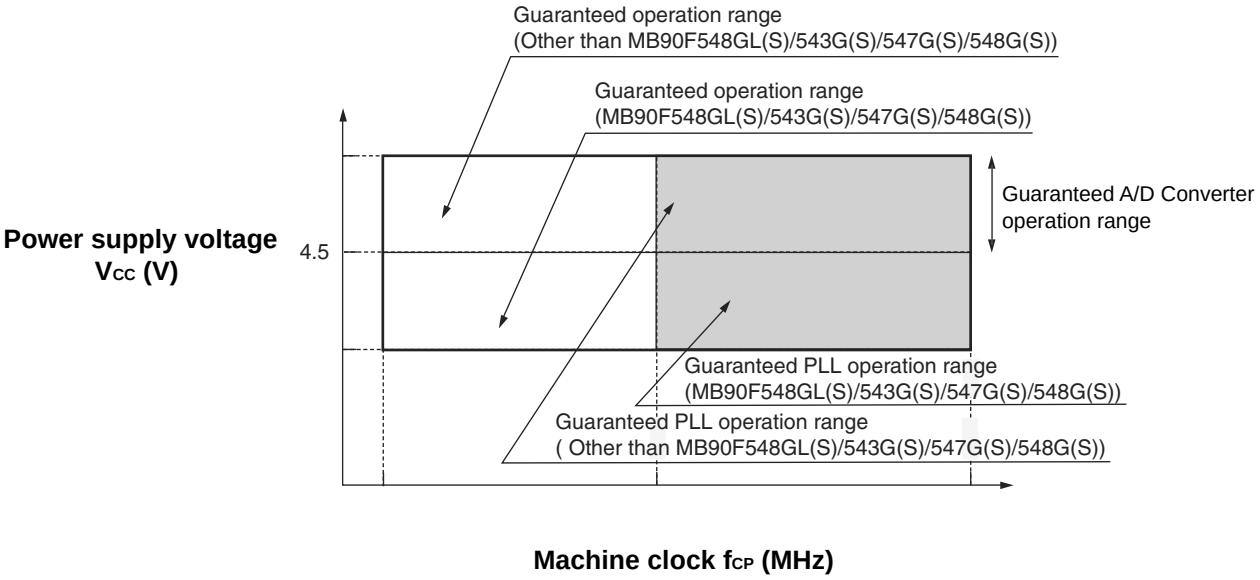
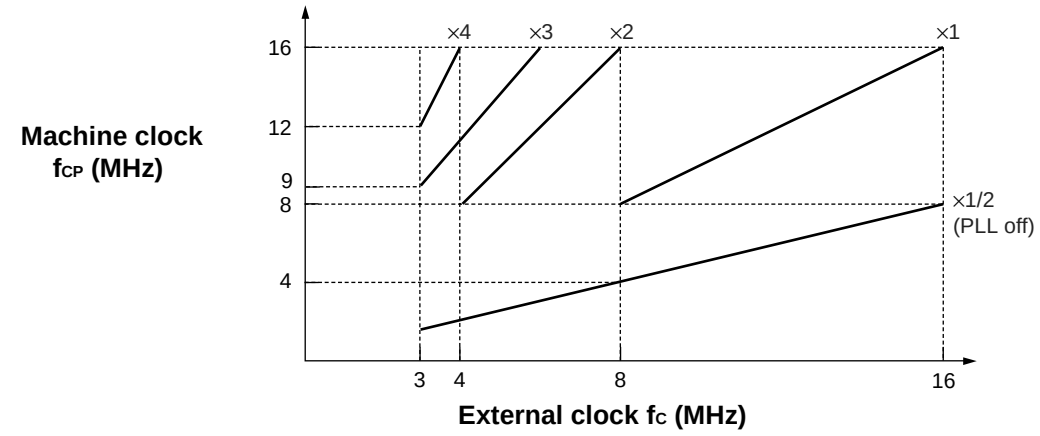
■ **Clock Timing**



■ **Guaranteed PLL operation range**

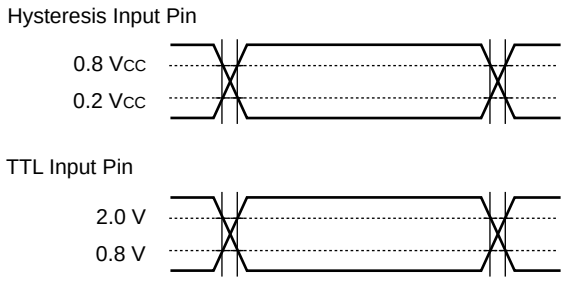


■ **External clock frequency and Machine clock frequency**

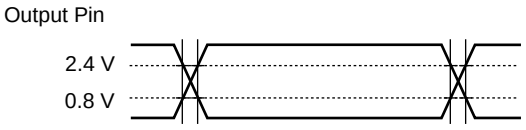


AC characteristics are set to the measured reference voltage values below.

■ **Input signal waveform**



■ **Output signal waveform**



11.4.5 Bus Timing (Read)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE		$t_{CP}/2 - 20$	−	ns	
Valid address → ALE↓ time	t_{AVLL}	ALE, A16 to A23, AD00 to AD15		$t_{CP}/2 - 20$	−	ns	
ALE↓ → Address valid time	t_{LLAX}	ALE, AD00 to AD15		$t_{CP}/2 - 15$	−	ns	
Valid address → $\overline{RD}$↓ time	t_{AVRL}	A16 toA23, AD00 to AD15, $\overline{RD}$		$t_{CP} - 15$	−	ns	
Valid address → Valid data input	t_{AVDV}	A16 to A23, AD00 to AD15		−	$5\ t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	RD	−	$3\ t_{CP}/2 - 20$	−	ns	
$\overline{RD}$↓ → Valid data input	t_{RLDV}	$\overline{RD}$, AD00 to AD15		−	$3\ t_{CP}/2 - 60$	ns	
$\overline{RD}$↑ → Data hold time	t_{RHDX}	$\overline{RD}$, AD00 to AD15		0	−	ns	
$\overline{RD}$↑ → ALE↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	−	ns	
$\overline{RD}$↑ → Address valid time	t_{RHAX}	$\overline{RD}$, A16 to A23		$t_{CP}/2 - 10$	−	ns	
Valid address → CLK↑ time	t_{AVCH}	A16 to A23, AD00 to AD15, CLK		$t_{CP}/2 - 20$	−	ns	
$\overline{RD}$↓ → CLK↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 20$	−	ns	
ALE↓ → $\overline{RD}$↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	−	ns	

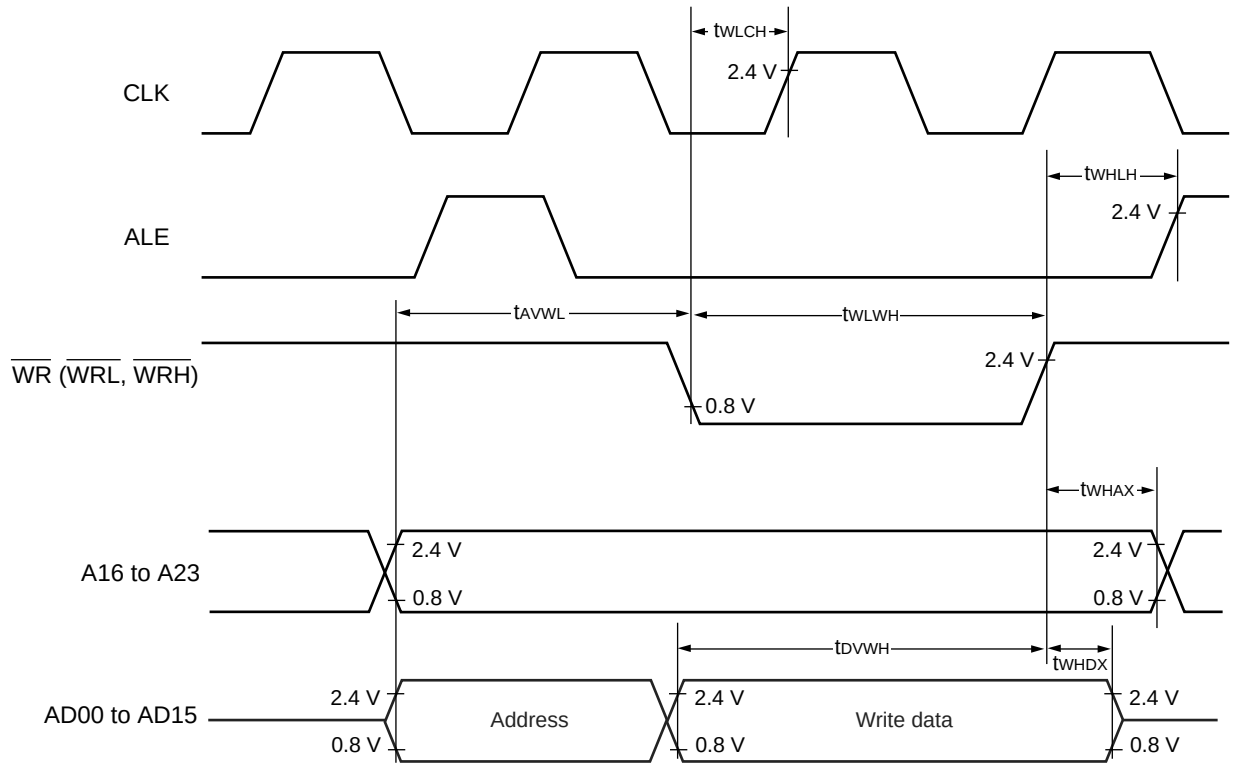
11.4.6 Bus Timing (Write)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Valid address → $\overline{WR}$↓ time	t_{AVWL}	A16 to A23 AD00 to AD15, $\overline{WR}$	—	t_{CP} − 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	WR		3 t_{CP}/2 − 20	—	ns	
Valid data output → $\overline{WR}$↑ time	t_{DVWH}	AD00 to AD15, $\overline{WR}$		3 t_{CP}/2 − 20	—	ns	
$\overline{WR}$↑ → Data hold time	t_{WHDX}	AD00 to AD15, $\overline{WR}$		20	—	ns	
$\overline{WR}$↑ → Address valid time	t_{WHAX}	A16 to A23, $\overline{WR}$		t_{CP}/2 − 10	—	ns	
$\overline{WR}$↑ → ALE↑ time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 − 15	—	ns	
$\overline{WR}$↑ → CLK↑ time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 − 20	—	ns	

■ **Bus Timing** (**Write**)



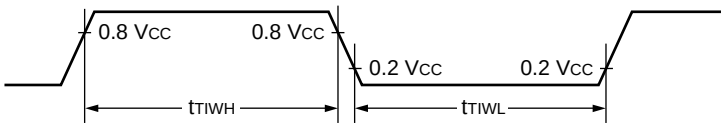
11.4.10 Timer Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	4 t_{CP}	—	ns	
	t_{TIWL}	IN0 to IN7					

■ **Timer Input Timing**



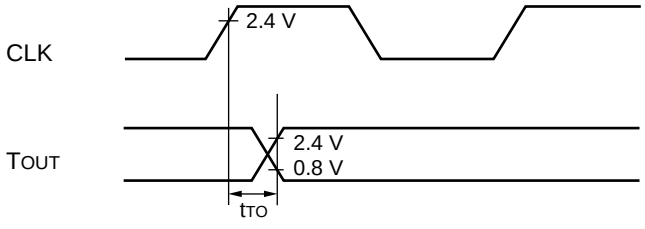
11.4.11 Timer Output Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
CLK↑ → T_{OUT} change time	t_{TO}	TOT0 , TOT1, PPG0 to PPG3	—	30	—	ns	

■ **Timer Output Timing**



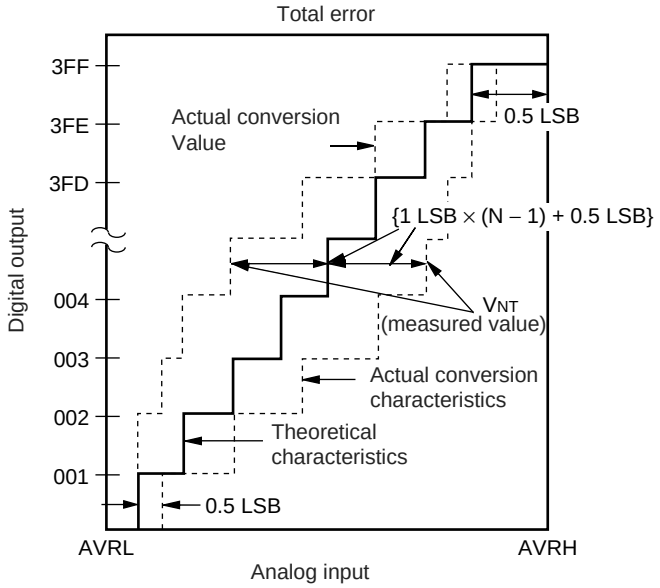
11.5.2 A/D Converter Glossary

Resolution : Analog changes that are identifiable with the A/D converter

Linearity error : The deviation of the straight line connecting the zero transition point (“00 0000 0000” ⟷ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ⟷ “11 1111 1111”) from actual conversion characteristics

Differential linearity error : The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error : The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1\,\text{LSB} = (\text{Theoretical value})\,\frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

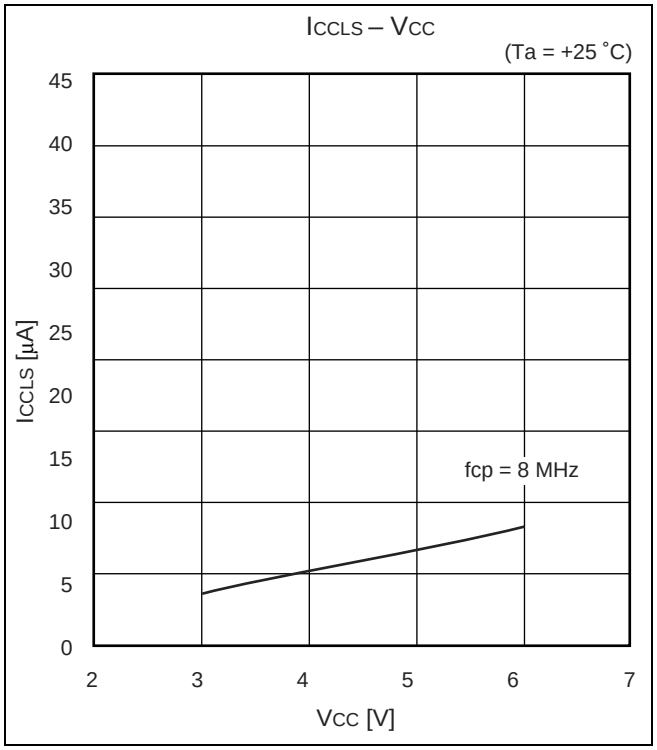
$$V_{OT}\ (\text{Theoretical value}) = \text{AVRL} + 0.5\ \text{LSB}\ [\text{V}]$$

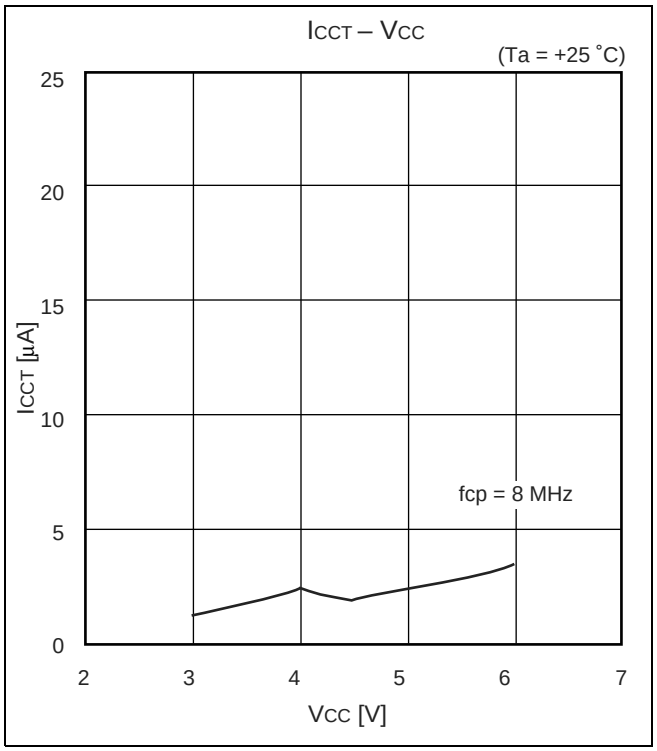
$$V_{FST}\ (\text{Theoretical value}) = \text{AVRH} - 1.5\ \text{LSB}\ [\text{V}]$$

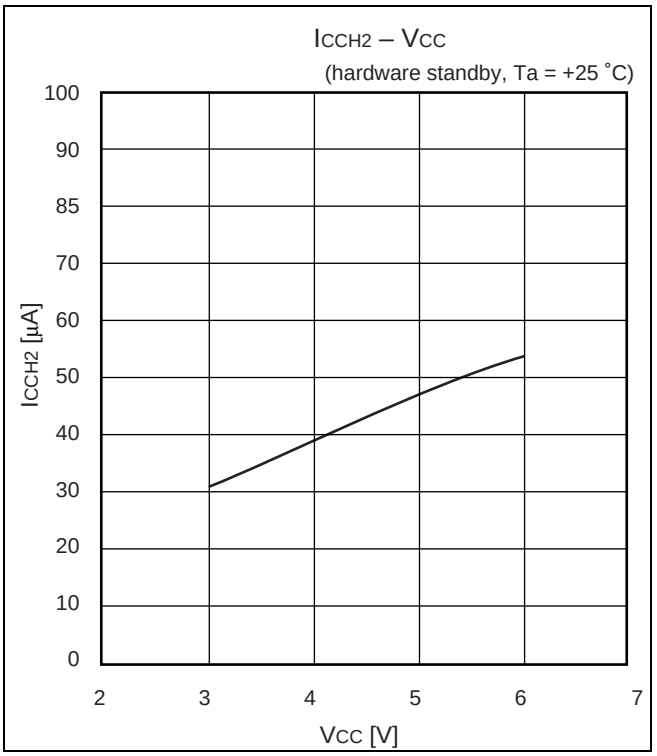
$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (\text{N} - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

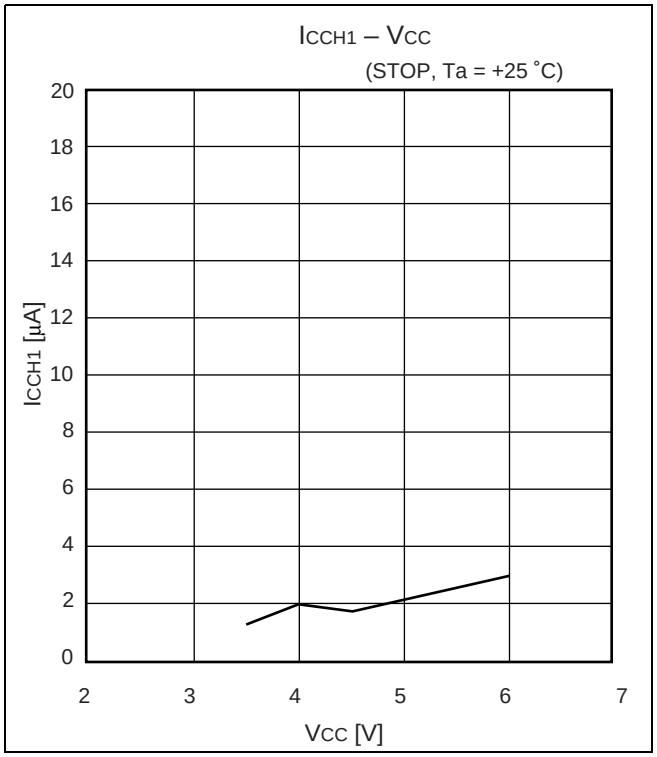
V_{NT} : Voltage at a transition of digital output from (N − 1) to N

(Continued)


ICCLS – VCC
(Ta = +25 ˚C)
ICCLS [µA]
45
40
35
30
25
20
15
10
5
0
fcp = 8 MHz
2
3
4
5
6
7
VCC [V]


ICCT – VCC
(Ta = +25 ˚C)
ICCT [µA]
25
20
15
10
5
0
fcp = 8 MHz
2
3
4
5
6
7
VCC [V]


ICCH2 – VCC
(hardware standby, Ta = +25 ˚C)
ICCH2 [µA]
100
90
85
70
60
50
40
30
20
10
0
2
3
4
5
6
7
VCC [V]


ICCH1 – VCC
(STOP, Ta = +25 ˚C)
ICCH1 [µA]
20
18
16
14
12
10
8
6
4
2
0
2
3
4
5
6
7
VCC [V]

15. Major Changes

Spansion Publication Number: DS07-13703-7E

Section	Change Results
■ PRODUCT LINEUP	Changed the name in peripheral resource. 16-bit I/O Timer → 16-bit Free-run Timer
■ I/O CIRCUIT TYPE	Changed the name of input typ. Hysteresis → CMOS Hysteresis HYS → CMOS Hysteresis
■ BLOCK DIAGRAM	Changed the arrow direction of SOT1 signal at UART1(SCI). "← →" (input/output) → "←" (output)
■ I/O MAP	Changed the text of "Note".
■ INTERRUPT MAP	Changed the name of peripheral resource of the pin number: #19. I/O Timer → 16-bit Free-run Timer
■ ELECTRICAL CHARACTERISTICS 2. Recommended Conditions	Changed the remarks of "parameter: Power supply voltage".
3. DC Characteristics	Changed the maximum value of symbol : VILM of parameter: Input voltage. V_{CC} + 0.3 → V_{SS} + 0.3
	Added the following remarks for parameter : Pull-down resistance. Except Flash device
4. AC Characteristics (1) Clock Timing	Added the value when using an external clock in Oscillation frequency and Clock cycle time on (1) Clock Timing for parameter.
	Added the item of A/D converter operation range in figure of "■ Guaranteed PLL operation range"
(3) Reset and Hardware Standby Input Timing	Changed the following item. (3) Reset and Hardware Standby Input Timing Remarks: In sub-clock mode, sub-sleep mode, timer mode $2t_{CP}$ → $2t_{LCP}$
(4) Power On Reset	Changed as follows; Due to repetitive operation → Waiting time until power-on
5. A/D Converter	Changed the unit of Zero transition voltage and Full scale transition voltage. mV → V
■ ORDERING INFORMATION	Added the MB90F548GLPMC in Part Numbers.

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: MB90F543G(S)/546G(S)/548G(S)/549G(S)/549G(S)/V540G/MB90543G(S)/547G(S)/548G(S)/F548GL(S) CMOS F2MC-16LX MB90540G/545G Series 16-bit Proprietary Microcontroller
Document Number: 002-07696

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	11/13/2008	Migrated to Cypress and assigned document number 002-07696. No change to document contents or format.
*A	5537115	AKIH	11/30/2016	Updated to Cypress template

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