Infineon Technologies - MB90F543GSPF-GS-9001 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspf-gs-9001

Contents

1. Product Lineup

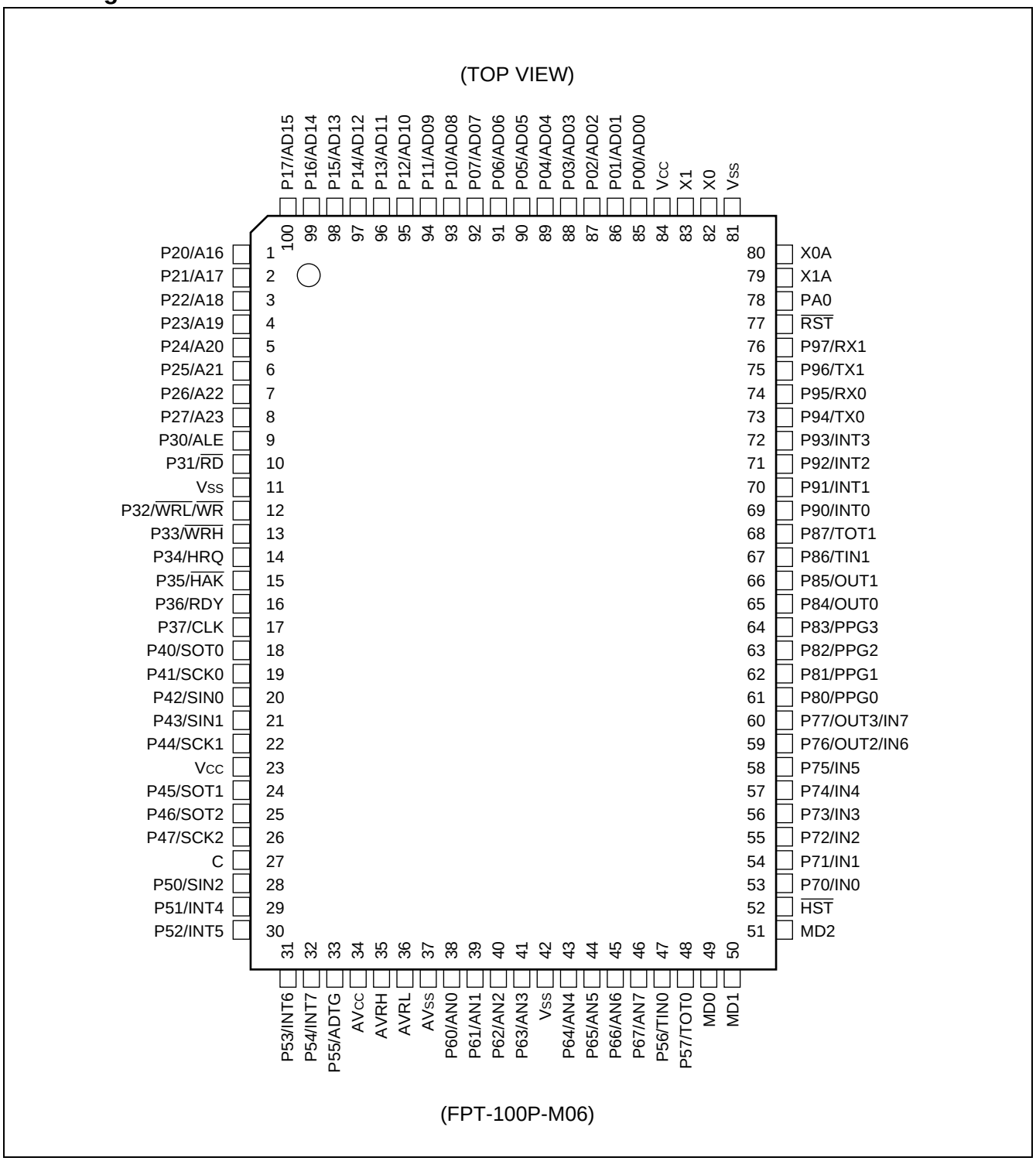
Features	MB90F543G (S) /F548G (S) MB90F549G (S) /F546G (S) MB90F548GL(S)	MB90543G (S) MB90547G (S) MB90548G (S) MB90549G (S)	MB90V540G
CPU	F²MC-16LX CPU		
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, 1/2 when PLL stop) Minimum instruction exection time : 62.5 ns (machine clock 16MHz, 4MHz osc. four times multiplied by PLL)		
ROM	Flash memory MB90F543G(S)/F548G(S) / F548GL(S) : 128 Kbytes MB90F549G(S)/F546G(S) : 256 Kbytes	MASK ROM : MB90547G(S): 64 Kbytes MB90543G(S)/548G(S): 128 Kbytes MB90549G(S): 256 Kbytes	External
RAM	MB90F548G(S)/F548GL(S): 4 Kbytes MB90F543G (S) /F549G(S) : 6 Kbytes MB90F546G(S) : 8 Kbytes	MB90547G(S): 2 Kbytes MB90548G(S): 4 Kbytes MB90543G(S)/549G(S): 6 Kbytes	8 Kbytes
Clocks	MB90F543G/F548G/F549G/F546G/F548GL : Two clocks system MB90F543GS/F548GS/F549GS/F546GS/F548GLS : One clock system	MB90543G/547G/548G/549G : Two clocks system MB90543GS/547GS/548GS/549GS : One clock system	Two clocks system*1
Operating voltage range	*3		
Temperature range	−40 °C to 105 °C		
Package	QFP100, LQFP100		PGA-256
Emulator-specify power supply*2	—		None
UART0	Full duplex double buffer Support asynchronous/synchronous (with start/stop bit) transfer Baud rate : 4808/5208/9615/10417/19230/38460/62500/500000 bps (asynchronous) 500 K/1 M/2 Mbps (synchronous) at System clock = 16 MHz		
UART1 (SCI)	Full duplex double buffer Asynchronous (start-stop synchronized) and CLK-synchronous communication Baud rate : 1202/2404/4808/9615/19230/31250/38460/62500 bps (asynchronous) 62.5 K/125 K/250 K/500 K/1 M/2 Mbps (synchronous) at 6, 8, 10, 12, 16 MHz		
Serial I/O	Transfer can be started from MSB or LSB Supports internal clock synchronized transfer and external clock synchronized transfer Supports positive-edge and nagative-edge clock synchronization Baud rate : 31.25 K/62.5 K/125 K/500 K/1 Mbps at System clock = 16 MHz		
A/D Converter	10-bit or 8-bit resolution 8 input channels Conversion time : 26.3 µs (per one channel)		

(Continued)

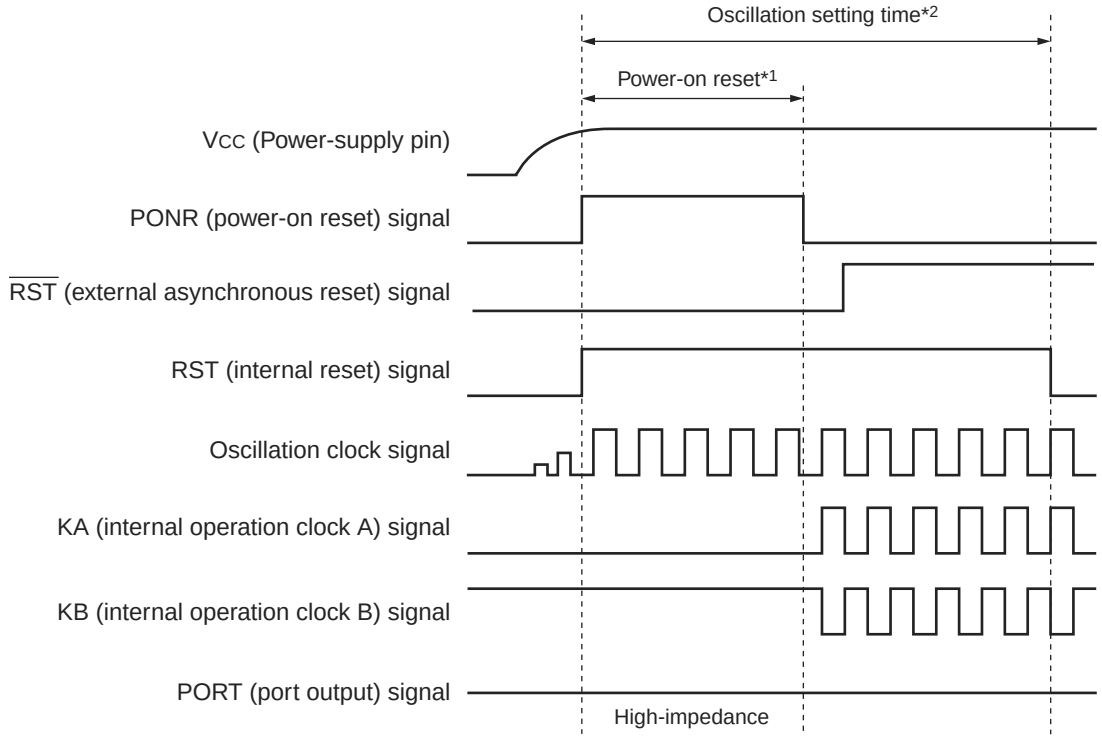
Features	MB90F543G (S) /F548G (S) MB90F549G (S) /F546G (S) MB90F548GL(S)	MB90543G (S) MB90547G (S) MB90548G (S) MB90549G (S)	MB90V540G
16-bit Reload Timer (2 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = System clock frequency) Supports External Event Count function Signals an interrupt when overflow		
16-bit Free-run Timer	Supports Timer Clear when a match with Output Compare (Channel 0) Operation clock freq. : fsys/2^2, fsys/2^4, fsys/2^6, fsys/2^8 (fsys = System clock freq.)		
16-bit Output Compare (4 channels)	Signals an interrupt when a match with 16-bit Free-run Timer Four 16-bit compare registers A pair of compare registers can be used to generate an output signal		
16-bit Input Capture (8 channels)	Rising edge, falling edge or rising & falling edge sensitive Four 16-bit Capture registers Signals an interrupt upon external event		
8/16-bit Programmable Pulse Generator (4 channels)	Supports 8-bit and 16-bit operation modes Eight 8-bit reload counters Eight 8-bit reload registers for L pulse width Eight 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter 4 output pins Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 µs@fosc = 4 MHz (fsys = System clock frequency, fosc = Oscillation clock frequency)		
CAN Interface MB90540G series : 2 channels MB90545G series : 1 channel	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 massage buffers for data and ID's supports multipe massages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps		
32 kHz Sub-clock	Sub-clock for low power operation		
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive		
External bus interface	External access using the selectable 8-bit or 16-bit bus is enabled (external bus mode.)		
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs and schmitt trigger inputs Bit-wise programmable as input/output or peripheral signal Sub-clock for 32 kHz Sub clock low power operation		
Flash Memory	Supports automatic programming, Embeded Algorithm Write/Erase/Erase-Suspend/Erase-Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block Block protection by externally programmed voltage		

*1 : If the one clock system is used, equip X0A and X1A with clocks from the tool side.

2. Pin Assignment



■ $\overline{\text{RST}}$ pin is “L”



*1 : Power-on reset time : “Period of clock frequency” × 2^{17} (Clock frequency of 16 MHz : 8.19 ms)

*2 : Oscillation setting time : “Period of clock frequency” × 2^{18} (Clock frequency of 16 MHz : 16.38 ms)

(13) Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(14) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions

In the Signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”) , the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00_H”.

If the values of the corresponding bank registers (DTB, ADB, USB, SSB) are set to other than “00_H”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

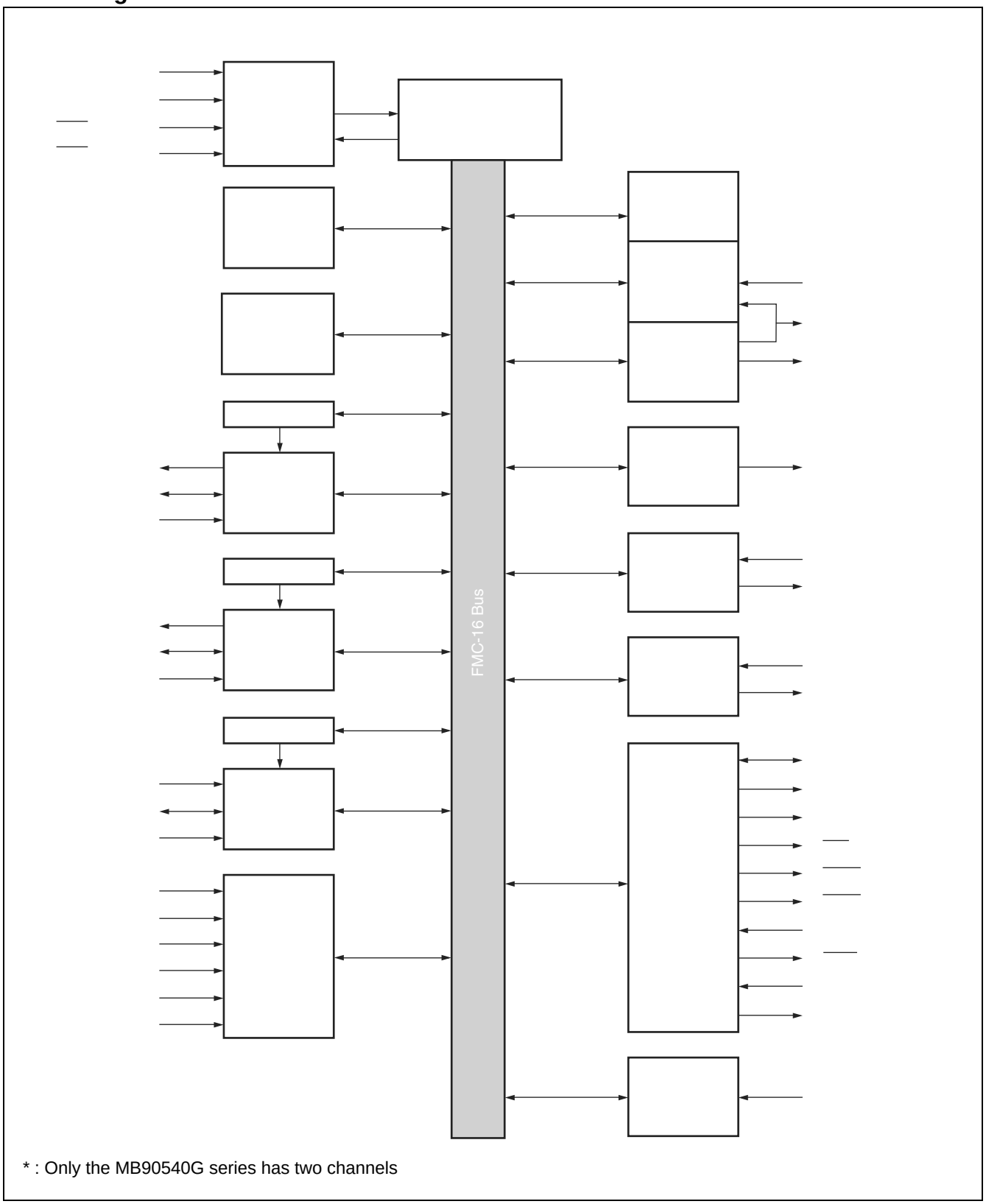
(15) Using REALOS

The use of EI²OS is not possible with the REALOS real time operating system.

(16) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

6. Block Diagram



* : Only the MB90540G series has two channels

Address	Register	Abbreviation	Access	Resource name	Initial value
24H	Serial mode register 1	SMR1	R/W	UART1	0 0 0 0 0 0 0 0B
25H	Serial control register 1	SCR1	R/W		0 0 0 0 0 1 0 0B
26H	Serial input data register 1/ Serial output data register 1	SIDR1/SODR1	R/W		XXXXXXXXB
27H	Serial status register 1	SSR1	R/W		0 0 0 0 1_0 0B
28H	UART1 prescaler control register	CDCR	R/W		0_ _ _1 1 1 1B
29H	Serial Edge select register	SES1	R/W		_ _ _ _ _ _ _0B
2AH	Prohibited				
2BH	Serial I/O prescaler	SCDCR	R/W	Extended I/O Serial Interface	0_ _ _1 1 1 1B
2CH	Serial mode control register	SMCS	R/W		_ _ _ _0 0 0 0B
2DH	Serial mode control register	SMCS	R/W		0 0 0 0 0 0 1 0B
2EH	Serial data register	SDR	R/W		XXXXXXXXB
2FH	Serial Edge select register	SES2	R/W		_ _ _ _ _ _ _0B
30H	External interrupt enable register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0B
31H	External interrupt request register	EIRR	R/W		XXXXXXXXB
32H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0B
33H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0B
34H	A/D control status register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0B
35H	A/D control status register 1	ADCS1	R/W		0 0 0 0 0 0 0 0B
36H	A/D data register 0	ADCR0	R		XXXXXXXXB
37H	A/D data register 1	ADCR1	R/W		0 0 0 0 1 _ XXB
38H	PPG0 operation mode control register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 0 _ _ 1B
39H	PPG1 operation mode control register	PPGC1	R/W		0 _ 0 0 0 0 0 1B
3AH	PPG0/1 clock selection register	PPG01	R/W		0 0 0 0 0 0 _ _B
3BH	Prohibited				
3CH	PPG2 operation mode control register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 0 _ _1B
3DH	PPG3 operation mode control register	PPGC3	R/W		0 _ 0 0 0 0 0 1B
3EH	PPG2/3 Clock Selection Register	PPG23	R/W		0 0 0 0 0 0 _ _B
3FH	Prohibited				
40H	PPG4 operation mode control register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 0 _ _ 1B
41H	PPG5 operation mode control register	PPGC5	R/W		0 _ 0 0 0 0 0 1B
42H	PPG4/5 clock selection register	PPG45	R/W		0 0 0 0 0 0 _ _B
43H	Prohibited				
44H	PPG6 operation mode control register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 0 _ _ 1B
45H	PPG7 operation mode control register	PPGC7	R/W		0 _ 0 0 0 0 0 1B
46H	PPG6/7 clock selection register	PPG67	R/W		0 0 0 0 0 0 _ _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
47_H to $4B_H$	Prohibited				
$4C_H$	Input capture control status register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0_B
$4D_H$	Input capture control status register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0_B
$4E_H$	Input capture control status register 4/5	ICS45	R/W	Input Capture 4/5	0 0 0 0 0 0 0 0_B
$4F_H$	Input capture control status register 6/7	ICS67	R/W	Input Capture 6/7	0 0 0 0 0 0 0 0_B
50_H	Timer control status register 0	TMCSR0	R/W	16-bit Reload Timer 0	0 0 0 0 0 0 0 0_B
51_H	Timer control status register 0	TMCSR0	R/W		_ _ _ _ 0 0 0 0_B
52_H	Timer register 0/reload register 0	TMR0/TMRLR0	R/W		XXXXXXXX_B
53_H	Timer register 0/reload register 0	TMR0/TMRLR0	R/W		XXXXXXXX_B
54_H	Timer control status register 1	TMCSR1	R/W	16-bit Reload Timer 1	0 0 0 0 0 0 0 0_B
55_H	Timer control status register 1	TMCSR1	R/W		_ _ _ _ 0 0 0 0_B
56_H	Timer register 1/reload register 1	TMR1/TMRLR1	R/W		XXXXXXXX_B
57_H	Timer register 1/reload register 1	TMR1/TMRLR1	R/W		XXXXXXXX_B
58_H	Output compare control status register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 _ _ 0 0_B
59_H	Output compare control status register 1	OCS1	R/W		_ _ _ 0 0 0 0 0_B
$5A_H$	Output compare control status register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 _ _ 0 0_B
$5B_H$	Output compare control status register 3	OCS3	R/W		_ _ _ 0 0 0 0 0_B
$5C_H$ to $6B_H$	Prohibited				
$6C_H$	Timer Data register	TCDT	R/W	I/O Timer	0 0 0 0 0 0 0 0_B
$6D_H$	Timer Data register	TCDT	R/W		0 0 0 0 0 0 0 0_B
$6E_H$	Timer Control register	TCCS	R/W		0 0 0 0 0 0 0 0_B
$6F_H$	ROM mirror function selection register	ROMM	R/W	ROM Mirror	_ _ _ _ _ _ _ 1_B
70_H to $7F_H$	Reserved for CAN 0 Interface.				
80_H to $8F_H$	Reserved for CAN 1 Interface.				
90_H to $9D_H$	Prohibited				
$9E_H$	Program address detection control status register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0_B
$9F_H$	Delayed interrupt/release register	DIRR	R/W	Delayed Interrupt	_ _ _ _ _ _ _ 0_B
$A0_H$	Low-power mode control register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0_B
$A1_H$	Clock selection register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0_B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
3900H	Reload L	PRLL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXXB
3901H	Reload H	PRLH0	R/W		XXXXXXXXB
3902H	Reload L	PRLL1	R/W		XXXXXXXXB
3903H	Reload H	PRLH1	R/W		XXXXXXXXB
3904H	Reload L	PRLL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXXB
3905H	Reload H	PRLH2	R/W		XXXXXXXXB
3906H	Reload L	PRLL3	R/W		XXXXXXXXB
3907H	Reload H	PRLH3	R/W		XXXXXXXXB
3908H	Reload L	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXXB
3909H	Reload H	PRLH4	R/W		XXXXXXXXB
390AH	Reload L	PRLL5	R/W		XXXXXXXXB
390BH	Reload H	PRLH5	R/W		XXXXXXXXB
390CH	Reload L	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXXB
390DH	Reload H	PRLH6	R/W		XXXXXXXXB
390EH	Reload L	PRLL7	R/W		XXXXXXXXB
390FH	Reload H	PRLH7	R/W		XXXXXXXXB
3910H to 3917H	Reserved				
3918H	Input Capture Register 0	IPCP0	R	Input Capture 0/1	XXXXXXXXB
3919H	Input Capture Register 0	IPCP0	R		XXXXXXXXB
391AH	Input Capture Register 1	IPCP1	R		XXXXXXXXB
391BH	Input Capture Register 1	IPCP1	R		XXXXXXXXB
391CH	Input Capture Register 2	IPCP2	R	Input Capture 2/3	XXXXXXXXB
391DH	Input Capture Register 2	IPCP2	R		XXXXXXXXB
391EH	Input Capture Register 3	IPCP3	R		XXXXXXXXB
391FH	Input Capture Register 3	IPCP3	R		XXXXXXXXB
3920H	Input Capture Register 4	IPCP4	R	Input Capture 4/5	XXXXXXXXB
3921H	Input Capture Register 4	IPCP4	R		XXXXXXXXB
3922H	Input Capture Register 5	IPCP5	R		XXXXXXXXB
3923H	Input Capture Register 5	IPCP5	R		XXXXXXXXB
3924H	Input Capture Register 6	IPCP6	R	Input Capture 6/7	XXXXXXXXB
3925H	Input Capture Register 6	IPCP6	R		XXXXXXXXB
3926H	Input Capture Register 7	IPCP7	R		XXXXXXXXB
3927H	Input Capture Register 7	IPCP7	R		XXXXXXXXB

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9. CAN Controller

The MB90540G series contains two CAN controllers (CAN0 and CAN1) , the MB90545G series contains only one (CAN0) . The Evaluation Chip MB90V540G also has two CAN controllers.

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 1 Mbps (when input clock is at 16 MHz)

List of Control Registers

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070_H	000080_H	Message buffer valid register	BVALR	R/W	$00000000\ 00000000_B$
000071_H	000081_H				
000072_H	000082_H	Transmit request register	TREQR	R/W	$00000000\ 00000000_B$
000073_H	000083_H				
000074_H	000084_H	Transmit cancel register	TCANR	W	$00000000\ 00000000_B$
000075_H	000085_H				
000076_H	000086_H	Transmit complete register	TCR	R/W	$00000000\ 00000000_B$
000077_H	000087_H				
000078_H	000088_H	Receive complete register	RCR	R/W	$00000000\ 00000000_B$
000079_H	000089_H				
$00007A_H$	$00008A_H$	Remote request receiving register	RRTRR	R/W	$00000000\ 00000000_B$
$00007B_H$	$00008B_H$				
$00007C_H$	$00008C_H$	Receive overrun register	ROVRR	R/W	$00000000\ 00000000_B$
$00007D_H$	$00008D_H$				
$00007E_H$	$00008E_H$	Receive interrupt enable register	RIER	R/W	$00000000\ 00000000_B$
$00007F_H$	$00008F_H$				

(Continued)

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003B00H	003D00H	Control status register	CSR	R/W, R	00---000 0----0-1B
003B01H	003D01H				
003B02H	003D02H	Last event indicator register	LEIR	R/W	-------- 000-0000B
003B03H	003D03H				
003B04H	003D04H	Receive/transmit error counter register	RTEC	R	00000000 00000000B
003B05H	003D05H				
003B06H	003D06H	Bit timing register	BTR	R/W	-1111111 11111111B
003B07H	003D07H				
003B08H	003D08H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXXB
003B09H	003D09H				
003B0AH	003D0AH	Transmit RTR register	TRTRR	R/W	00000000 00000000B
003B0BH	003D0BH				
003B0CH	003D0CH	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXXB
003B0DH	003D0DH				
003B0EH	003D0EH	Transmit request enable register	TIER	R/W	00000000 00000000B
003B0FH	003D0FH				
003B10H	003D10H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXXB
003B11H	003D11H				
003B12H	003D12H				XXXXXXXX XXXXXXXXB
003B13H	003D13H				
003B14H	003D14H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXXB
003B15H	003D15H				
003B16H	003D16H				XXXXX--- XXXXXXXXB
003B17H	003D17H				
003B18H	003D18H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXXB
003B19H	003D19H				
003B1AH	003D1AH				XXXXX--- XXXXXXXXB
003B1BH	003D1BH				

List of Message Buffers (ID Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A00H to 003A1FH	003C00H to 003C1FH	General-purpose RAM	—	R/W	XXXXXXXXB to XXXXXXXXB
003A20H	003C20H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXXB
003A21H	003C21H				
003A22H	003C22H				XXXXX--- XXXXXXXXB
003A23H	003C23H				

(Continued)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A3C$_H$	003C3C$_H$	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX$_B$
003A3D$_H$	003C3D$_H$				
003A3E$_H$	003C3E$_H$				XXXXX--- XXXXXXXX$_B$
003A3F$_H$	003C3F$_H$				
003A40$_H$	003C40$_H$	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX$_B$
003A41$_H$	003C41$_H$				
003A42$_H$	003C42$_H$				XXXXX--- XXXXXXXX$_B$
003A43$_H$	003C43$_H$				
003A44$_H$	003C44$_H$	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX$_B$
003A45$_H$	003C45$_H$				
003A46$_H$	003C46$_H$				XXXXX--- XXXXXXXX$_B$
003A47$_H$	003C47$_H$				
003A48$_H$	003C48$_H$	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX$_B$
003A49$_H$	003C49$_H$				
003A4A$_H$	003C4A$_H$				XXXXX--- XXXXXXXX$_B$
003A4B$_H$	003C4B$_H$				
003A4C$_H$	003C4C$_H$	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX$_B$
003A4D$_H$	003C4D$_H$				
003A4E$_H$	003C4E$_H$				XXXXX--- XXXXXXXX$_B$
003A4F$_H$	003C4F$_H$				
003A50$_H$	003C50$_H$	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX$_B$
003A51$_H$	003C51$_H$				
003A52$_H$	003C52$_H$				XXXXX--- XXXXXXXX$_B$
003A53$_H$	003C53$_H$				
003A54$_H$	003C54$_H$	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX$_B$
003A55$_H$	003C55$_H$				
003A56$_H$	003C56$_H$				XXXXX--- XXXXXXXX$_B$
003A57$_H$	003C57$_H$				
003A58$_H$	003C58$_H$	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX$_B$
003A59$_H$	003C59$_H$				
003A5A$_H$	003C5A$_H$				XXXXX--- XXXXXXXX$_B$
003A5B$_H$	003C5B$_H$				
003A5C$_H$	003C5C$_H$	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX$_B$
003A5D$_H$	003C5D$_H$				
003A5E$_H$	003C5E$_H$				XXXXX--- XXXXXXXX$_B$
003A5F$_H$	003C5F$_H$				

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0.0$ V)

Parameter	Symbol	Value		Units	Remarks
		Min	Max		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *1
	AVRH, AVRL	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq$ AVRH/AVRL, AVRH $\geq$ AVRL *1
Input voltage	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Output voltage	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Maximum clamp current	I_{CLAMP}	−2.0	+2.0	mA	*6
Total maximum clamp current	$\Sigma\lvert I_{CLAMP} \rvert$	−	20	mA	*6
“L” level max output current	I_{OL}	−	15	mA	*3
“L” level avg. output current	I_{OLAV}	−	4	mA	*4
“L” level max overall output current	ΣI_{OL}	−	100	mA	
“L” level avg. overall output current	ΣI_{OLAV}	−	50	mA	*5
“H” level max output current	I_{OH}	−	−15	mA	*3
“H” level avg. output current	I_{OHAV}	−	−4	mA	*4
“H” level max overall output current	ΣI_{OH}	−	−100	mA	
“H” level avg. overall output current	ΣI_{OHAV}	−	−50	mA	*5
Power consumption	P_D	−	500	mW	Flash device
		−	400	mW	MASK ROM
Operating temperature	T_A	−40	+105	°C	
Storage temperature	T_{STG}	−55	+150	°C	

*1 : AV_{CC}, AVRH, AVRL should not exceed V_{CC}. Also, AVRH, AVRL should not exceed AV_{CC}, and AVRL does not exceed AVRH.

*2 : V_I and V_O should not exceed $V_{CC} + 0.3$ V. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supercedes the V_I rating.

*3 : The maximum output current is a peak value for a corresponding pin.

*4 : Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5 : Total average current is an average current value observed for a 100 ms period for all corresponding pins.

*6 :

- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The + B signal should always be applied with a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the + B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a + B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- Care must be taken not to leave the + B input pin open.

11.4 AC Characteristics

11.4.1 Clock Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Oscillation frequency	f_C	X0, X1	3	—	16	MHz	No multiplier When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			8	—	16	MHz	PLL multiplied by 1 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			4	—	8	MHz	PLL multiplied by 2 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			3	—	5.33	MHz	PLL multiplied by 3 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			3	—	4	MHz	PLL multiplied by 4 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			3	—	5	MHz	When using an oscillator circuit V_{CC} < 4.5 V(MB90F548GL(S)/543G(S)/547G(S)/548G(S))
			3	—	16	MHz	No multiplier When using an external clock
			8	—	16	MHz	PLL multiplied by 1 When using an external clock
			4	—	8	MHz	PLL multiplied by 2 When using an external clock
			3	—	5.33	MHz	PLL multiplied by 3 When using an external clock
			3	—	4	MHz	PLL multiplied by 4 When using an external clock
	f_{CL}	X0A, X1A	—	32.768	—	kHz	

(Continued)

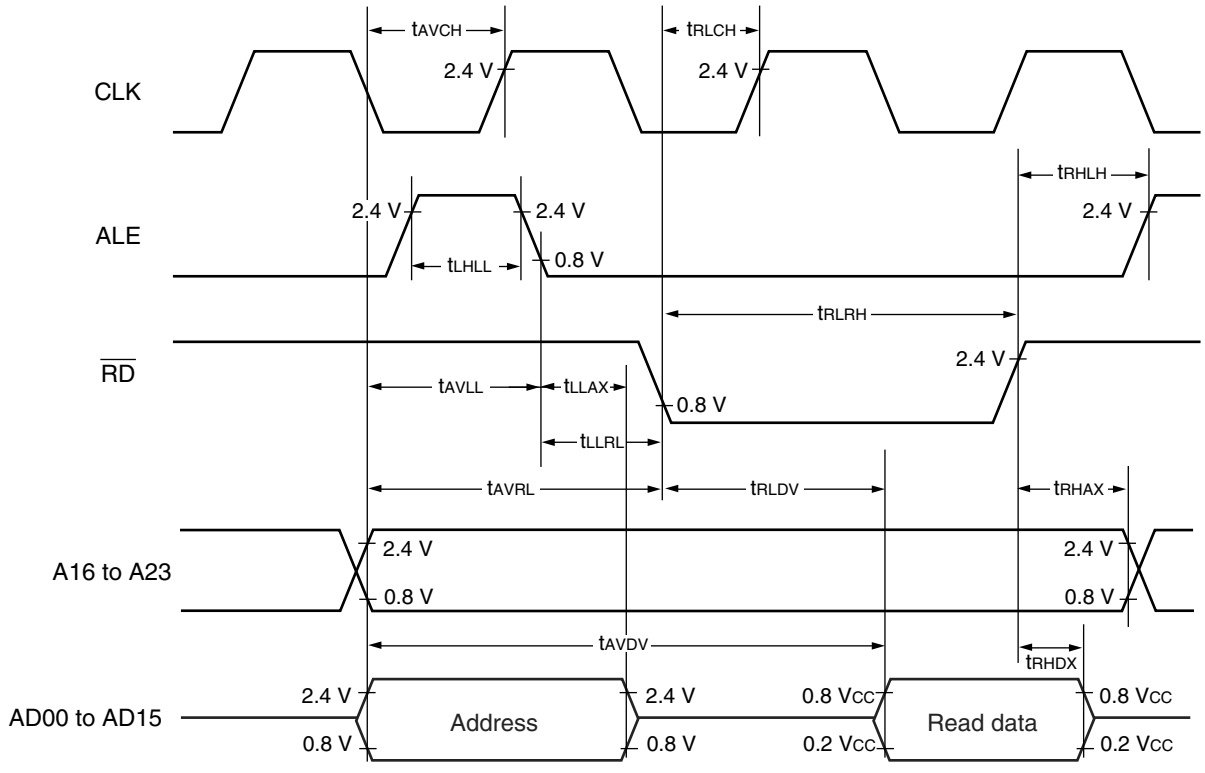
11.4.5 Bus Timing (Read)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE		$t_{CP}/2 - 20$	−	ns	
Valid address → ALE↓ time	t_{AVLL}	ALE, A16 to A23, AD00 to AD15		$t_{CP}/2 - 20$	−	ns	
ALE↓ → Address valid time	t_{LLAX}	ALE, AD00 to AD15		$t_{CP}/2 - 15$	−	ns	
Valid address → $\overline{RD}$↓ time	t_{AVRL}	A16 toA23, AD00 to AD15, $\overline{RD}$		$t_{CP} - 15$	−	ns	
Valid address → Valid data input	t_{AVDV}	A16 to A23, AD00 to AD15		−	$5\ t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	RD	−	$3\ t_{CP}/2 - 20$	−	ns	
$\overline{RD}$↓ → Valid data input	t_{RLDV}	$\overline{RD}$, AD00 to AD15		−	$3\ t_{CP}/2 - 60$	ns	
$\overline{RD}$↑ → Data hold time	t_{RHDX}	$\overline{RD}$, AD00 to AD15		0	−	ns	
$\overline{RD}$↑ → ALE↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	−	ns	
$\overline{RD}$↑ → Address valid time	t_{RHAX}	$\overline{RD}$, A16 to A23		$t_{CP}/2 - 10$	−	ns	
Valid address → CLK↑ time	t_{AVCH}	A16 to A23, AD00 to AD15, CLK		$t_{CP}/2 - 20$	−	ns	
$\overline{RD}$↓ → CLK↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 20$	−	ns	
ALE↓ → $\overline{RD}$↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	−	ns	

■ **Bus Timing (Read)**



11.4.7 Ready Input Timing

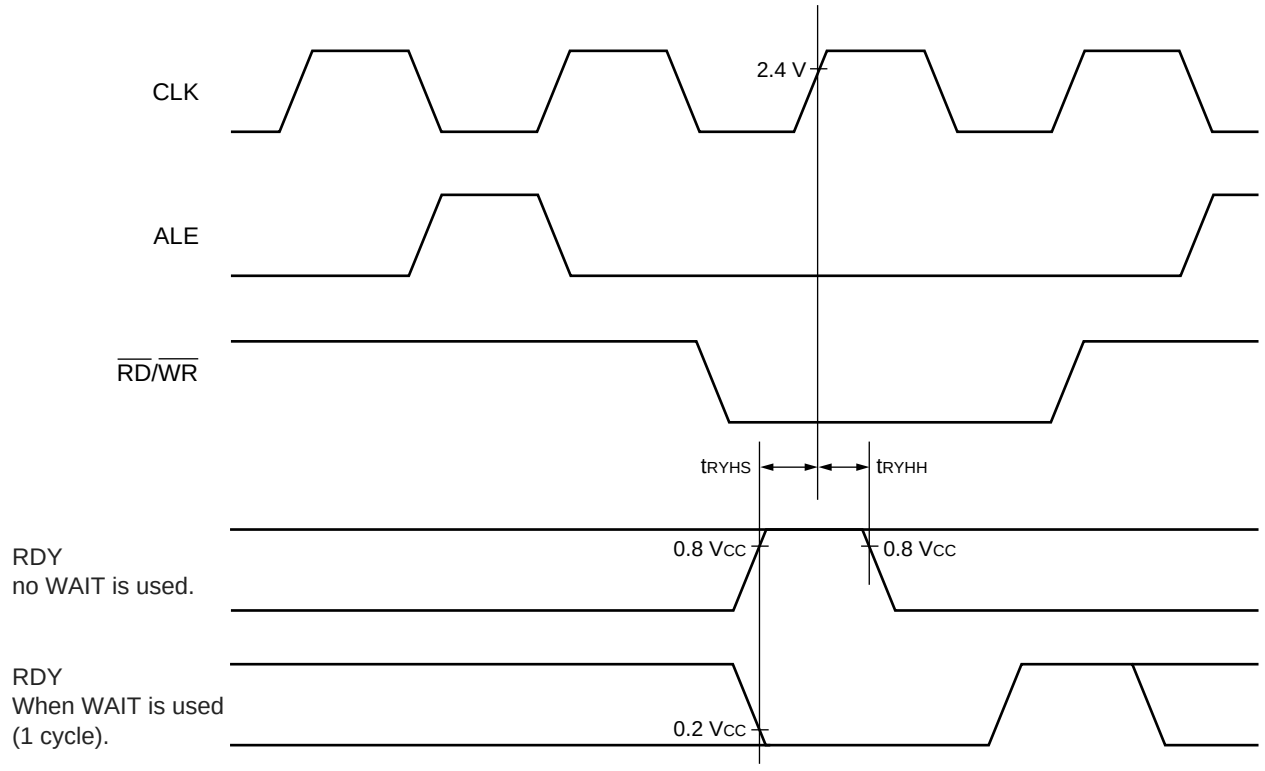
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.

■ **Ready Input Timing**



11.4.8 Hold Timing

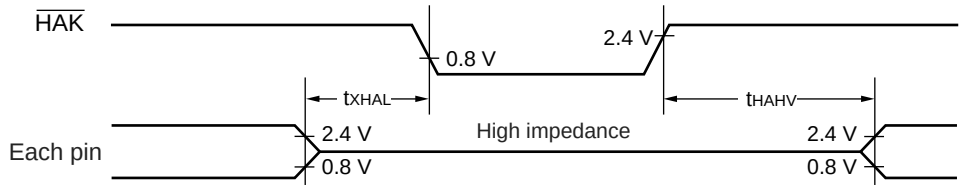
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Pin floating → $\overline{HAK}$↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}	ns	
$\overline{HAK}$↑ time → Pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}	ns	

Note : There is more than 1 cycle from the time HRQ is read to the time the $\overline{HAK}$ is changed.

■ **Hold Timing**



11.4.9 UART0/1, Serial I/O Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

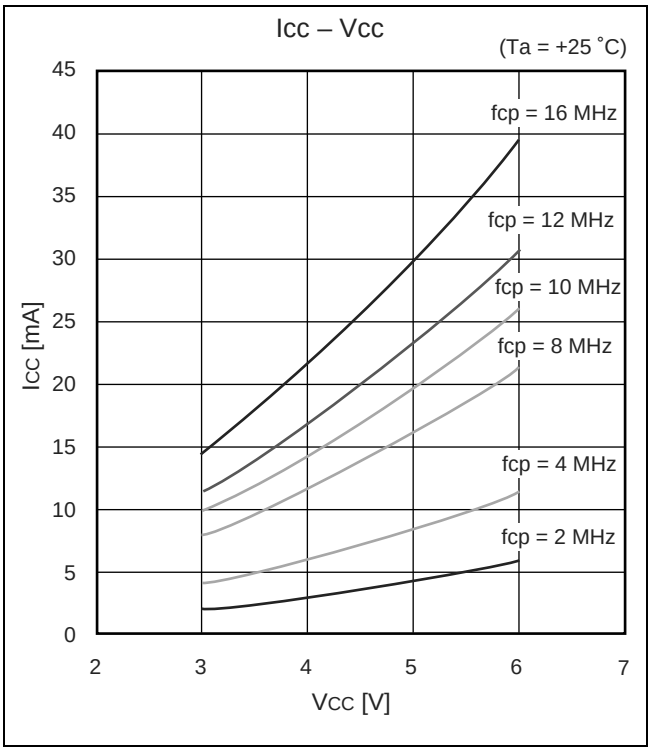
(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

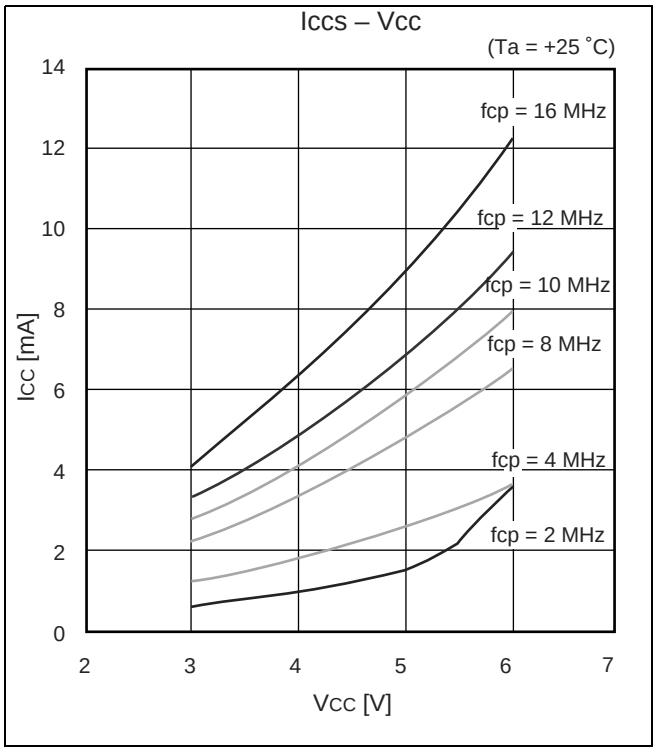
Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	8 t_{CP}	—	ns	
SCK↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		− 80	80	ns	
Valid SIN → SCK↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK2	External clock operation output pins are C_L = 80 pF + 1 TTL.	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK2		4 t_{CP}	—	ns	
SCK↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN → SCK↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

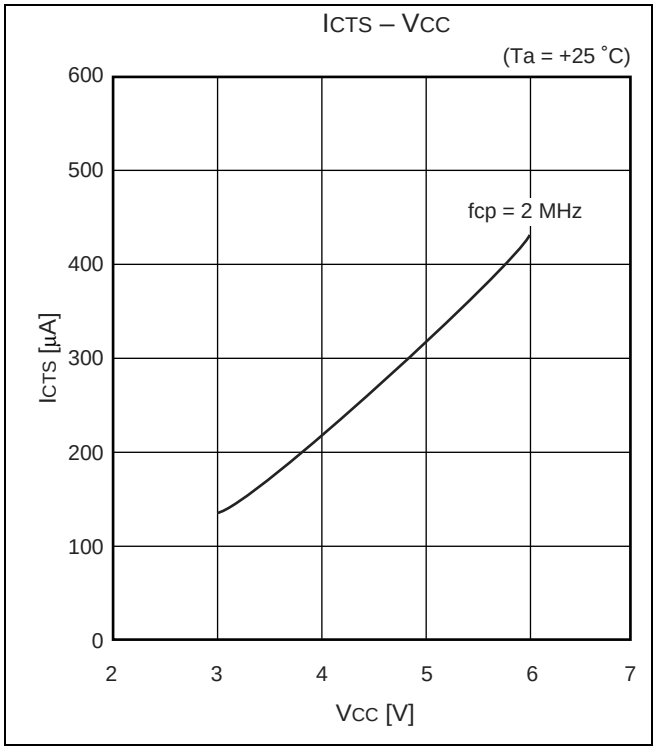
Notes :

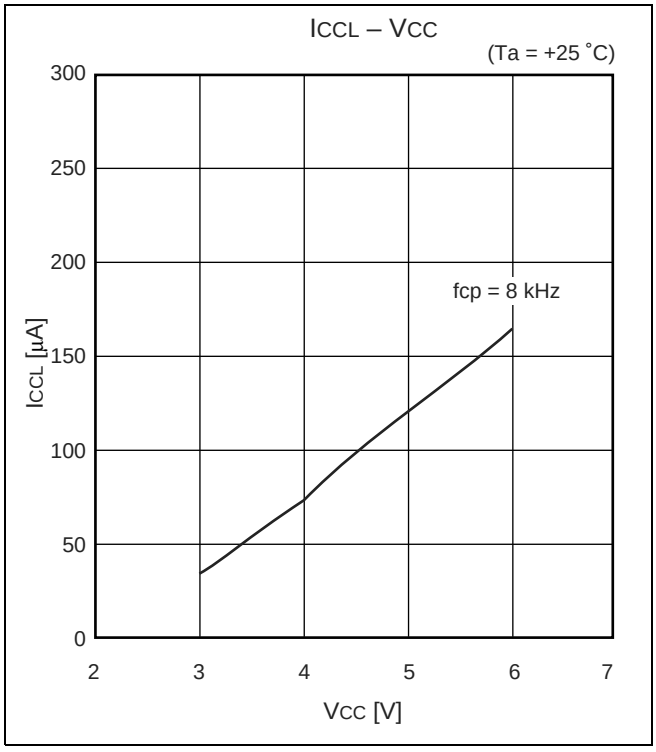
- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- For t_{CP} (Machine clock cycle time) , refer to “ (1) Clock Timing”.

■ Power supply current (MB90F549G)

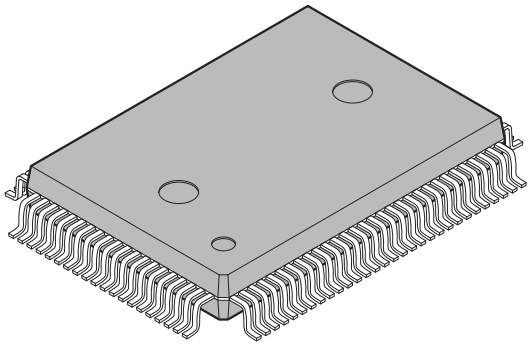


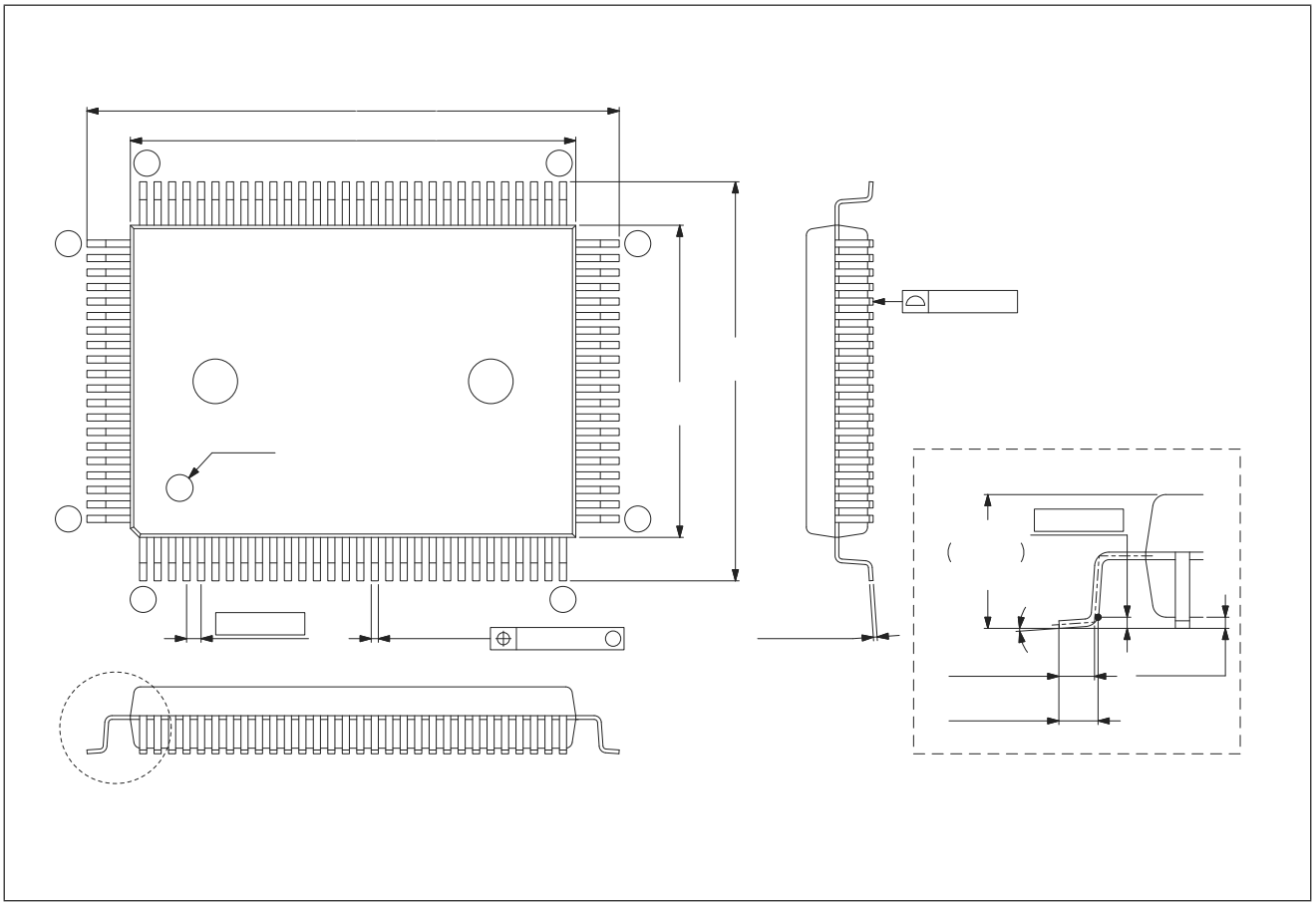






14. Package Dimensions



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