Infineon Technologies - MB90F543GSPF-GS-9002 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspf-gs-9002

Starting by an external trigger input.
Conversion time : 26.3 μs

- FULL-CAN interfaces
  MB90540G series : 2 channels
  MB90545G series : 1 channel
  Conforming to Version 2.0 Part A and Part B
  Flexible message buffering (mailbox and FIFO buffering can be mixed)
- External bus interface : Maximum address space 16 Mbytes
- Package: QFP-100, LQFP-100

Contents

Features	MB90F543G (S) /F548G (S) MB90F549G (S) /F546G (S) MB90F548GL(S)	MB90543G (S) MB90547G (S) MB90548G (S) MB90549G (S)	MB90V540G
16-bit Reload Timer (2 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = System clock frequency) Supports External Event Count function Signals an interrupt when overflow		
16-bit Free-run Timer	Supports Timer Clear when a match with Output Compare (Channel 0) Operation clock freq. : fsys/2^2, fsys/2^4, fsys/2^6, fsys/2^8 (fsys = System clock freq.)		
16-bit Output Compare (4 channels)	Signals an interrupt when a match with 16-bit Free-run Timer Four 16-bit compare registers A pair of compare registers can be used to generate an output signal		
16-bit Input Capture (8 channels)	Rising edge, falling edge or rising & falling edge sensitive Four 16-bit Capture registers Signals an interrupt upon external event		
8/16-bit Programmable Pulse Generator (4 channels)	Supports 8-bit and 16-bit operation modes Eight 8-bit reload counters Eight 8-bit reload registers for L pulse width Eight 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter 4 output pins Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 µs@fosc = 4 MHz (fsys = System clock frequency, fosc = Oscillation clock frequency)		
CAN Interface MB90540G series : 2 channels MB90545G series : 1 channel	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 massage buffers for data and ID's supports multipe massages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps		
32 kHz Sub-clock	Sub-clock for low power operation		
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive		
External bus interface	External access using the selectable 8-bit or 16-bit bus is enabled (external bus mode.)		
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs and schmitt trigger inputs Bit-wise programmable as input/output or peripheral signal Sub-clock for 32 kHz Sub clock low power operation		
Flash Memory	Supports automatic programming, Embeded Algorithm Write/Erase/Erase-Suspend/Erase-Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block Block protection by externally programmed voltage		

*1 : If the one clock system is used, equip X0A and X1A with clocks from the tool side.

*2 : It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*3 : Operating Voltage Range

Products	Operation guarantee range
MB90F543G(S)/F546G(S)/F548G(S)/ MB90549G(S)/F549G(S)/V540/V540G	4.5 V to 5.5 V
MB90F548GL(S)/543G(S)/547G(S)/548G(S)	3.5 V to 5.5 V

Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
11	13	P33	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode, external bus 8-bit mode or when WRH pin output is disabled.
		$\overline{\text{WRH}}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{\text{WRH}}$ output pin is enabled.
12	14	P34	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.
13	15	P35	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.
14	16	P36	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.
		RDY		Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.
15	17	P37	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the CLK output is disabled.
		CLK		CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled.
16	18	P40	G	General I/O port. This function is enabled when UART0 disables the serial data output.
		SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.
17	19	P41	G	General I/O port. This function is enabled when UART0 disables serial clock output.
		SCK0		Serial clock I/O pin for UART0. This function is enabled when UART0 enables the serial clock output.
18	20	P42	G	General I/O port. This function is always enabled.
		SIN0		Serial data input pin for UART0. Set the corresponding Port Direction Register to input if this function is used.
19	21	P43	G	General I/O port. This function is always enabled.
		SIN1		Serial data input pin for UART1. Set the corresponding Port Direction Register to input if this function is used.

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Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
20	22	P44	G	General I/O port. This function is enabled when UART1 disables the clock output.
		SCK1		Serial clock pulse I/O pin for UART1. This function is enabled when UART1 enables the serial clock output.
22	24	P45	G	General I/O port. This function is enabled when UART1 disables the serial data output.
		SOT1		Serial data output pin for UART1. This function is enabled when UART1 enables the serial data output.
23	25	P46	G	General I/O port. This function is enabled when the Extended I/O serial interface disables the serial data output.
		SOT2		Serial data output pin for the Extended I/O serial interface. This function is enabled when the Extended I/O serial interface enables the serial data output.
24	26	P47	G	General I/O port. This function is enabled when the Extended I/O serial interface disables the clock output.
		SCK2		Serial clock pulse I/O pin for the Extended I/O serial interface . This function is enabled when the Extended I/O serial interface enables the Serial clock output.
26	28	P50	D	General I/O port. This function is always enabled.
		SIN2		Serial data input pin for the Extended I/O serial interface . Set the corresponding Port Direction Register to input if this function is used.
27 to 30	29 to 32	P51 to P54	D	General I/O port. This function is always enabled.
		INT4 to INT7		External interrupt request input pins for INT4 to INT7. Set the corresponding Port Direction Register to input if this function is used.
31	33	P55	D	General I/O port. This function is always enabled.
		ADTG		Trigger input pin for the A/D converter. Set the corresponding Port Direction Register to input if this function is used.
36 to 39	38 to 41	P60 to P63	E	General I/O port. This function is enabled when the analog input enable register specifies a port.
		AN0 to AN3		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.
41 to 44	43 to 46	P64 to P67	E	General I/O port. The function is enabled when the analog input enable register specifies a port.
		AN4 to AN7		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.
45	47	P56	D	General I/O port. This function is always enabled.
		TIN0		Event input pin for the 16-bit reload timers 0. Set the corresponding Port Direction Register to input if this function is used.

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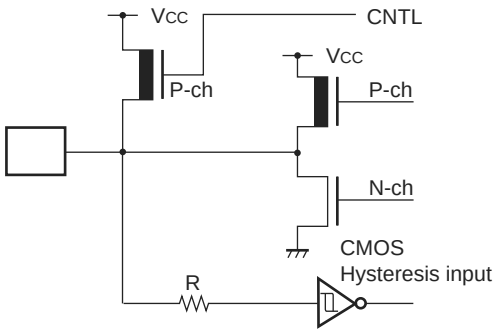
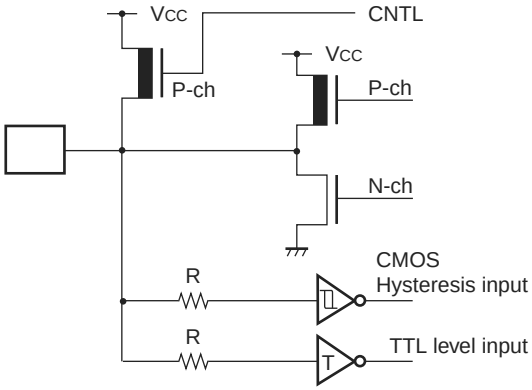
Circuit type	Diagram	Remarks
H		■ CMOS level output ■ CMOS Hysteresis input ■ Programmable pull-up resistor : 50 kΩ approx.
I		■ CMOS level output ■ CMOS Hysteresis input ■ TTL level input (Flash devices in Flash writer mode only) ■ Programmable pullup resistor : 50 kΩ approx.

(6) Pull-up/down resistors

The MB90540G/545G Series does not support internal pull-up/down resistors (except Port0 − Port3 : pull-up resistors) . Use external components where needed.

(7) Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via the shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuits do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation.

(8) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}) .

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable) .

(9) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

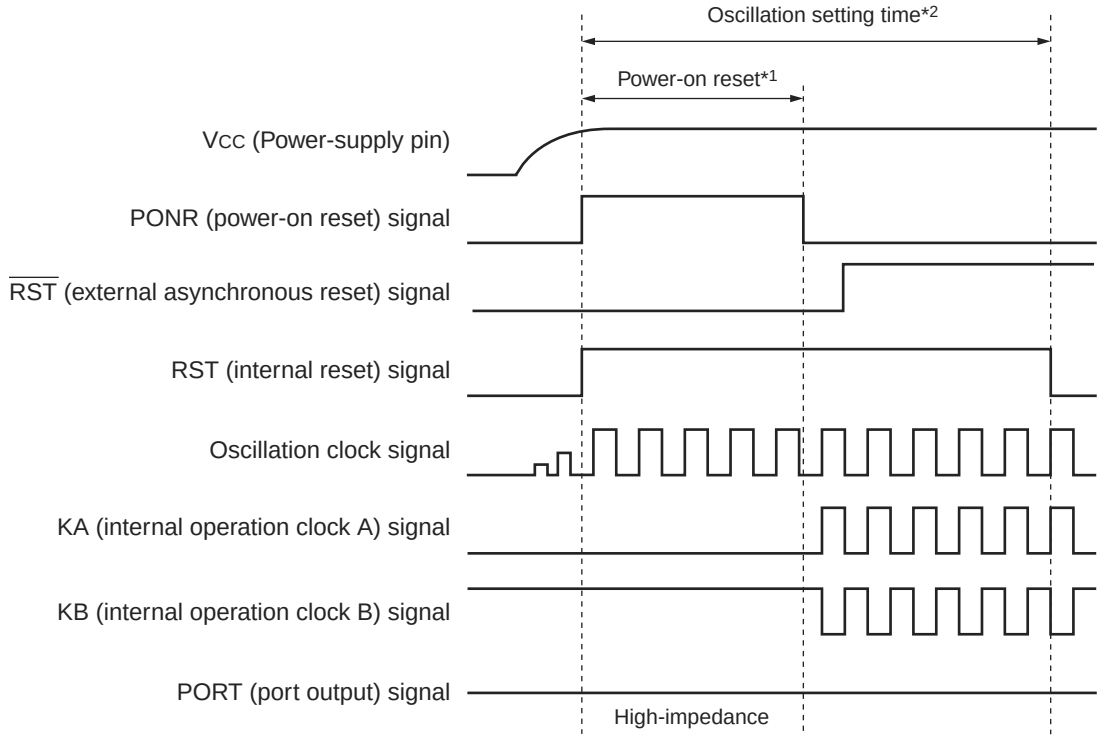
(10) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

(11) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μs or more (0.2 V to 2.7 V) .

■ $\overline{\text{RST}}$ pin is “L”



*1 : Power-on reset time : “Period of clock frequency” × 2^{17} (Clock frequency of 16 MHz : 8.19 ms)

*2 : Oscillation setting time : “Period of clock frequency” × 2^{18} (Clock frequency of 16 MHz : 16.38 ms)

(13) Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(14) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions

In the Signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”) , the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00_H”.

If the values of the corresponding bank registers (DTB, ADB, USB, SSB) are set to other than “00_H”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

(15) Using REALOS

The use of EI²OS is not possible with the REALOS real time operating system.

(16) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

(Continued)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A3C$_H$	003C3C$_H$	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX$_B$
003A3D$_H$	003C3D$_H$				
003A3E$_H$	003C3E$_H$				XXXXX--- XXXXXXXX$_B$
003A3F$_H$	003C3F$_H$				
003A40$_H$	003C40$_H$	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX$_B$
003A41$_H$	003C41$_H$				
003A42$_H$	003C42$_H$				XXXXX--- XXXXXXXX$_B$
003A43$_H$	003C43$_H$				
003A44$_H$	003C44$_H$	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX$_B$
003A45$_H$	003C45$_H$				
003A46$_H$	003C46$_H$				XXXXX--- XXXXXXXX$_B$
003A47$_H$	003C47$_H$				
003A48$_H$	003C48$_H$	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX$_B$
003A49$_H$	003C49$_H$				
003A4A$_H$	003C4A$_H$				XXXXX--- XXXXXXXX$_B$
003A4B$_H$	003C4B$_H$				
003A4C$_H$	003C4C$_H$	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX$_B$
003A4D$_H$	003C4D$_H$				
003A4E$_H$	003C4E$_H$				XXXXX--- XXXXXXXX$_B$
003A4F$_H$	003C4F$_H$				
003A50$_H$	003C50$_H$	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX$_B$
003A51$_H$	003C51$_H$				
003A52$_H$	003C52$_H$				XXXXX--- XXXXXXXX$_B$
003A53$_H$	003C53$_H$				
003A54$_H$	003C54$_H$	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX$_B$
003A55$_H$	003C55$_H$				
003A56$_H$	003C56$_H$				XXXXX--- XXXXXXXX$_B$
003A57$_H$	003C57$_H$				
003A58$_H$	003C58$_H$	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX$_B$
003A59$_H$	003C59$_H$				
003A5A$_H$	003C5A$_H$				XXXXX--- XXXXXXXX$_B$
003A5B$_H$	003C5B$_H$				
003A5C$_H$	003C5C$_H$	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX$_B$
003A5D$_H$	003C5D$_H$				
003A5E$_H$	003C5E$_H$				XXXXX--- XXXXXXXX$_B$
003A5F$_H$	003C5F$_H$				

11.2 Recommended Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value			Units	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.5	5.0	5.5	V	Under normal operation : Other than MB90F548GL(S)/543G(S)/547G(S)/548G(S)
						Under normal operation when A/D conveter is used : MB90F548GL(S)/543G(S)/547G(S)/548G(S)
		3.5	5.0	5.5	V	Under normal operation when A/D conveter is not used : MB90F548GL(S)/543G(S)/547G(S)/548G(S)
		3.0	−	5.5	V	Maintain RAM data in stop mode
Smooth capacitor	C_S	0.022	0.1	1.0	µF	*
Operating temperature	T_A	−40	−	+105	°C	

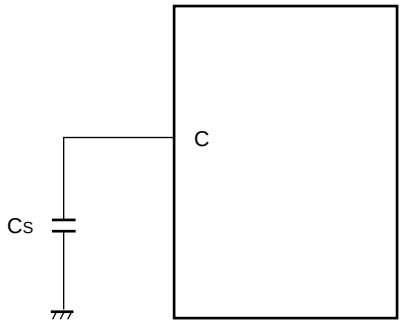
*: Use a ceramic capacitor or a capacitor of better 4. AC characteristics. The bypass capacitor should be greater than this capacitor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ **C Pin Connection Diagram**



11.3 DC Characteristics

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Input H voltage	V_{IHS}	CMOS hysteresis input pin	−	0.8 V_{CC}	−	V_{CC} + 0.3	V	
	V_{IH}	TTL input pin	−	2.0	−	−	V	
	V_{IHM}	MD input pin	−	V_{CC} − 0.3	−	V_{CC} + 0.3	V	
Input L voltage	V_{ILS}	CMOS hysteresis input pin	−	V_{CC} − 0.3	−	0.2 V_{CC}	V	
	V_{IL}	TTL input pin	−	−	−	0.8	V	
	V_{ILM}	MD input pin	−	V_{SS} − 0.3	−	V_{SS} + 0.3	V	
Output H voltage	V_{OH}	All output pins	V_{CC} = 4.5 V, I_{OH} = −4.0 mA	V_{CC} − 0.5	−	−	V	
Output L voltage	V_{OL}	All output pins	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	−	−	0.4	V	
Input leak current	I_{IL}	−	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	−5	−	5	µA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, RST	−	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	−	25	50	100	kΩ	Except Flash devices

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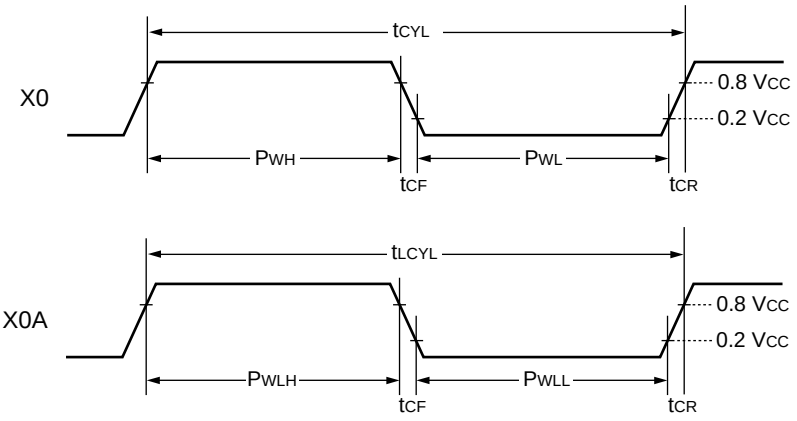
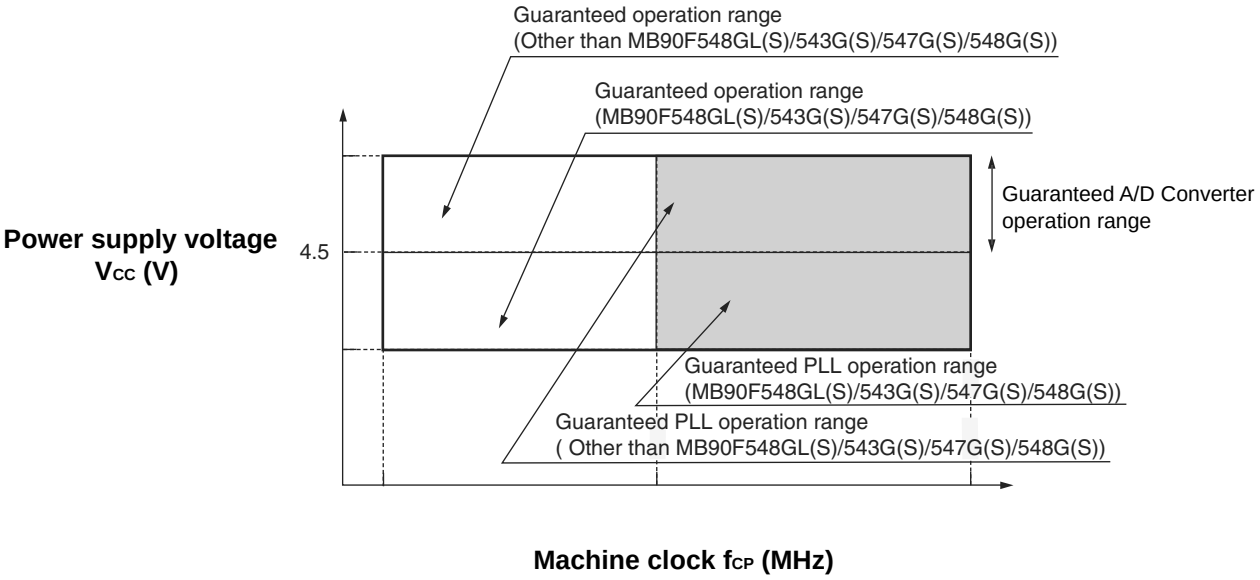
■ **Clock Timing**



■ **Guaranteed PLL operation range**



11.4.4 Power On Reset

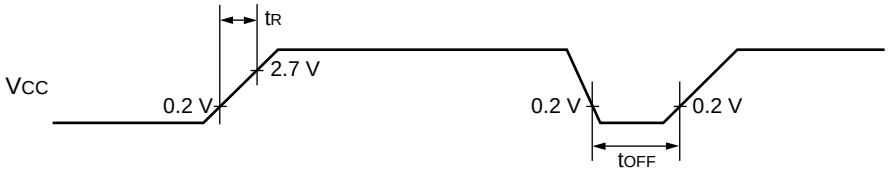
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

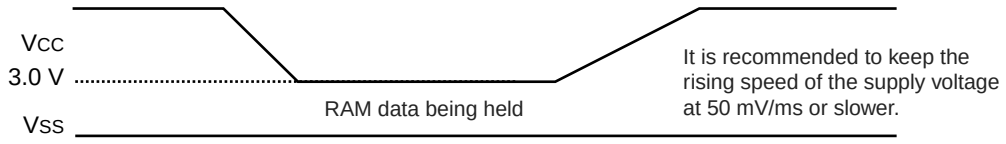
Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	*
Power off time	t_{OFF}	V_{CC}		50	—	ms	Waiting time until power-on

* : V_{CC} must be kept lower than 0.2 V before power-on.

Notes : ■ The above values are used for creating a power-on reset.
■ Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.



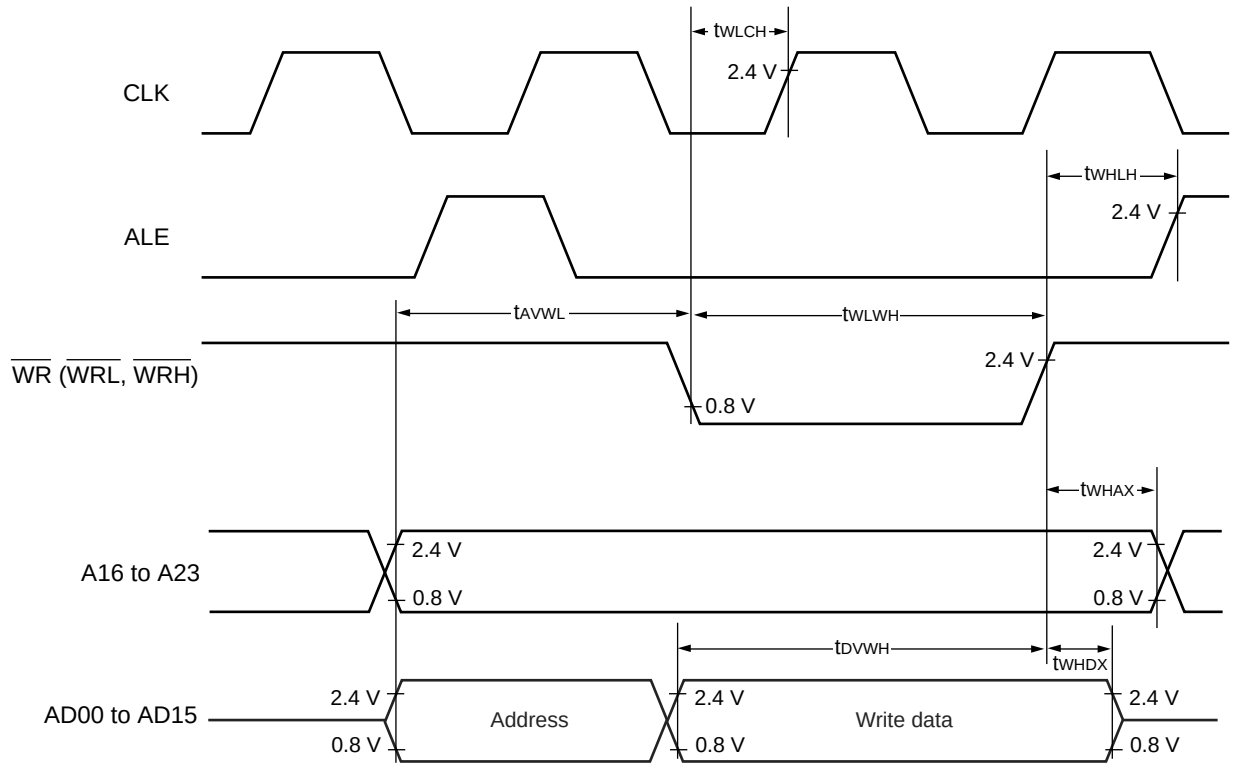
11.4.6 Bus Timing (Write)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Valid address → $\overline{WR}$↓ time	t_{AVWL}	A16 to A23 AD00 to AD15, $\overline{WR}$	—	t_{CP} − 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	WR		3 t_{CP}/2 − 20	—	ns	
Valid data output → $\overline{WR}$↑ time	t_{DVWH}	AD00 to AD15, $\overline{WR}$		3 t_{CP}/2 − 20	—	ns	
$\overline{WR}$↑ → Data hold time	t_{WHDX}	AD00 to AD15, $\overline{WR}$		20	—	ns	
$\overline{WR}$↑ → Address valid time	t_{WHAX}	A16 to A23, $\overline{WR}$		t_{CP}/2 − 10	—	ns	
$\overline{WR}$↑ → ALE↑ time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 − 15	—	ns	
$\overline{WR}$↑ → CLK↑ time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 − 20	—	ns	

■ **Bus Timing** (**Write**)



11.4.7 Ready Input Timing

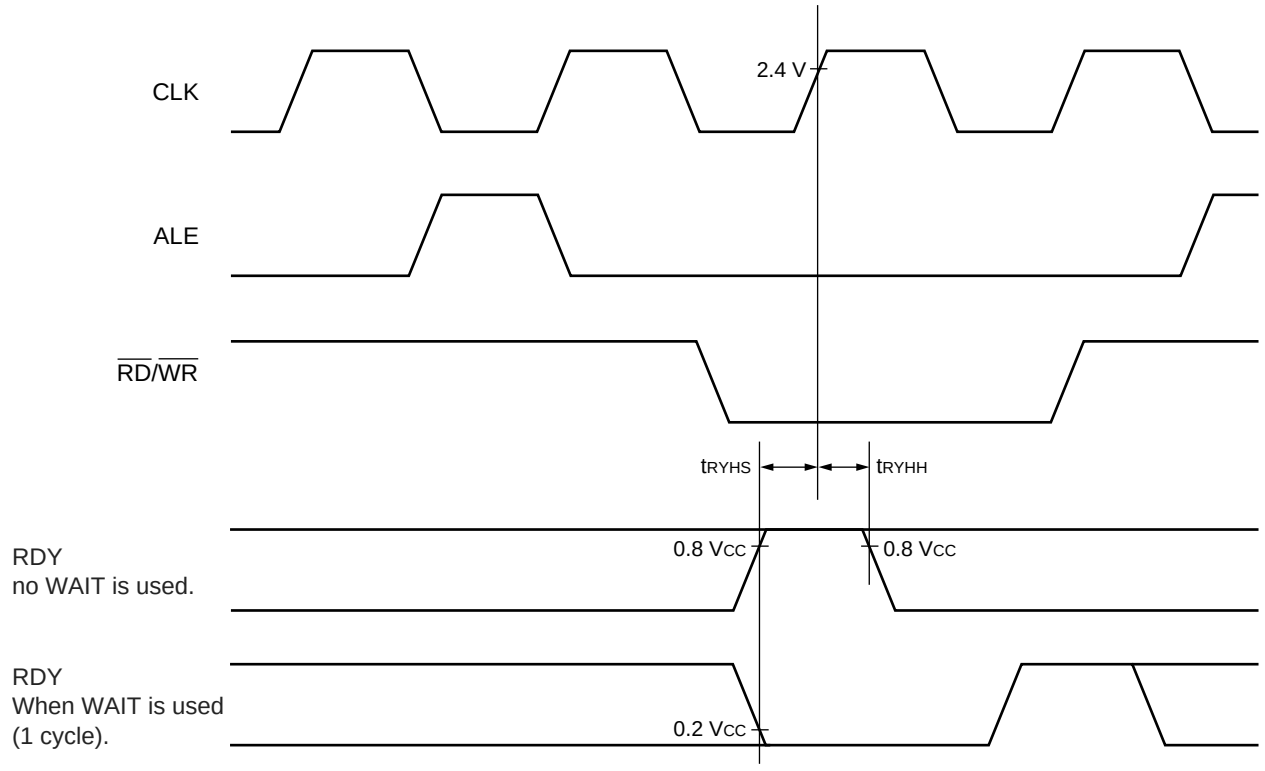
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.

■ **Ready Input Timing**



11.4.8 Hold Timing

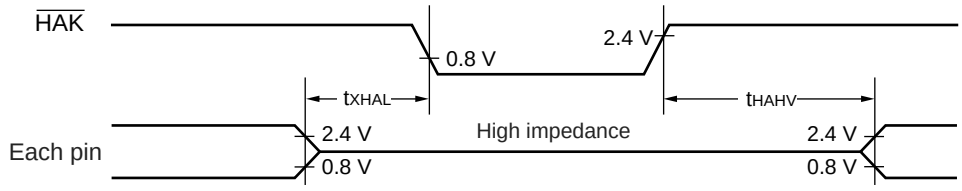
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Pin floating → $\overline{HAK}$↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}	ns	
$\overline{HAK}$↑ time → Pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}	ns	

Note : There is more than 1 cycle from the time HRQ is read to the time the $\overline{HAK}$ is changed.

■ **Hold Timing**



11.4.9 UART0/1, Serial I/O Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

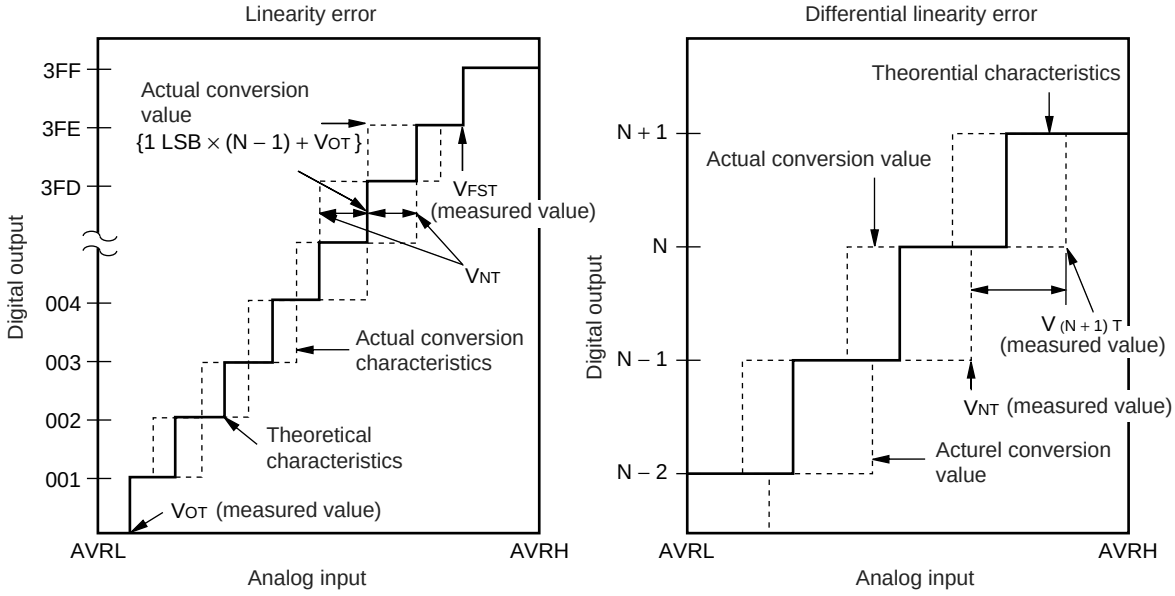
(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	8 t_{CP}	—	ns	
SCK↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		− 80	80	ns	
Valid SIN → SCK↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK2	External clock operation output pins are C_L = 80 pF + 1 TTL.	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK2		4 t_{CP}	—	ns	
SCK↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN → SCK↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

Notes :

- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- For t_{CP} (Machine clock cycle time) , refer to “ (1) Clock Timing”.

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage at transition of digital output from "000_H" to "001_H"
V_{FST} : Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

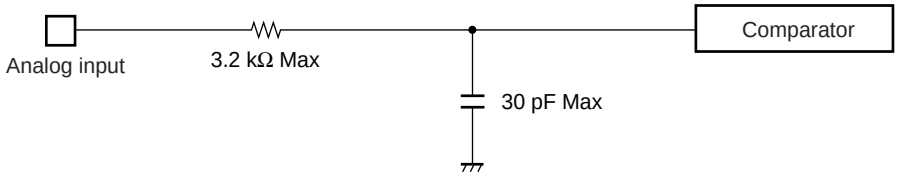
11.5.3 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions, :

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

Note : When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz) .

■ **Equipment of analog input circuit model**

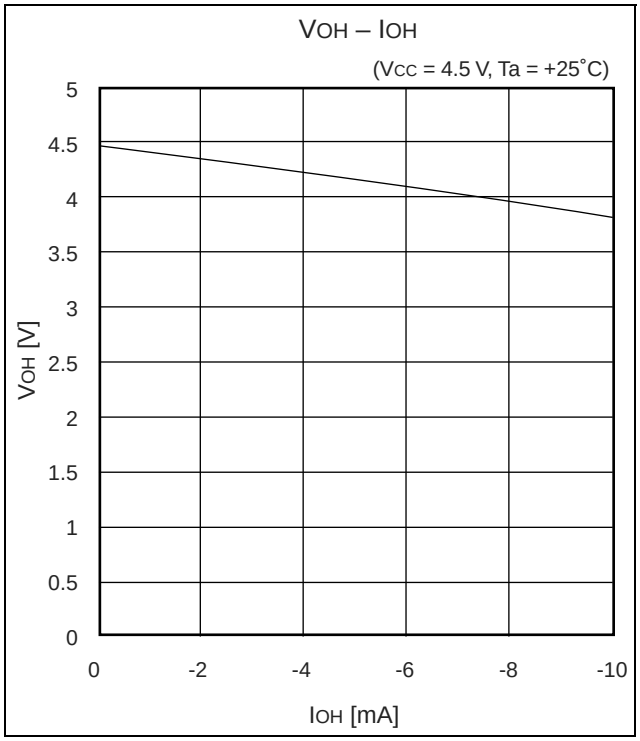


11.5.4 Error

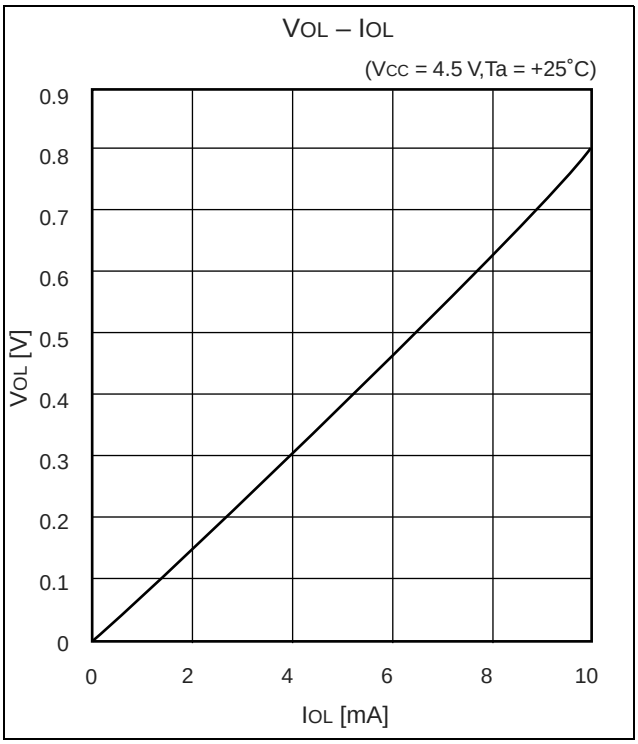
The smaller the | AVRH − AVRL |, the greater the error would become relatively.

12. Example Characteristics

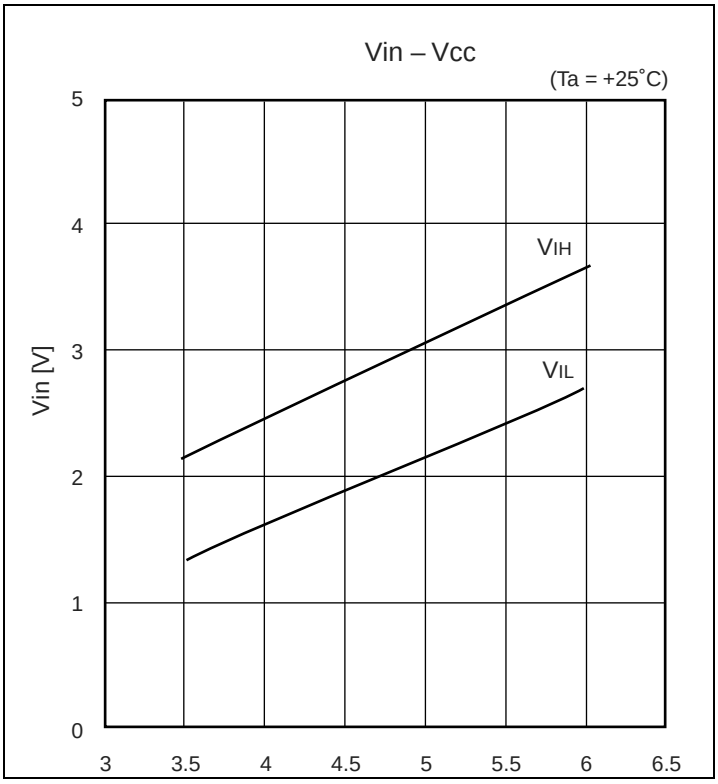
■ “H” level output voltage



■ “L” level output voltage



■ “H” level input voltage/ “L” level input voltage (Hysterisis inpiut)



■ Power supply current (MB90F549G)