# Infineon Technologies - MB90F543GSPF-GS-9003 Datasheet

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-16LX |
| Core Size | 16-Bit |
| Speed | 16MHz |
| Connectivity | CANbus, EBI/EMI, SCI, Serial I/O, UART/USART |
| Peripherals | POR, WDT |
| Number of I/O | 81 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 6K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 8x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BQFP |
| Supplier Device Package | 100-QFP (14x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspf-gs-9003 |

## 1. Product Lineup

| Features | MB90F543G (S) /F548G (S)<br>MB90F549G (S) /F546G (S)<br>MB90F548GL(S) | MB90543G (S)<br>MB90547G (S)<br>MB90548G (S)<br>MB90549G (S) | MB90V540G |
|---|---|---|---|
| CPU | F²MC-16LX CPU | | |
| System clock | On-chip PLL clock multiplier (×1, ×2, ×3, ×4, 1/2 when PLL stop)<br>Minimum instruction exection time : 62.5 ns (machine clock 16MHz, 4MHz osc. four times multiplied by PLL) | | |
| ROM | Flash memory<br>MB90F543G(S)/F548G(S) / F548GL(S) : 128 Kbytes<br>MB90F549G(S)/F546G(S) : 256 Kbytes | MASK ROM :<br>MB90547G(S): 64 Kbytes<br>MB90543G(S)/548G(S): 128 Kbytes<br>MB90549G(S): 256 Kbytes | External |
| RAM | MB90F548G(S)/F548GL(S): 4 Kbytes<br>MB90F543G (S) /F549G(S) : 6 Kbytes<br>MB90F546G(S) : 8 Kbytes | MB90547G(S): 2 Kbytes<br>MB90548G(S): 4 Kbytes<br>MB90543G(S)/549G(S): 6 Kbytes | 8 Kbytes |
| Clocks | MB90F543G/F548G/F549G/F546G/F548GL :<br>Two clocks system<br>MB90F543GS/F548GS/F549GS/F546GS/F548GLS :<br>One clock system | MB90543G/547G/548G/549G : Two clocks system<br>MB90543GS/547GS/548GS/549GS :<br>One clock system | Two clocks system*1 |
| Operating voltage range | *3 | | |
| Temperature range | −40 °C to 105 °C | | |
| Package | QFP100, LQFP100 | | PGA-256 |
| Emulator-specify power supply*2 | — | | None |
| UART0 | Full duplex double buffer<br>Support asynchronous/synchronous (with start/stop bit) transfer<br>Baud rate : 4808/5208/9615/10417/19230/38460/62500/500000 bps (asynchronous)<br>500 K/1 M/2 Mbps (synchronous) at System clock = 16 MHz | | |
| UART1 (SCI) | Full duplex double buffer<br>Asynchronous (start-stop synchronized) and CLK-synchronous communication<br>Baud rate : 1202/2404/4808/9615/19230/31250/38460/62500 bps (asynchronous)<br>62.5 K/125 K/250 K/500 K/1 M/2 Mbps (synchronous) at 6, 8, 10, 12, 16 MHz | | |
| Serial I/O | Transfer can be started from MSB or LSB<br>Supports internal clock synchronized transfer and external clock synchronized transfer<br>Supports positive-edge and nagative-edge clock synchronization<br>Baud rate : 31.25 K/62.5 K/125 K/500 K/1 Mbps at System clock = 16 MHz | | |
| A/D Converter | 10-bit or 8-bit resolution<br>8 input channels<br>Conversion time : 26.3 µs (per one channel) | | |

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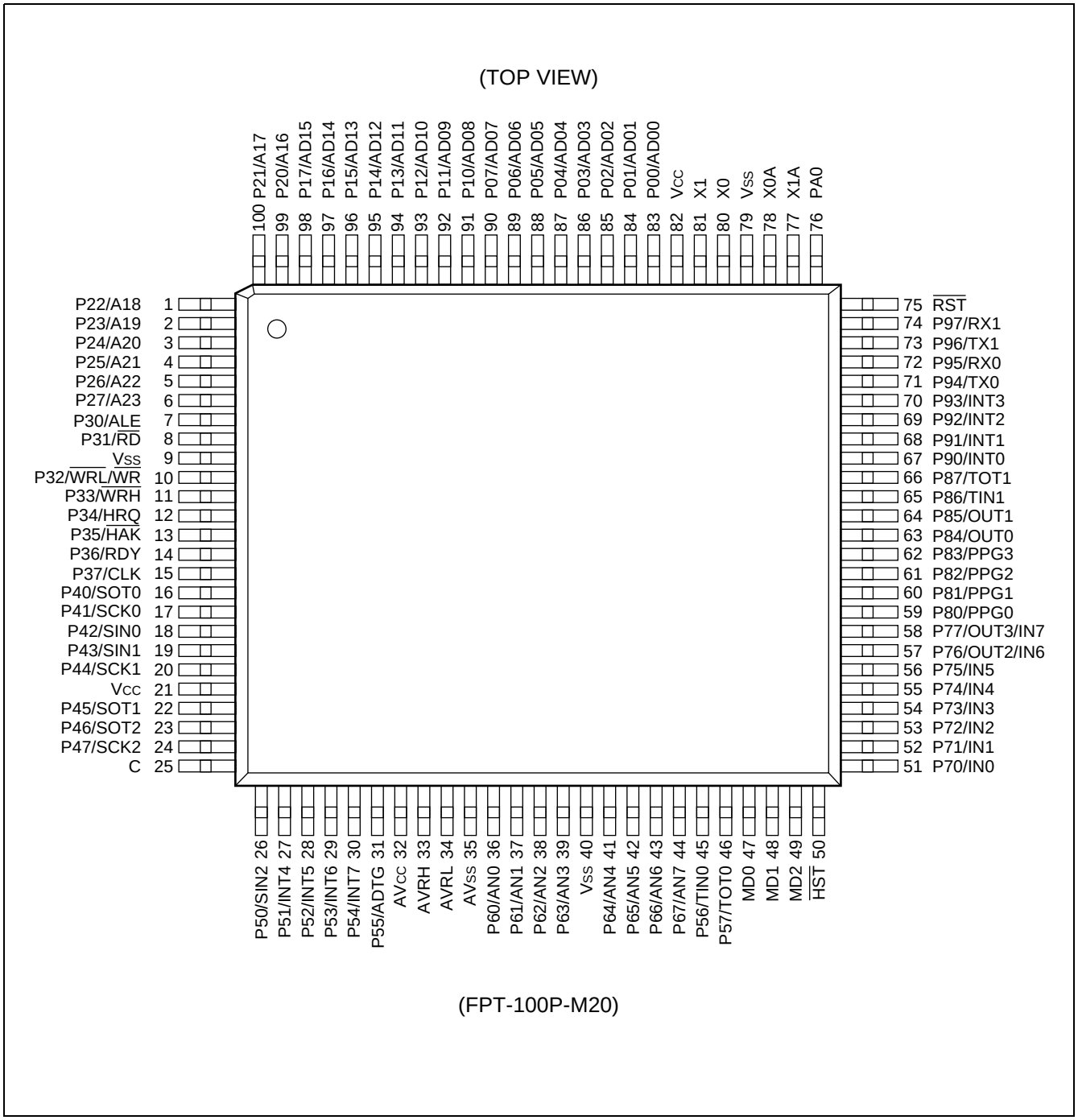
(TOP VIEW)
100 P21/A17
99 P20/A16
98 P17/AD15
97 P16/AD14
96 P15/AD13
95 P14/AD12
94 P13/AD11
93 P12/AD10
92 P11/AD09
91 P10/AD08
90 P07/AD07
89 P06/AD06
88 P05/AD05
87 P04/AD04
86 P03/AD03
85 P02/AD02
84 P01/AD01
83 P00/AD00
82 VCC
81 X1
80 X0
79 VSS
78 X0A
77 X1A
76 PA0
P22/A18 1
P23/A19 2
P24/A20 3
P25/A21 4
P26/A22 5
P27/A23 6
P30/ALE 7
P31/RD 8
VSS 9
P32/WRL/WR 10
P33/WRH 11
P34/HRQ 12
P35/HAK 13
P36/RDY 14
P37/CLK 15
P40/SOT0 16
P41/SCK0 17
P42/SIN0 18
P43/SIN1 19
P44/SCK1 20
VCC 21
P45/SOT1 22
P46/SOT2 23
P47/SCK2 24
C 25
75 RST
74 P97/RX1
73 P96/TX1
72 P95/RX0
71 P94/TX0
70 P93/INT3
69 P92/INT2
68 P91/INT1
67 P90/INT0
66 P87/TOT1
65 P86/TIN1
64 P85/OUT1
63 P84/OUT0
62 P83/PPG3
61 P82/PPG2
60 P81/PPG1
59 P80/PPG0
58 P77/OUT3/IN7
57 P76/OUT2/IN6
56 P75/IN5
55 P74/IN4
54 P73/IN3
53 P72/IN2
52 P71/IN1
51 P70/IN0
P50/SIN2 26
P51/INT4 27
P52/INT5 28
P53/INT6 29
P54/INT7 30
P55/ADTG 31
AVCC 32
AVRH 33
AVRL 34
AVSS 35
P60/AN0 36
P61/AN1 37
P62/AN2 38
P63/AN3 39
VSS 40
P64/AN4 41
P65/AN5 42
P66/AN6 43
P67/AN7 44
P56/TIN0 45
P57/TOT0 46
MD0 47
MD1 48
MD2 49
HST 50

(FPT-100P-M20)

## 3. Pin Description

| Pin No. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP*2 | QFP*1 | | | |
| 80<br>81 | 82<br>83 | X0<br>X1 | A<br>(Oscillation) | High speed crystal oscillator input pins |
| 78 | 80 | X0A | A<br>(Oscillation) | Low speed crystal oscillator input pins. For the one clock system parts, perfom external pull-down processing. |
| 77 | 79 | X1A | | Low speed crystal oscillator input pins. For the one clock system parts, leave it open. |
| 75 | 77 | $\overline{RST}$ | B | External reset request input pin |
| 50 | 52 | $\overline{HST}$ | C | Hardware standby input pin |
| 83 to 90 | 85 to 92 | P00 to P07 | I | General I/O port with programmable pullup. This function is enabled in the single-chip mode. |
| | | AD00 to AD07 | | I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled. |
| 91 to 98 | 93 to 100 | P10 to P17 | I | General I/O port with programmable pullup. This function is enabled in the single-chip mode. |
| | | AD08 to AD15 | | I/O pins for 8 higher bits of the external address/data bus. This function is enabled when the external bus is enabled. |
| 99 to 6 | 1 to 8 | P20 to P27 | I | General I/O port with programmable pullup. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to “1”. |
| | | A16 to A23 | | 8-bit I/O pins for A16 to A23 at the external address/data bus. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to “0”. |
| 7 | 9 | P30 | I | General I/O port with programmable pullup. This function is enabled in the single-chip mode. |
| | | ALE | | Address latch enable output pin. This function is enabled when the external bus is enabled. |
| 8 | 10 | P31 | I | General I/O port with programmable pullup. This function is enabled in the single-chip mode. |
| | | $\overline{RD}$ | | Read strobe output pin for the data bus. This function is enabled when the external bus is enabled. |
| 10 | 12 | P32 | I | General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the $\overline{WR}$/$\overline{WRL}$ pin output is disabled. |
| | | $\overline{WRL}$ | | Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{WR}$/$\overline{WRL}$ pin output are enabled. $\overline{WRL}$ is write-strobe output pin for the lower 8 bits of the data bus in 16-bit access. $\overline{WR}$ is write-strobe output pin for the 8 bits of the data bus in 8-bit access. |
| | | $\overline{WR}$ | | |

*(Continued)*

| Pin No. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP*2 | QFP*1 | | | |
| 11 | 13 | P33 | I | General I/O port with programmable pullup. This function is enabled in the single-chip mode, external bus 8-bit mode or when WRH pin output is disabled. |
| | | $\overline{\text{WRH}}$ | | Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{\text{WRH}}$ output pin is enabled. |
| 12 | 14 | P34 | I | General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled. |
| | | HRQ | | Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled. |
| 13 | 15 | P35 | I | General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled. |
| | | $\overline{\text{HAK}}$ | | Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled. |
| 14 | 16 | P36 | I | General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled. |
| | | RDY | | Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled. |
| 15 | 17 | P37 | H | General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the CLK output is disabled. |
| | | CLK | | CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled. |
| 16 | 18 | P40 | G | General I/O port. This function is enabled when UART0 disables the serial data output. |
| | | SOT0 | | Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output. |
| 17 | 19 | P41 | G | General I/O port. This function is enabled when UART0 disables serial clock output. |
| | | SCK0 | | Serial clock I/O pin for UART0. This function is enabled when UART0 enables the serial clock output. |
| 18 | 20 | P42 | G | General I/O port. This function is always enabled. |
| | | SIN0 | | Serial data input pin for UART0. Set the corresponding Port Direction Register to input if this function is used. |
| 19 | 21 | P43 | G | General I/O port. This function is always enabled. |
| | | SIN1 | | Serial data input pin for UART1. Set the corresponding Port Direction Register to input if this function is used. |

*(Continued)*

| Pin No. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP*2 | QFP*1 | | | |
| 46 | 48 | P57 | D | General I/O port. This function is enabled when the 16-bit reload timers 0 disables the output. |
| | | TOT0 | | Output pin for the 16-bit reload timers 0. This function is enabled when the 16-bit reload timers 0 enables the output. |
| 51 to 56 | 53 to 58 | P70 to P75 | D | General I/O ports. This function is always enabled. |
| | | IN0 to IN5 | | Trigger input pins for input captures ICU0 to ICU5. Set the corresponding Port Direction Register to input if this function is used. |
| 57 , 58 | 59 , 60 | P76 , P77 | D | General I/O ports. This function is enabled when the OCU disables the waveform output. |
| | | OUT2 , OUT3 | | Event output pins for output compares OCU2 and OCU3. This function is enabled when the OCU enables the waveform output. |
| | | IN6 , IN7 | | Trigger input pins for input captures ICU6 and ICU7. Set the corresponding Port Direction Register to input and disable the OCU waveform output if this function is used. |
| 59 to 62 | 61 to 64 | P80 to P83 | D | General I/O ports. This function is enabled when 8/16-bit PPG disables the waveform output. |
| | | PPG0 to PPG3 | | Output pins for 8/16-bit PPGs. This function is enabled when 8/16-bit PPG enables the waveform output. |
| 63 , 64 | 65 , 66 | P84 , P85 | D | General I/O ports. This function is enabled when the OCU disables the waveform output. |
| | | OUT0 , OUT1 | | Waveform output pins for output compares OCU0 and OCU1. This function is enabled when the OCU enables the waveform output. |
| 65 | 67 | P86 | D | General I/O port. This function is always enabled. |
| | | TIN1 | | Input pin for the 16-bit reload timers 1. Set the corresponding Port Direction Register to input if this function is used. |
| 66 | 68 | P87 | D | General I/O port. This function is enabled when the 16-bit reload timers 1 disables the output. |
| | | TOT1 | | Output pin for the 16-bit reload timers 1.This function is enabled when the 16-bit reload timers 1 enables the output. |
| 67 to 70 | 69 to 72 | P90 to P93 | D | General I/O port. This function is always enabled. |
| | | INT0 to INT3 | | External interrupt request input pins for INT0 to INT3. Set the corresponding Port Direction Register to input if this function is used. |
| 71 | 73 | P94 | D | General I/O port. This function is enabled when CAN0 disables the output. |
| | | TX0 | | TX output pin for CAN0. This function is enabled when CAN0 enables the output. |

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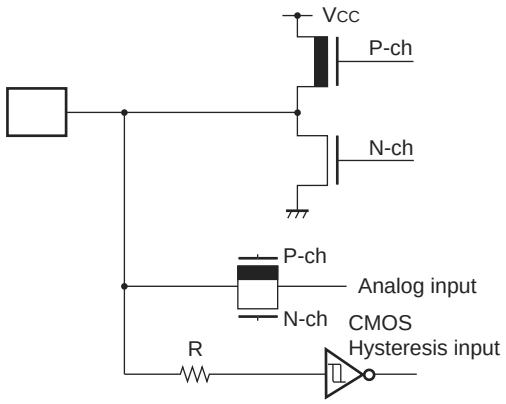
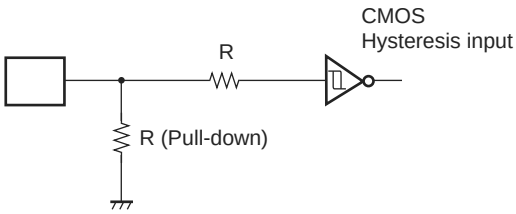
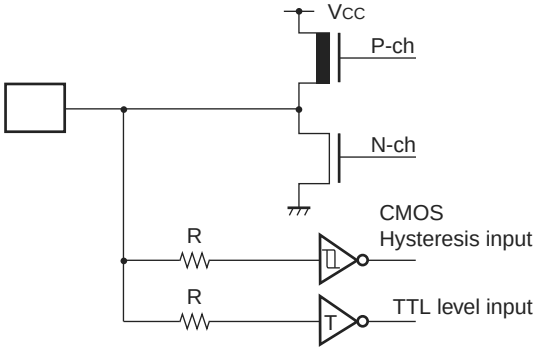
*(Continued)*

| Pin No. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP*2 | QFP*1 | | | |
| 72 | 74 | P95 | D | General I/O port. This function is always enabled. |
| | | RX0 | | RX input pin for CAN0 Interface. When the CAN function is used, output from the other functions must be stopped. |
| 73 | 75 | P96 | D | General I/O port. This function is enabled when CAN1 disables the output. |
| | | TX1 | | TX output pin for CAN1. This function is enabled when CAN1 enables the output (only MB90540G series) . |
| 74 | 76 | P97 | D | General I/O port. This function is always enabled. |
| | | RX1 | | RX input pin for CAN1 Interface. When the CAN function is used, output from the other functions must be stopped (only MB90540G series) . |
| 76 | 78 | PA0 | D | General I/O port. This function is always enabled. |
| 32 | 34 | $AV_{CC}$ | Power supply | Power supply pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to $AV_{CC}$ is applied to $V_{CC}$. |
| 35 | 37 | $AV_{SS}$ | Power supply | Power supply pin for the A/D Converter. |
| 33 | 35 | AVRH | Power supply | External reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to $AV_{CC}$. |
| 34 | 36 | AVRL | Power supply | External reference voltage input pin for the A/D Converter. |
| 47, 48 | 49, 50 | MD0, MD1 | C | Input pins for specifying the operating mode. The pins must be directly connected to $V_{CC}$ or $V_{SS}$. |
| 49 | 51 | MD2 | F | Input pin for specifying the operating mode. The pin must be directly connected to $V_{CC}$ or $V_{SS}$. |
| 25 | 27 | C | — | Power supply stabilization capacitor pin. It should be connected externally to an 0.1 µF ceramic capacitor. |
| 21, 82 | 23, 84 | $V_{CC}$ | Power supply | Input pin for power supply (5.0 V) . |
| 9, 40, 79 | 11, 42, 81 | $V_{SS}$ | Power supply | Input pin for power supply (0.0 V) . |

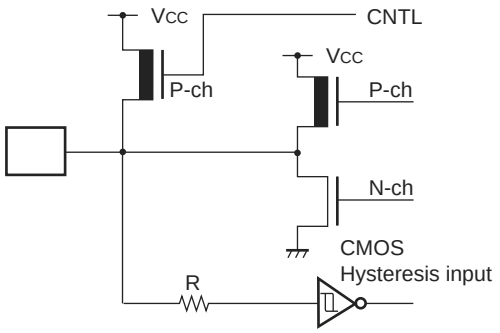
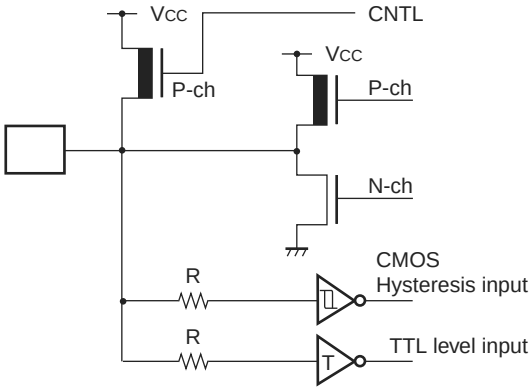
*1 : FPT-100P-M06

*2 : FPT-100P-M20

| Circuit type | Diagram | Remarks |
|---|---|---|
| E |  | ■ CMOS level output<br>■ CMOS Hysteresis input<br>■ Analog input |
| F |  | ■ CMOS Hysteresis input<br>■ Pull-down Resistor : 50 kΩ approx. (except Flash devices) |
| G |  | ■ CMOS level output<br>■ CMOS Hysteresis input<br>■ TTL level input (Flash devices in Flash writer mode only) |

*(Continued)*

*(Continued)*

| Circuit type | Diagram | Remarks |
|---|---|---|
| H |  | ■ CMOS level output<br>■ CMOS Hysteresis input<br>■ Programmable pull-up resistor : 50 kΩ approx. |
| I |  | ■ CMOS level output<br>■ CMOS Hysteresis input<br>■ TTL level input (Flash devices in Flash writer mode only)<br>■ Programmable pullup resistor : 50 kΩ approx. |

**(6) Pull-up/down resistors**

The MB90540G/545G Series does not support internal pull-up/down resistors (except Port0 − Port3 : pull-up resistors) . Use external components where needed.

**(7) Crystal Oscillator Circuit**

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via the shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuits do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation.

**(8) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs**

Make sure to turn on the A/D converter power supply ($AV_{CC}$, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply ($V_{CC}$) .

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or $AV_{CC}$ (turning on/off the analog and digital power supplies simultaneously is acceptable) .

**(9) Connection of Unused Pins of A/D Converter**

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

**(10) N.C. Pin**

The N.C. (internally connected) pin must be opened for use.

**(11) Notes on Energization**

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μs or more (0.2 V to 2.7 V) .

*(Continued)*

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC}$ = 3.5 V to 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = −40 °C to +105 °C)

| Parameter | Symbol | Pin name | Condition | Value | | | Units | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current* | $I_{CC}$ | $V_{CC}$ | Internal frequency : 16 MHz, At normal operating | − | 40 | 55 | mA | |
| | | | Internal frequency : 16 MHz, At Flash programming/erasing | − | 50 | 70 | mA | Flash device |
| | $I_{CCS}$ | | Internal frequency : 16 MHz, At sleep mode | − | 12 | 20 | mA | |
| | $I_{CTS}$ | | $V_{CC}$ = 5.0 V ± 10%, Internal frequency : 2 MHz, At pseudo timer mode | − | 300 | 600 | µA | |
| | | | | − | 600 | 1100 | µA | MB90F548GL (S) only |
| | | | | − | 200 | 400 | µA | MB90543G(S)/547G(S)/548(S) only |
| | $I_{CCL}$ | | Internal frequency : 8 kHz, At sub operation, $T_A$ = 25 °C | − | 400 | 750 | µA | MB90F548GL only |
| | | | | − | 50 | 100 | µA | MASK ROM |
| | | | | − | 150 | 300 | µA | Flash device |
| | $I_{CCLS}$ | | Internal frequency : 8 kHz, At sub sleep, $T_A$ = 25 °C | − | 15 | 40 | µA | |
| | $I_{CCT}$ | | Internal frequency : 8 kHz, At timer mode, $T_A$ = 25 °C | − | 7 | 25 | µA | |
| | $I_{CCH1}$ | | At stop, $T_A$ = 25 °C | − | 5 | 20 | µA | |
| | $I_{CCH2}$ | | At hardware standby mode, $T_A$ = 25 °C | − | 50 | 100 | µA | |
| Input capacity | $C_{IN}$ | Other than $AV_{CC}$, $AV_{SS}$, AVRH, AVRL, C, $V_{CC}$, $V_{SS}$ | − | − | 5 | 15 | pF | |

* : The power supply current testing conditions are when using the external clock.

## 11.4 AC Characteristics

### 11.4.1 Clock Timing

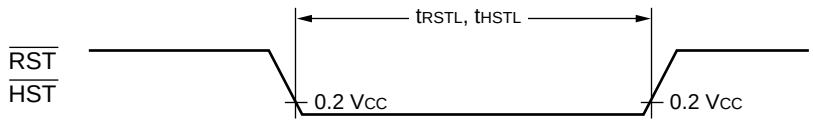
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC}$ = 3.5 V to 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = −40 °C to +105 °C)

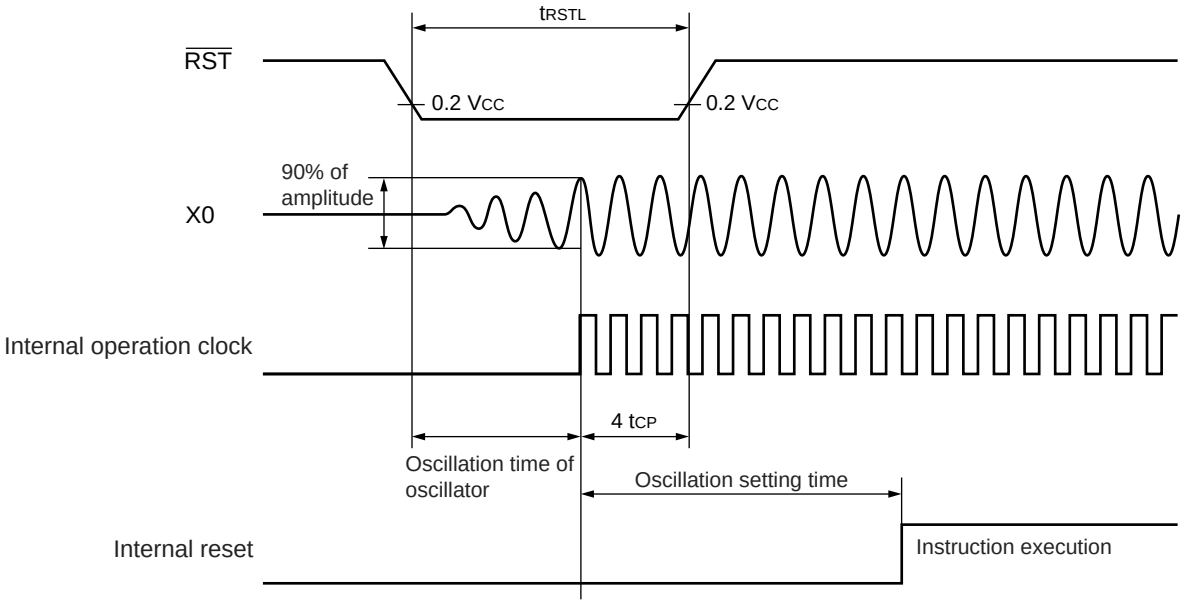
| Parameter | Symbol | Pin name | Value | | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Oscillation frequency | $f_C$ | X0, X1 | 3 | — | 16 | MHz | No multiplier<br>When using an oscillator circuit<br>$V_{CC}$ = 5.0 V ± 10% |
| | | | 8 | — | 16 | MHz | PLL multiplied by 1<br>When using an oscillator circuit<br>$V_{CC}$ = 5.0 V ± 10% |
| | | | 4 | — | 8 | MHz | PLL multiplied by 2<br>When using an oscillator circuit<br>$V_{CC}$ = 5.0 V ± 10% |
| | | | 3 | — | 5.33 | MHz | PLL multiplied by 3<br>When using an oscillator circuit<br>$V_{CC}$ = 5.0 V ± 10% |
| | | | 3 | — | 4 | MHz | PLL multiplied by 4<br>When using an oscillator circuit<br>$V_{CC}$ = 5.0 V ± 10% |
| | | | 3 | — | 5 | MHz | When using an oscillator circuit<br>$V_{CC}$ < 4.5 V(MB90F548GL(S)/543G(S)/547G(S)/548G(S)) |
| | | | 3 | — | 16 | MHz | No multiplier<br>When using an external clock |
| | | | 8 | — | 16 | MHz | PLL multiplied by 1<br>When using an external clock |
| | | | 4 | — | 8 | MHz | PLL multiplied by 2<br>When using an external clock |
| | | | 3 | — | 5.33 | MHz | PLL multiplied by 3<br>When using an external clock |
| | | | 3 | — | 4 | MHz | PLL multiplied by 4<br>When using an external clock |
| | $f_{CL}$ | X0A, X1A | — | 32.768 | — | kHz | |

*(Continued)*

■ In under normal operation, pseudo timer mode, sub-clock mode, sub-sleep mode, timer mode




■ In stop mode



### 11.4.5 Bus Timing (Read)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC}$ = 3.5 V to 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = − 40 °C to + 105 °C)

| Parameter | Symbol | Pin name | Condition | Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| ALE pulse width | $t_{LHLL}$ | ALE | | $t_{CP}/2 - 20$ | − | ns | |
| Valid address → ALE↓ time | $t_{AVLL}$ | ALE, A16 to A23, AD00 to AD15 | | $t_{CP}/2 - 20$ | − | ns | |
| ALE↓ → Address valid time | $t_{LLAX}$ | ALE, AD00 to AD15 | | $t_{CP}/2 - 15$ | − | ns | |
| Valid address → $\overline{RD}$↓ time | $t_{AVRL}$ | A16 toA23, AD00 to AD15, $\overline{RD}$ | | $t_{CP} - 15$ | − | ns | |
| Valid address → Valid data input | $t_{AVDV}$ | A16 to A23, AD00 to AD15 | | − | $5\ t_{CP}/2 - 60$ | ns | |
| $\overline{RD}$ pulse width | $t_{RLRH}$ | RD | − | $3\ t_{CP}/2 - 20$ | − | ns | |
| $\overline{RD}$↓ → Valid data input | $t_{RLDV}$ | $\overline{RD}$, AD00 to AD15 | | − | $3\ t_{CP}/2 - 60$ | ns | |
| $\overline{RD}$↑ → Data hold time | $t_{RHDX}$ | $\overline{RD}$, AD00 to AD15 | | 0 | − | ns | |
| $\overline{RD}$↑ → ALE↑ time | $t_{RHLH}$ | $\overline{RD}$, ALE | | $t_{CP}/2 - 15$ | − | ns | |
| $\overline{RD}$↑ → Address valid time | $t_{RHAX}$ | $\overline{RD}$, A16 to A23 | | $t_{CP}/2 - 10$ | − | ns | |
| Valid address → CLK↑ time | $t_{AVCH}$ | A16 to A23, AD00 to AD15, CLK | | $t_{CP}/2 - 20$ | − | ns | |
| $\overline{RD}$↓ → CLK↑ time | $t_{RLCH}$ | $\overline{RD}$, CLK | | $t_{CP}/2 - 20$ | − | ns | |
| ALE↓ → $\overline{RD}$↓ time | $t_{LLRL}$ | ALE, $\overline{RD}$ | | $t_{CP}/2 - 15$ | − | ns | |

### 11.4.7 Ready Input Timing

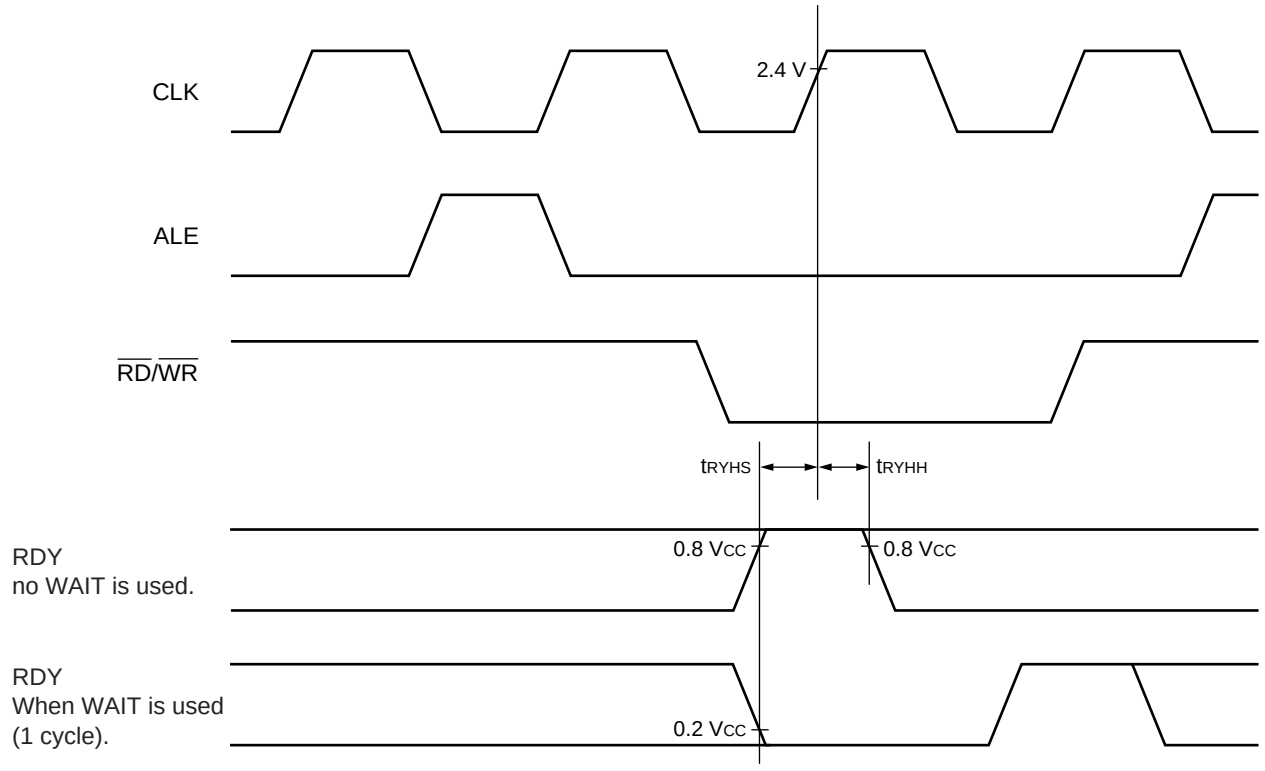
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC}$ = 3.5 V to 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = − 40 °C to + 105 °C)

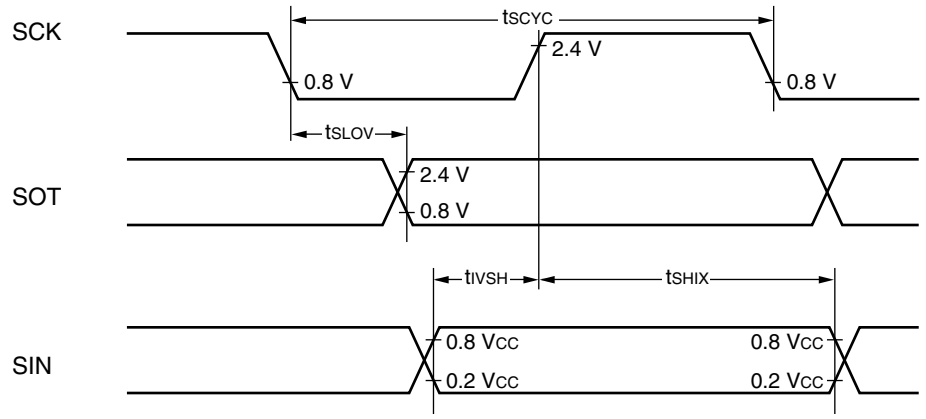
| Parameter | Symbol | Pin name | Condition | Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| RDY setup time | $t_{RYHS}$ | RDY | — | 45 | — | ns | |
| RDY hold time | $t_{RYHH}$ | RDY | | 0 | — | ns | |

Note : If the RDY setup time is insufficient, use the auto-ready function.

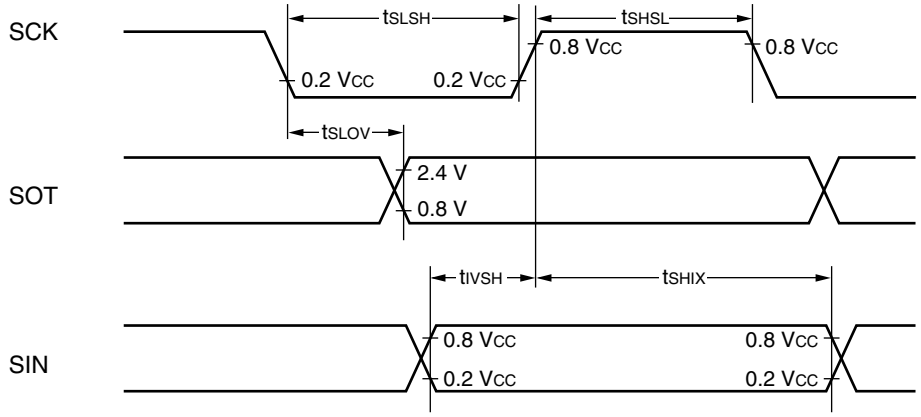
■ **Ready Input Timing**



■ Internal Shift Clock Mode

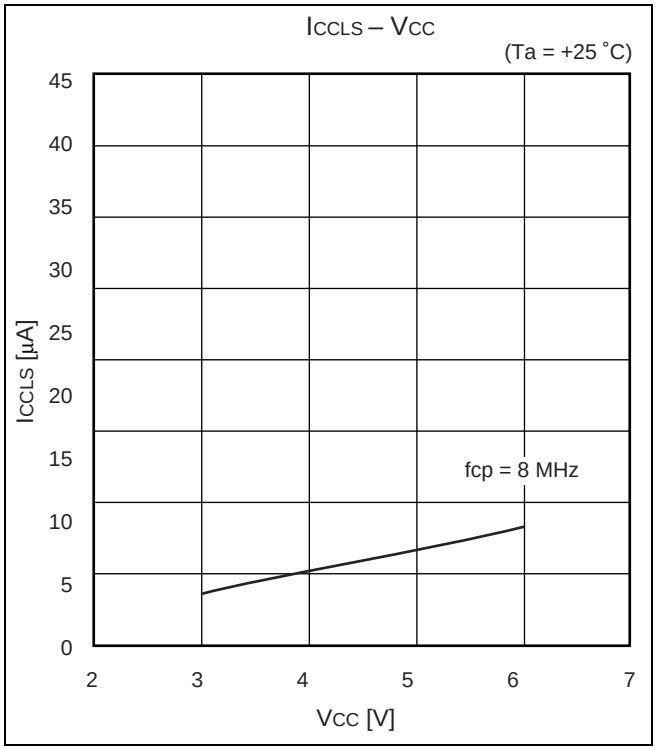


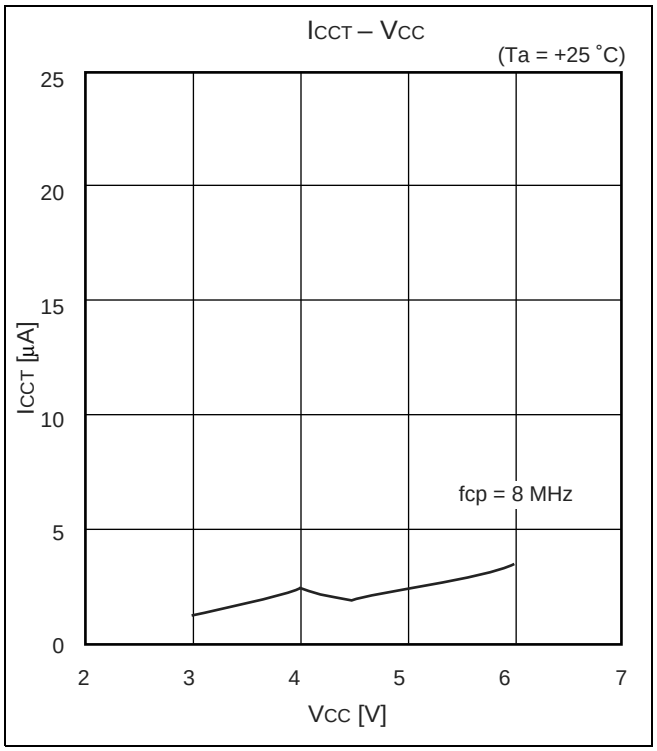

■ External Shift Clock Mode

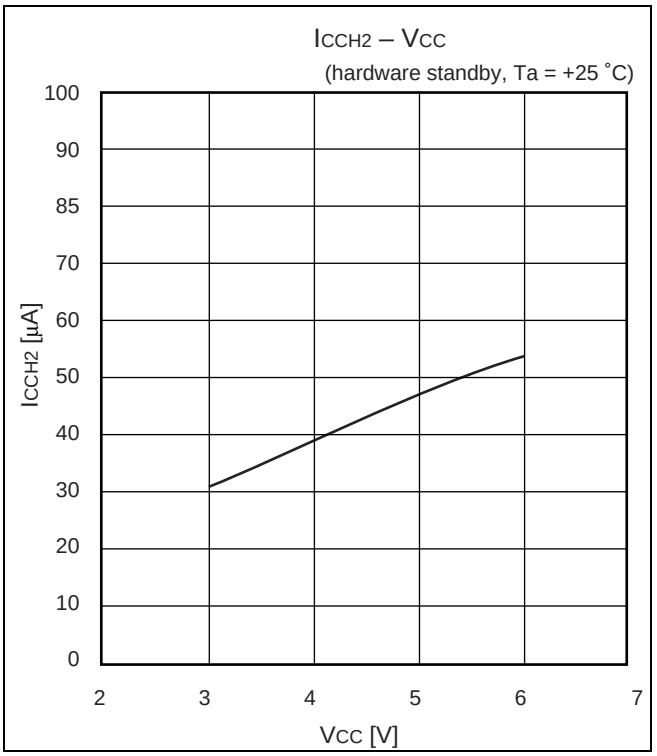


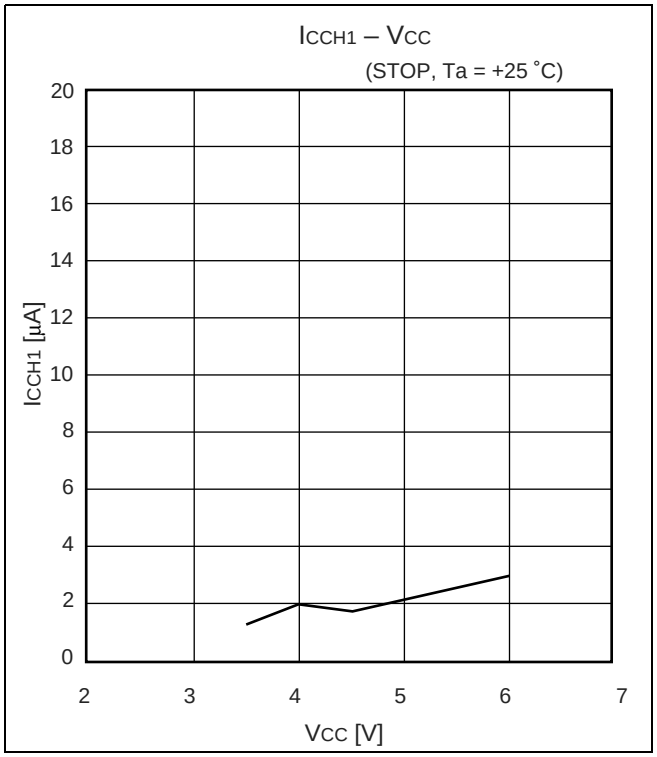
## 11.6 Flash Memory Program/Erase Characteristics

| Parameter | Condition | Value | | | Units | Remarks | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | | |
| Sector erase time | $T_A$ = + 25 °C<br>$V_{CC}$ = 5.0 V | — | 1 | 15 | s | Excludes 00H programming prior erasure | |
| Chip erase time | | — | 5 | — | s | MB90F543G (S) /F548G (S) /F548GL (S) | Excludes 00H programming prior erasure |
| | | | 7 | — | s | MB90F549G (S) /F546G (S) | |
| Word (16 bit width) programming time | | — | 16 | 3,600 | µs | Excludes system-level overhead | |
| Erase/Program cycle | — | 10,000 | — | — | cycle | | |

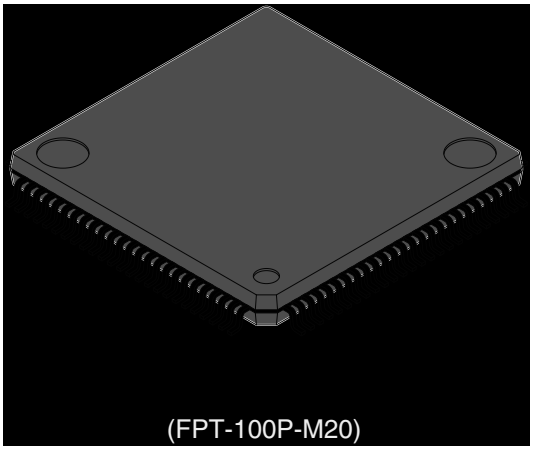

ICCLS – VCC
(Ta = +25 ˚C)
ICCLS [µA]
45
40
35
30
25
20
15
10
5
0
fcp = 8 MHz
2
3
4
5
6
7
VCC [V]


ICCT – VCC
(Ta = +25 ˚C)
ICCT [µA]
25
20
15
10
5
0
fcp = 8 MHz
2
3
4
5
6
7
VCC [V]

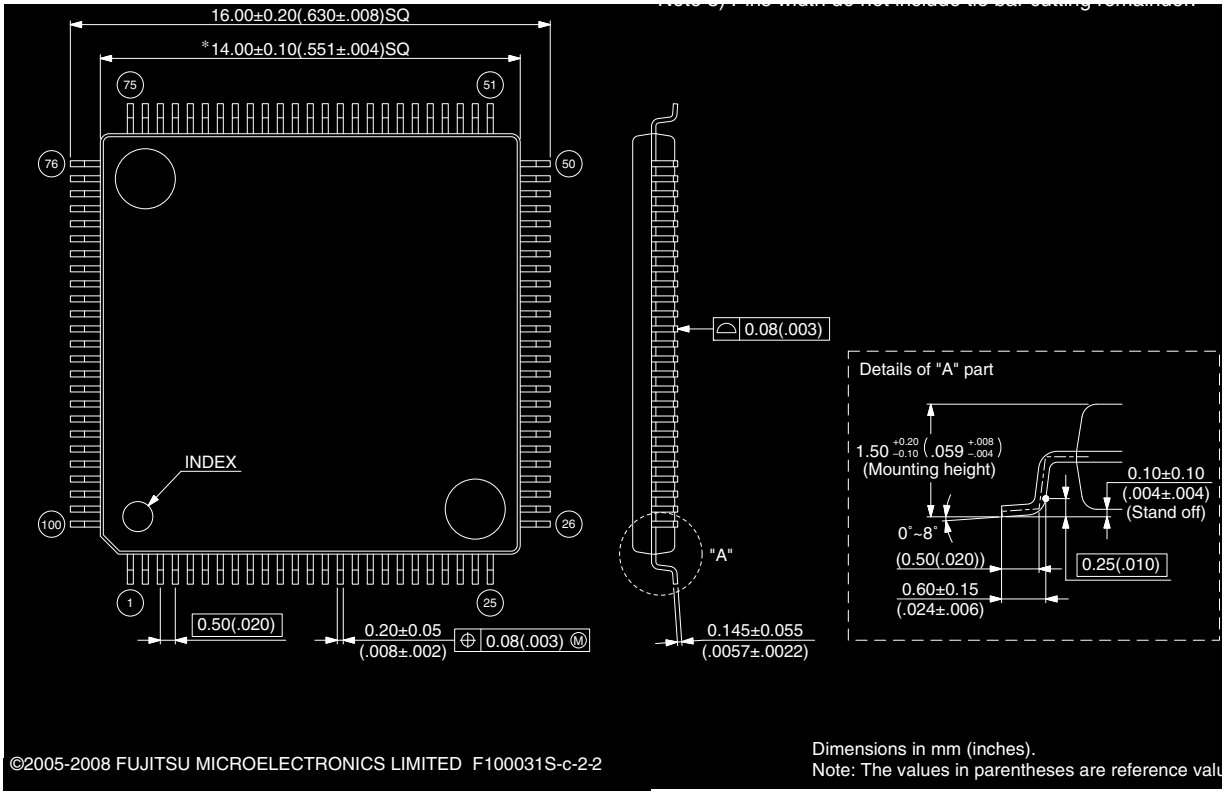

ICCH2 – VCC
(hardware standby, Ta = +25 ˚C)
ICCH2 [µA]
100
90
85
70
60
50
40
30
20
10
0
2
3
4
5
6
7
VCC [V]


ICCH1 – VCC
(STOP, Ta = +25 ˚C)
ICCH1 [µA]
20
18
16
14
12
10
8
6
4
2
0
2
3
4
5
6
7
VCC [V]

*(Continued)*



(FPT-100P-M20)



## 15. Major Changes

Spansion Publication Number: DS07-13703-7E

| Section | Change Results |
|---|---|
| ■ PRODUCT LINEUP | Changed the name in peripheral resource.<br>16-bit I/O Timer → 16-bit Free-run Timer |
| ■ I/O CIRCUIT TYPE | Changed the name of input typ.<br>Hysteresis → CMOS Hysteresis<br>HYS → CMOS Hysteresis |
| ■ BLOCK DIAGRAM | Changed the arrow direction of SOT1 signal at UART1(SCI).<br>"← →" (input/output) → "←" (output) |
| ■ I/O MAP | Changed the text of "Note". |
| ■ INTERRUPT MAP | Changed the name of peripheral resource of the pin number: #19.<br>I/O Timer → 16-bit Free-run Timer |
| ■ ELECTRICAL CHARACTERISTICS<br>2. Recommended Conditions | Changed the remarks of "parameter: Power supply voltage". |
| 3. DC Characteristics | Changed the maximum value of symbol : VILM of parameter: Input voltage.<br>$V_{CC}$ + 0.3 → $V_{SS}$ + 0.3 |
| | Added the following remarks for parameter : Pull-down resistance.<br>Except Flash device |
| 4. AC Characteristics<br>(1) Clock Timing | Added the value when using an external clock in Oscillation frequency and Clock cycle time on (1) Clock Timing for parameter. |
| | Added the item of A/D converter operation range in figure of "■ Guaranteed PLL operation range" |
| (3) Reset and Hardware Standby Input Timing | Changed the following item.<br>(3) Reset and Hardware Standby Input Timing Remarks:<br>In sub-clock mode, sub-sleep mode, timer mode<br>$2t_{CP}$ → $2t_{LCP}$ |
| (4) Power On Reset | Changed as follows;<br>Due to repetitive operation → Waiting time until power-on |
| 5. A/D Converter | Changed the unit of Zero transition voltage and Full scale transition voltage.<br>mV → V |
| ■ ORDERING INFORMATION | Added the MB90F548GLPMC in Part Numbers. |

**NOTE: Please see "Document History" about later revised information.**

## Document History

**Document Title: MB90F543G(S)/546G(S)/548G(S)/549G(S)/549G(S)/V540G/MB90543G(S)/547G(S)/548G(S)/F548GL(S) CMOS F2MC-16LX MB90540G/545G Series 16-bit Proprietary Microcontroller**
**Document Number: 002-07696**

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | — | AKIH | 11/13/2008 | Migrated to Cypress and assigned document number 002-07696.<br>No change to document contents or format. |
| *A | 5537115 | AKIH | 11/30/2016 | Updated to Cypress template |

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