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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspf-gs-9004

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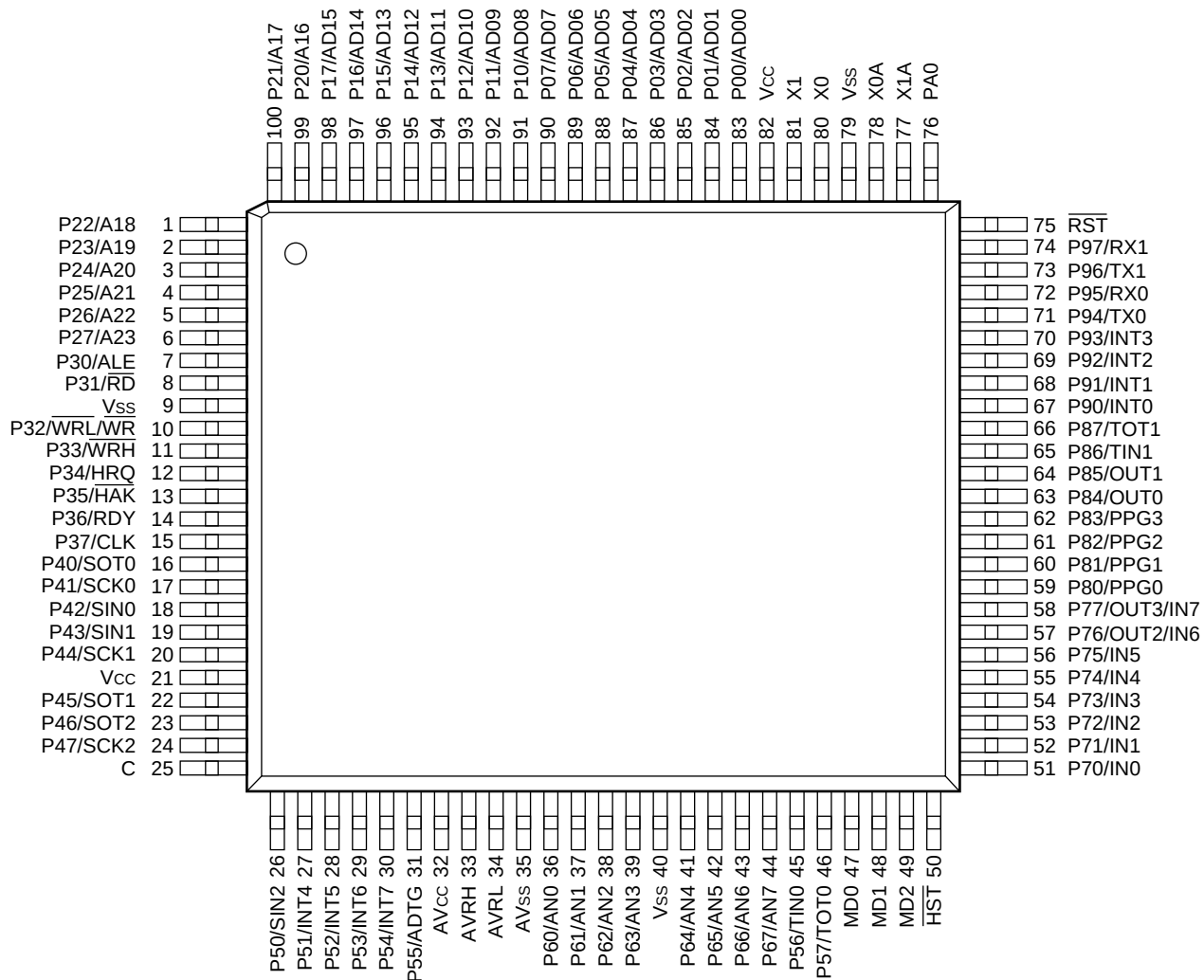
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Features	MB90F543G (S) /F548G (S) MB90F549G (S) /F546G (S) MB90F548GL(S)	MB90543G (S) MB90547G (S) MB90548G (S) MB90549G (S)	MB90V540G
16-bit Reload Timer (2 channels)	Operation clock frequency : $f_{sys}/2^1$, $f_{sys}/2^3$, $f_{sys}/2^5$ (f_{sys} = System clock frequency) Supports External Event Count function Signals an interrupt when overflow		
16-bit Free-run Timer	Supports Timer Clear when a match with Output Compare (Channel 0) Operation clock freq. : $f_{sys}/2^2$, $f_{sys}/2^4$, $f_{sys}/2^6$, $f_{sys}/2^8$ (f_{sys} = System clock freq.)		
16-bit Output Compare (4 channels)	Signals an interrupt when a match with 16-bit Free-run Timer Four 16-bit compare registers A pair of compare registers can be used to generate an output signal		
16-bit Input Capture (8 channels)	Rising edge, falling edge or rising & falling edge sensitive Four 16-bit Capture registers Signals an interrupt upon external event		
8/16-bit Programmable Pulse Generator (4 channels)	Supports 8-bit and 16-bit operation modes Eight 8-bit reload counters Eight 8-bit reload registers for L pulse width Eight 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter 4 output pins Operation clock freq. : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$ or $128 \mu s @ f_{osc} = 4 \text{ MHz}$ (f_{sys} = System clock frequency, f_{osc} = Oscillation clock frequency)		
CAN Interface MB90540G series : 2 channels MB90545G series : 1 channel	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's supports multiple messages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps		
32 kHz Sub-clock	Sub-clock for low power operation		
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive		
External bus interface	External access using the selectable 8-bit or 16-bit bus is enabled (external bus mode.)		
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs and schmitt trigger inputs Bit-wise programmable as input/output or peripheral signal Sub-clock for 32 kHz Sub clock low power operation		
Flash Memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Erase-Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block Block protection by externally programmed voltage		

*1 : If the one clock system is used, equip X0A and X1A with clocks from the tool side.

(TOP VIEW)

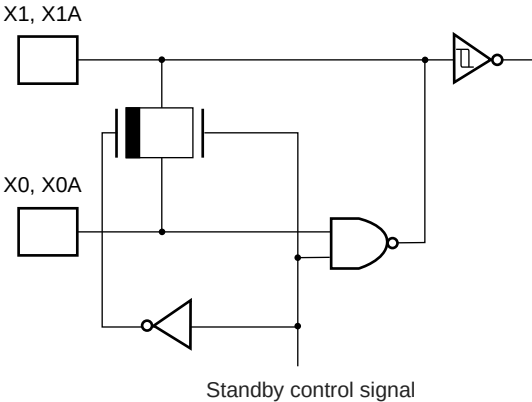
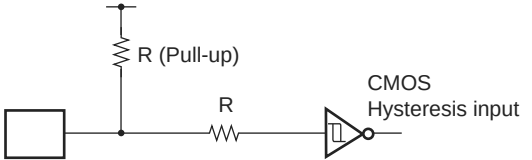
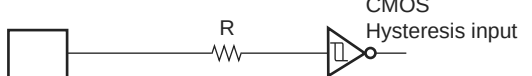
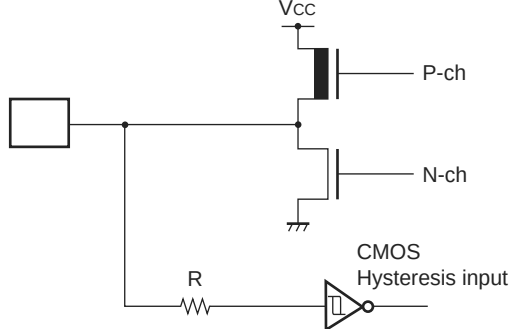


(FPT-100P-M20)

Pin No.		Pin name	Circuit type	Function
LQFP ²	QFP ¹			
11	13	P33	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode, external bus 8-bit mode or when WRH pin output is disabled.
		$\overline{\text{WRH}}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the WRH output pin is enabled.
12	14	P34	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.
13	15	P35	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.
14	16	P36	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.
		RDY		Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.
15	17	P37	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the CLK output is disabled.
		CLK		CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled.
16	18	P40	G	General I/O port. This function is enabled when UART0 disables the serial data output.
		SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.
17	19	P41	G	General I/O port. This function is enabled when UART0 disables serial clock output.
		SCK0		Serial clock I/O pin for UART0. This function is enabled when UART0 enables the serial clock output.
18	20	P42	G	General I/O port. This function is always enabled.
		SIN0		Serial data input pin for UART0. Set the corresponding Port Direction Register to input if this function is used.
19	21	P43	G	General I/O port. This function is always enabled.
		SIN1		Serial data input pin for UART1. Set the corresponding Port Direction Register to input if this function is used.

(Continued)

4. I/O Circuit Type

Circuit type	Diagram	Remarks
A	 Standby control signal	■ High-speed oscillation feedback resistor : 1 MΩ approx. ■ Low-speed oscillation feedback resistor: 10 MΩ approx.
B	 R (Pull-up) CMOS Hysteresis input	■ CMOS Hysteresis input ■ Pull-up resistor : 50 kΩ approx.
C	 CMOS Hysteresis input	■ CMOS Hysteresis input
D	 Vcc P-ch N-ch CMOS Hysteresis input R	■ CMOS level output ■ CMOS Hysteresis input

(Continued)

(6) Pull-up/down resistors

The MB90540G/545G Series does not support internal pull-up/down resistors (except Port0 – Port3 : pull-up resistors) . Use external components where needed.

(7) Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via the shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuits do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation.

(8) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC} , AV_{RH} , AV_{RL}) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}) .

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AV_{RH} or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable) .

(9) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AV_{RH} = V_{SS}$.

(10) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

(11) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μ s or more (0.2 V to 2.7 V) .

Address	Register	Abbreviation	Access	Resource name	Initial value
47 _H to 4B _H	Prohibited				
4C _H	Input capture control status register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0 _B
4D _H	Input capture control status register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0 _B
4E _H	Input capture control status register 4/5	ICS45	R/W	Input Capture 4/5	0 0 0 0 0 0 0 0 _B
4F _H	Input capture control status register 6/7	ICS67	R/W	Input Capture 6/7	0 0 0 0 0 0 0 0 _B
50 _H	Timer control status register 0	TMCSR0	R/W	16-bit Reload Timer 0	0 0 0 0 0 0 0 0 _B
51 _H	Timer control status register 0	TMCSR0	R/W		____ 0 0 0 0 _B
52 _H	Timer register 0/reload register 0	TMR0/TMRLR0	R/W		XXXXXXXX _B
53 _H	Timer register 0/reload register 0	TMR0/TMRLR0	R/W		XXXXXXXX _B
54 _H	Timer control status register 1	TMCSR1	R/W	16-bit Reload Timer 1	0 0 0 0 0 0 0 0 _B
55 _H	Timer control status register 1	TMCSR1	R/W		____ 0 0 0 0 _B
56 _H	Timer register 1/reload register 1	TMR1/TMRLR1	R/W		XXXXXXXX _B
57 _H	Timer register 1/reload register 1	TMR1/TMRLR1	R/W		XXXXXXXX _B
58 _H	Output compare control status register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 __ 0 0 _B
59 _H	Output compare control status register 1	OCS1	R/W		__ __ 0 0 0 0 0 _B
5A _H	Output compare control status register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 __ 0 0 _B
5B _H	Output compare control status register 3	OCS3	R/W		__ __ 0 0 0 0 0 _B
5C _H to 6B _H	Prohibited				
6C _H	Timer Data register	TCDT	R/W	I/O Timer	0 0 0 0 0 0 0 0 _B
6D _H	Timer Data register	TCDT	R/W		0 0 0 0 0 0 0 0 _B
6E _H	Timer Control register	TCCS	R/W		0 0 0 0 0 0 0 0 _B
6F _H	ROM mirror function selection register	ROMM	R/W	ROM Mirror	____ _ 1 _B
70 _H to 7F _H	Reserved for CAN 0 Interface.				
80 _H to 8F _H	Reserved for CAN 1 Interface.				
90 _H to 9D _H	Prohibited				
9E _H	Program address detection control status register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0 _B
9F _H	Delayed interrupt/release register	DIRR	R/W	Delayed Interrupt	____ _ 0 _B
A0 _H	Low-power mode control register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0 _B
A1 _H	Clock selection register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0 _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
A2 _H to A4 _H	Prohibited				
A5 _H	Automatic ready function select register	ARSR	W	External Memory Access	0 0 1 1 _ _ 0 0 _B
A6 _H	External address output control register	HACR	W		0 0 0 0 0 0 0 0 _B
A7 _H	Bus control signal selection register	ECSR	W		0 0 0 0 0 0 0 _ _B
A8 _H	Watchdog Timer control register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1 _B
A9 _H	Time Base Timer Control register	TBTC	R/W	Time Base Timer	1 - - 0 0 1 0 0 _B
AA _H	Watch timer control register	WTC	R/W	Watch Timer	1 X 0 0 0 0 0 0 _B
AB _H to AD _H	Prohibited				
AE _H	Flash memory control status register (Flash only, otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0 _B
AF _H	Prohibited				
B0 _H	Interrupt control register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1 _B
B1 _H	Interrupt control register 01	ICR01	R/W		0 0 0 0 0 1 1 1 _B
B2 _H	Interrupt control register 02	ICR02	R/W		0 0 0 0 0 1 1 1 _B
B3 _H	Interrupt control register 03	ICR03	R/W		0 0 0 0 0 1 1 1 _B
B4 _H	Interrupt control register 04	ICR04	R/W		0 0 0 0 0 1 1 1 _B
B5 _H	Interrupt control register 05	ICR05	R/W		0 0 0 0 0 1 1 1 _B
B6 _H	Interrupt control register 06	ICR06	R/W		0 0 0 0 0 1 1 1 _B
B7 _H	Interrupt control register 07	ICR07	R/W		0 0 0 0 0 1 1 1 _B
B8 _H	Interrupt control register 08	ICR08	R/W		0 0 0 0 0 1 1 1 _B
B9 _H	Interrupt control register 09	ICR09	R/W		0 0 0 0 0 1 1 1 _B
BA _H	Interrupt control register 10	ICR10	R/W		0 0 0 0 0 1 1 1 _B
BB _H	Interrupt control register 11	ICR11	R/W		0 0 0 0 0 1 1 1 _B
BC _H	Interrupt control register 12	ICR12	R/W		0 0 0 0 0 1 1 1 _B
BD _H	Interrupt control register 13	ICR13	R/W		0 0 0 0 0 1 1 1 _B
BE _H	Interrupt control register 14	ICR14	R/W		0 0 0 0 0 1 1 1 _B
BF _H	Interrupt control register 15	ICR15	R/W		0 0 0 0 0 1 1 1 _B
C0 _H to FF _H	External				

Address	Register	Abbreviation	Access	Resource name	Initial value
1FF0 _H	Program address detection register 0	PADR0	R/W	Address Match Detection Function	XXXXXXXX _B
1FF1 _H	Program address detection register 0	PADR0	R/W		XXXXXXXX _B
1FF2 _H	Program address detection register 0	PADR0	R/W		XXXXXXXX _B
1FF3 _H	Program address detection register 1	PADR1	R/W		XXXXXXXX _B
1FF4 _H	Program address detection register 1	PADR1	R/W		XXXXXXXX _B
1FF5 _H	Program address detection register 1	PADR1	R/W		XXXXXXXX _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
3900 _H	Reload L	PRLLO	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX _B
3901 _H	Reload H	PRLH0	R/W		XXXXXXXX _B
3902 _H	Reload L	PRLLO1	R/W		XXXXXXXX _B
3903 _H	Reload H	PRLH1	R/W		XXXXXXXX _B
3904 _H	Reload L	PRLLO2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX _B
3905 _H	Reload H	PRLH2	R/W		XXXXXXXX _B
3906 _H	Reload L	PRLLO3	R/W		XXXXXXXX _B
3907 _H	Reload H	PRLH3	R/W		XXXXXXXX _B
3908 _H	Reload L	PRLLO4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX _B
3909 _H	Reload H	PRLH4	R/W		XXXXXXXX _B
390A _H	Reload L	PRLLO5	R/W		XXXXXXXX _B
390B _H	Reload H	PRLH5	R/W		XXXXXXXX _B
390C _H	Reload L	PRLLO6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX _B
390D _H	Reload H	PRLH6	R/W		XXXXXXXX _B
390E _H	Reload L	PRLLO7	R/W		XXXXXXXX _B
390F _H	Reload H	PRLH7	R/W		XXXXXXXX _B
3910 _H to 3917 _H	Reserved				
3918 _H	Input Capture Register 0	IPCP0	R	Input Capture 0/1	XXXXXXXX _B
3919 _H	Input Capture Register 0	IPCP0	R		XXXXXXXX _B
391A _H	Input Capture Register 1	IPCP1	R		XXXXXXXX _B
391B _H	Input Capture Register 1	IPCP1	R		XXXXXXXX _B
391C _H	Input Capture Register 2	IPCP2	R	Input Capture 2/3	XXXXXXXX _B
391D _H	Input Capture Register 2	IPCP2	R		XXXXXXXX _B
391E _H	Input Capture Register 3	IPCP3	R		XXXXXXXX _B
391F _H	Input Capture Register 3	IPCP3	R		XXXXXXXX _B
3920 _H	Input Capture Register 4	IPCP4	R	Input Capture 4/5	XXXXXXXX _B
3921 _H	Input Capture Register 4	IPCP4	R		XXXXXXXX _B
3922 _H	Input Capture Register 5	IPCP5	R		XXXXXXXX _B
3923 _H	Input Capture Register 5	IPCP5	R		XXXXXXXX _B
3924 _H	Input Capture Register 6	IPCP6	R	Input Capture 6/7	XXXXXXXX _B
3925 _H	Input Capture Register 6	IPCP6	R		XXXXXXXX _B
3926 _H	Input Capture Register 7	IPCP7	R		XXXXXXXX _B
3927 _H	Input Capture Register 7	IPCP7	R		XXXXXXXX _B

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
3928 _H	Output Compare Register 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX _B
3929 _H	Output Compare Register 0	OCCP0	R/W		XXXXXXXX _B
392A _H	Output Compare Register 1	OCCP1	R/W		XXXXXXXX _B
392B _H	Output Compare Register 1	OCCP1	R/W		XXXXXXXX _B
392C _H	Output Compare Register 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX _B
392D _H	Output Compare Register 2	OCCP2	R/W		XXXXXXXX _B
392E _H	Output Compare Register 3	OCCP3	R/W		XXXXXXXX _B
392F _H	Output Compare Register 3	OCCP3	R/W		XXXXXXXX _B
3930 _H to 39FF _H	Reserved				
3A00 _H to 3AFF _H	Reserved for CAN 0 Interface.				
3B00 _H to 3BFF _H	Reserved for CAN 0 Interface.				
3C00 _H to 3CFF _H	Reserved for CAN 1 Interface.				
3D00 _H to 3DFF _H	Reserved for CAN 1 Interface.				
3E00 _H to 3FFF _H	Reserved				

■ Read/write notation

R/W : Reading and writing permitted
R : Read-only
W : Write-only

■ Initial value notation

0 : Initial value is "0".
1 : Initial value is "1".
X : Initial value is undefined.
— : Initial value is unused.

Note: Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading "X".

(Continued)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A3C _H	003C3C _H	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX _B
003A3D _H	003C3D _H				
003A3E _H	003C3E _H				XXXXX--- XXXXXXXX _B
003A3F _H	003C3F _H				
003A40 _H	003C40 _H	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX _B
003A41 _H	003C41 _H				
003A42 _H	003C42 _H				XXXXX--- XXXXXXXX _B
003A43 _H	003C43 _H				
003A44 _H	003C44 _H	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX _B
003A45 _H	003C45 _H				
003A46 _H	003C46 _H				XXXXX--- XXXXXXXX _B
003A47 _H	003C47 _H				
003A48 _H	003C48 _H	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX _B
003A49 _H	003C49 _H				
003A4A _H	003C4A _H				XXXXX--- XXXXXXXX _B
003A4B _H	003C4B _H				
003A4C _H	003C4C _H	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX _B
003A4D _H	003C4D _H				
003A4E _H	003C4E _H				XXXXX--- XXXXXXXX _B
003A4F _H	003C4F _H				
003A50 _H	003C50 _H	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX _B
003A51 _H	003C51 _H				
003A52 _H	003C52 _H				XXXXX--- XXXXXXXX _B
003A53 _H	003C53 _H				
003A54 _H	003C54 _H	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX _B
003A55 _H	003C55 _H				
003A56 _H	003C56 _H				XXXXX--- XXXXXXXX _B
003A57 _H	003C57 _H				
003A58 _H	003C58 _H	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX _B
003A59 _H	003C59 _H				
003A5A _H	003C5A _H				XXXXX--- XXXXXXXX _B
003A5B _H	003C5B _H				
003A5C _H	003C5C _H	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX _B
003A5D _H	003C5D _H				
003A5E _H	003C5E _H				XXXXX--- XXXXXXXX _B
003A5F _H	003C5F _H				

(Continued)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A88 _H to 003A8F _H	003C88 _H to 003C8F _H	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
003A90 _H to 003A97 _H	003C90 _H to 003C97 _H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
003A98 _H to 003A9F _H	003C98 _H to 003C9F _H	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
003AA0 _H to 003AA7 _H	003CA0 _H to 003CA7 _H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
003AA8 _H to 003AAF _H	003CA8 _H to 003CAF _H	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
003AB0 _H to 003AB7 _H	003CB0 _H to 003CB7 _H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
003AB8 _H to 003ABF _H	003CB8 _H to 003CBF _H	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
003AC0 _H to 003AC7 _H	003CC0 _H to 003CC7 _H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
003AC8 _H to 003ACF _H	003CC8 _H to 003CCF _H	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
003AD0 _H to 003AD7 _H	003CD0 _H to 003CD7 _H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
003AD8 _H to 003ADF _H	003CD8 _H to 003CDF _H	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
003AE0 _H to 003AE7 _H	003CE0 _H to 003CE7 _H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
003AE8 _H to 003AEF _H	003CE8 _H to 003CEF _H	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B
003AF0 _H to 003AF7 _H	003CF0 _H to 003CF7 _H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
003AF8 _H to 003AFF _H	003CF8 _H to 003CFF _H	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

10. Interrupt Map

Interrupt cause	EI ² OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC _H	—	—
INT9 instruction	N/A	#09	FFFFD8 _H	—	—
Exception	N/A	#10	FFFFD4 _H	—	—
CAN 0 RX	N/A	#11	FFFFD0 _H	ICR00	0000B0 _H
CAN 0 TX/NS	N/A	#12	FFFFCC _H		
CAN 1 RX	N/A	#13	FFFFC8 _H	ICR01	0000B1 _H
CAN 1 TX/NS	N/A	#14	FFFFC4 _H		
External Interrupt INT0/INT1	*1	#15	FFFFC0 _H	ICR02	0000B2 _H
Time Base Timer	N/A	#16	FFFFBC _H		
16-bit Reload Timer 0	*1	#17	FFFFB8 _H	ICR03	0000B3 _H
8/10-bit A/D Converter	*1	#18	FFFFB4 _H		
16-bit Free-run Timer	N/A	#19	FFFFB0 _H	ICR04	0000B4 _H
External Interrupt INT2/INT3	*1	#20	FFFFAC _H		
Serial I/O	*1	#21	FFFFA8 _H	ICR05	0000B5 _H
8/16-bit PPG 0/1	N/A	#22	FFFFA4 _H		
Input Capture 0	*1	#23	FFFFA0 _H	ICR06	0000B6 _H
External Interrupt INT4/INT5	*1	#24	FFFF9C _H		
Input Capture 1	*1	#25	FFFF98 _H	ICR07	0000B7 _H
8/16-bit PPG 2/3	N/A	#26	FFFF94 _H		
External Interrupt INT6/INT7	*1	#27	FFFF90 _H	ICR08	0000B8 _H
Watch Timer	N/A	#28	FFFF8C _H		
8/16-bit PPG 4/5	N/A	#29	FFFF88 _H	ICR09	0000B9 _H
Input Capture 2/3	*1	#30	FFFF84 _H		
8/16-bit PPG 6/7	N/A	#31	FFFF80 _H	ICR10	0000BA _H
Output Compare 0	*1	#32	FFFF7C _H		
Output Compare 1	*1	#33	FFFF78 _H	ICR11	0000BB _H
Input Capture 4/5	*1	#34	FFFF74 _H		
Output Compare 2/3 - Input Capture 6/7	*1	#35	FFFF70 _H	ICR12	0000BC _H
16-bit Reload Timer 1	*1	#36	FFFF6C _H		
UART 0 RX	*2	#37	FFFF68 _H	ICR13	0000BD _H
UART 0 TX	*1	#38	FFFF64 _H		
UART 1 RX	*2	#39	FFFF60 _H	ICR14	0000BE _H
UART 1 TX	*1	#40	FFFF5C _H		
Flash Memory	N/A	#41	FFFF58 _H	ICR15	0000BF _H
Delayed interrupt	N/A	#42	FFFF54 _H		

(Continued)

(Continued)

*1 : The interrupt request flag is cleared by the EI²OS interrupt clear signal.

*2 : The interrupt request flag is cleared by the EI²OS interrupt clear signal. A stop request is available.

Notes :

- N/A : The interrupt request flag is not cleared by the EI²OS interrupt clear signal.
- For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.
- At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by a hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.
- If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Units	Remarks
		Min	Max		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *1
	$AVRH, AVRL$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH/AVRL, AVRH \geq AVRL$ *1
Input voltage	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Output voltage	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Maximum clamp current	I_{CLAMP}	- 2.0	+ 2.0	mA	*6
Total maximum clamp current	$\Sigma I_{CLAMP} $	—	20	mA	*6
"L" level max output current	I_{OL}	—	15	mA	*3
"L" level avg. output current	I_{OLAV}	—	4	mA	*4
"L" level max overall output current	ΣI_{OL}	—	100	mA	
"L" level avg. overall output current	ΣI_{OLAV}	—	50	mA	*5
"H" level max output current	I_{OH}	—	-15	mA	*3
"H" level avg. output current	I_{OHAV}	—	-4	mA	*4
"H" level max overall output current	ΣI_{OH}	—	-100	mA	
"H" level avg. overall output current	ΣI_{OHAV}	—	-50	mA	*5
Power consumption	P_D	—	500	mW	Flash device
		—	400	mW	MASK ROM
Operating temperature	T_A	-40	+105	°C	
Storage temperature	T_{STG}	-55	+150	°C	

*1 : AV_{CC} , $AVRH$, $AVRL$ should not exceed V_{CC} . Also, $AVRH$, $AVRL$ should not exceed AV_{CC} , and $AVRL$ does not exceed $AVRH$.

*2 : V_I and V_O should not exceed $V_{CC} + 0.3\text{ V}$. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supercedes the V_I rating.

*3 : The maximum output current is a peak value for a corresponding pin.

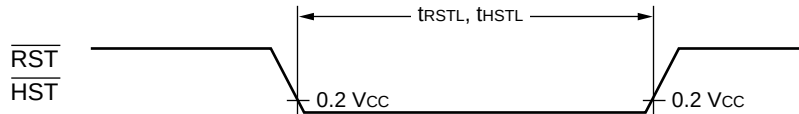
*4 : Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5 : Total average current is an average current value observed for a 100 ms period for all corresponding pins.

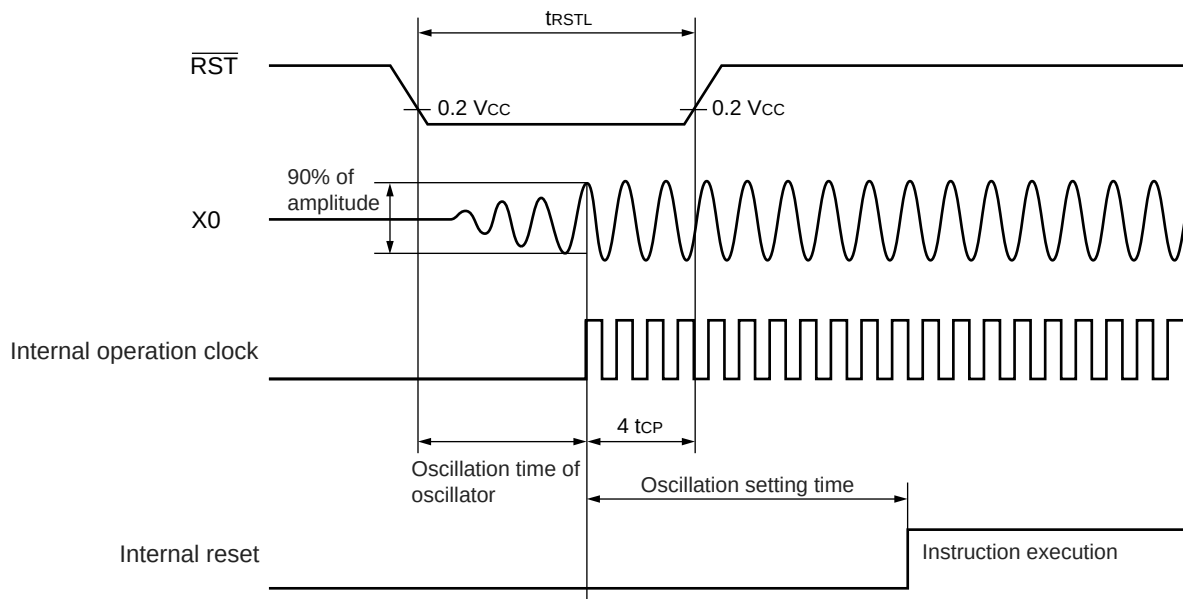
*6 :

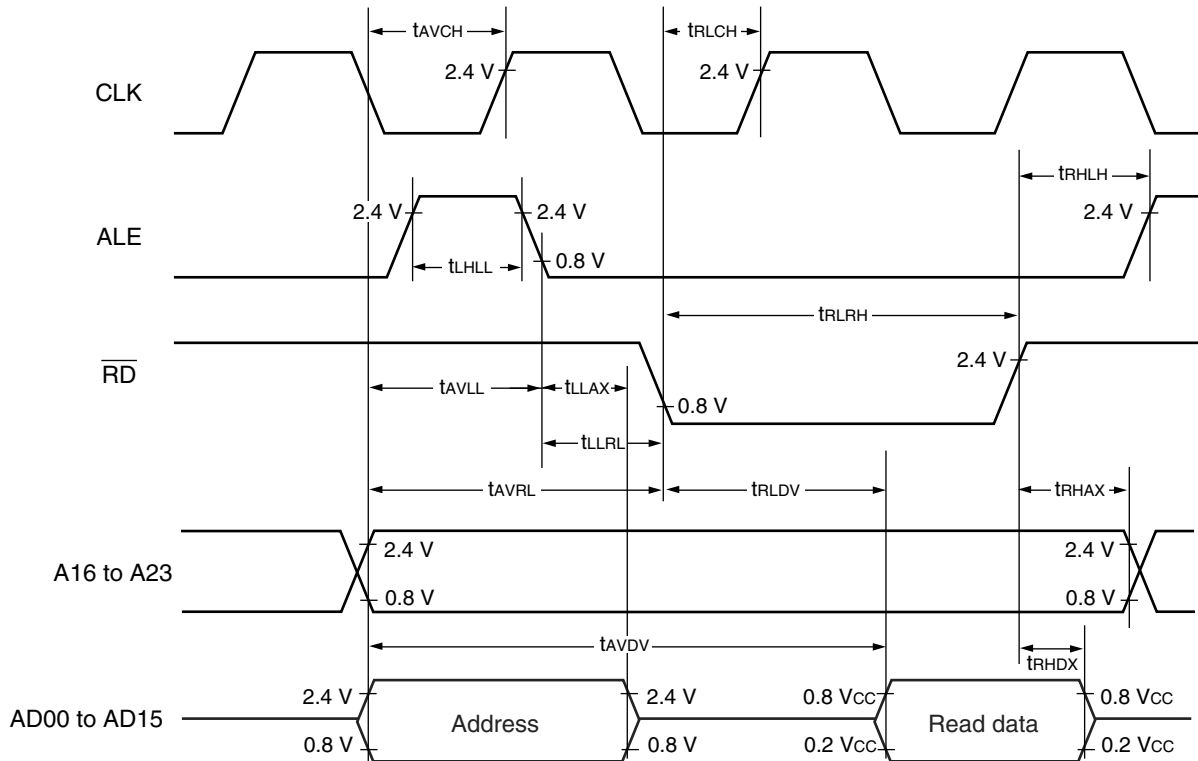
- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The + B signal should always be applied with a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the + B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a + B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- Care must be taken not to leave the + B input pin open.

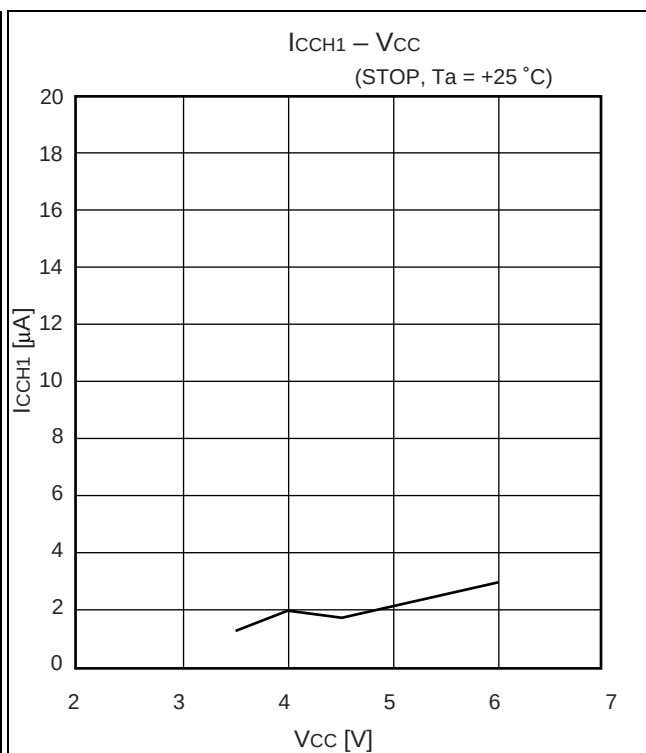
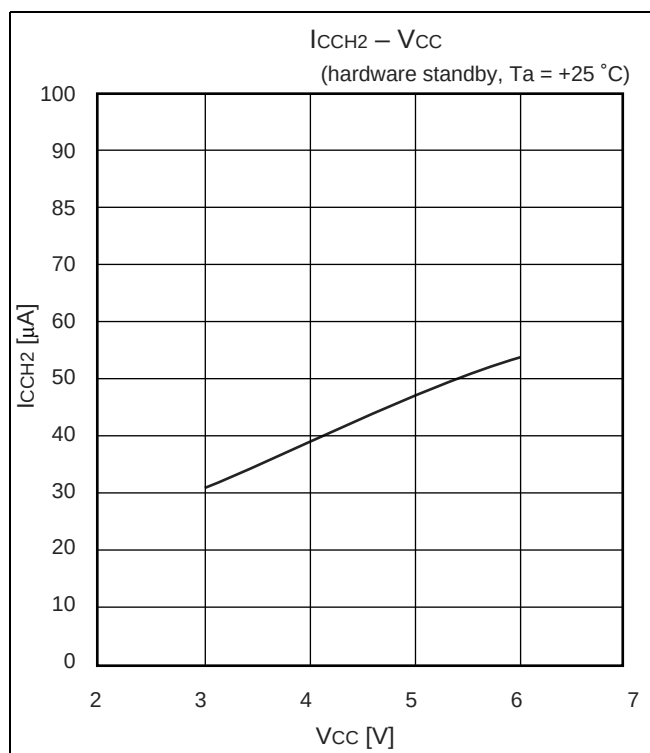
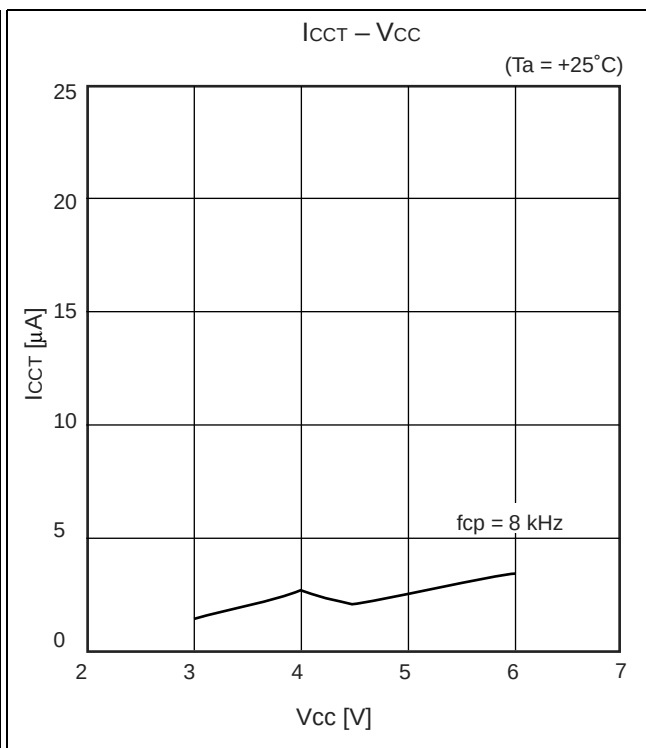
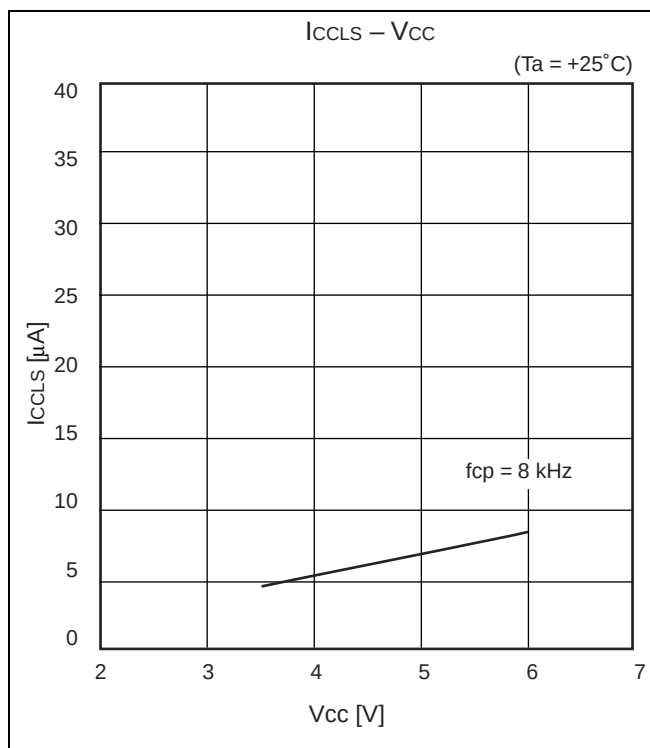
- In under normal operation, pseudo timer mode, sub-clock mode, sub-sleep mode, timer mode

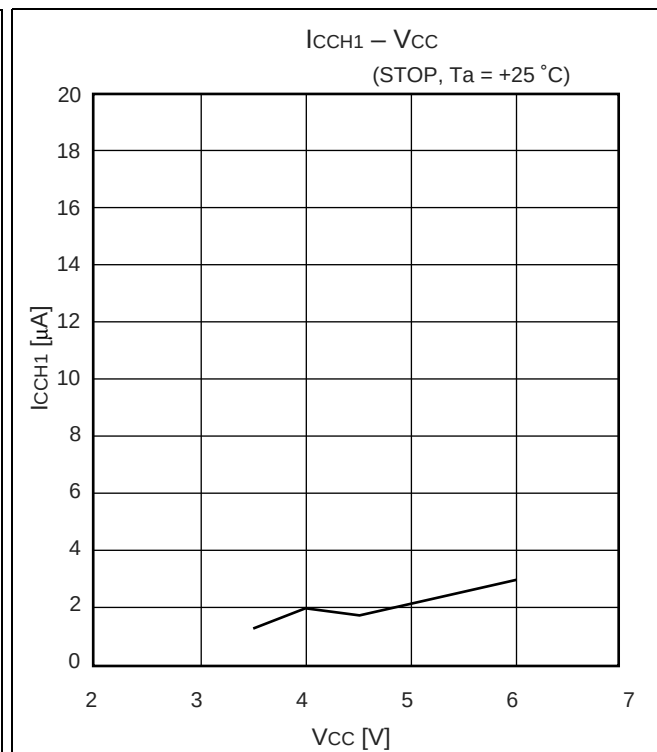
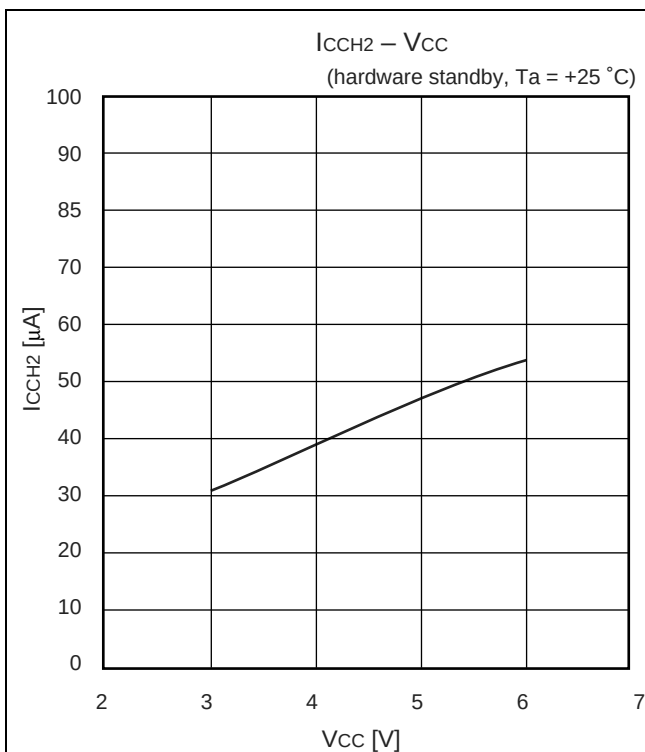
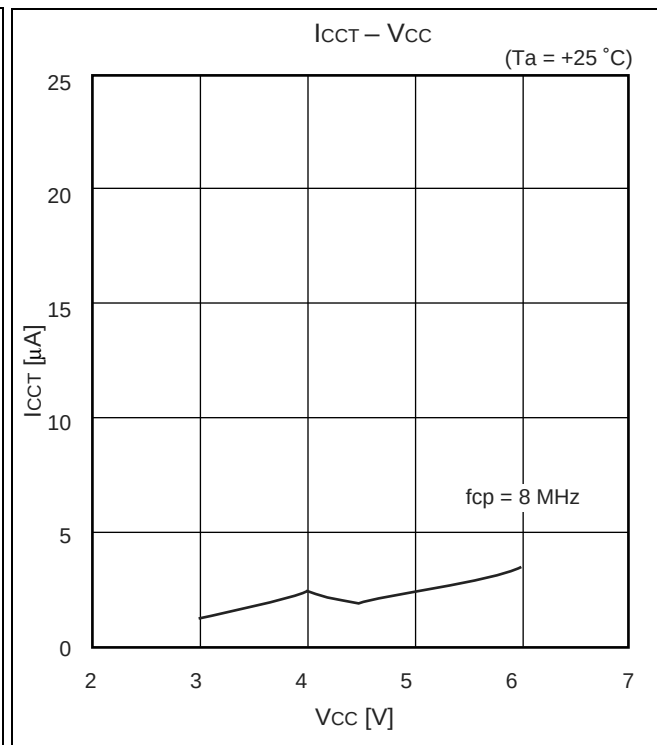
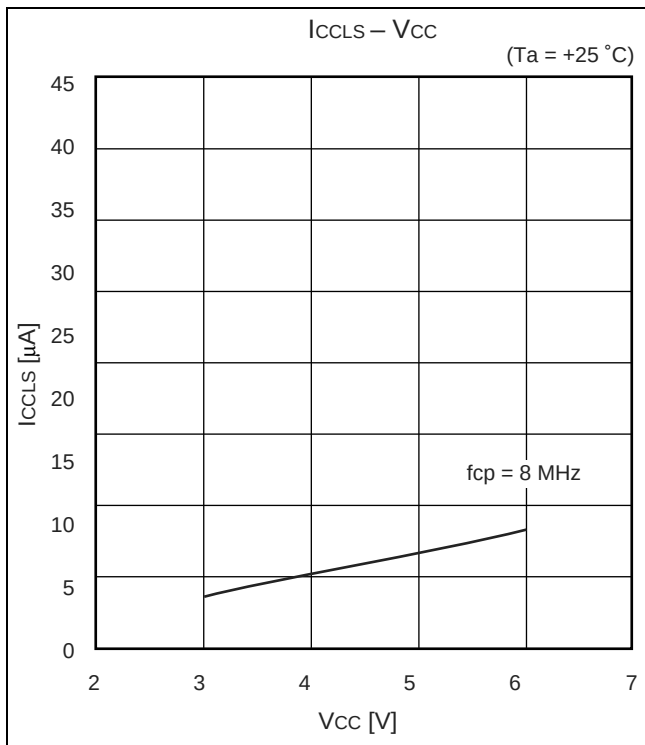


- In stop mode



■ Bus Timing (Read)






15. Major Changes

Spansion Publication Number: DS07-13703-7E

Section	Change Results
■ PRODUCT LINEUP	Changed the name in peripheral resource. 16-bit I/O Timer → 16-bit Free-run Timer
■ I/O CIRCUIT TYPE	Changed the name of input typ. Hysteresis → CMOS Hysteresis HYS → CMOS Hysteresis
■ BLOCK DIAGRAM	Changed the arrow direction of SOT1 signal at UART1(SCI). “← →” (input/output) → “←” (output)
■ I/O MAP	Changed the text of “Note”.
■ INTERRUPT MAP	Changed the name of peripheral resource of the pin number: #19. I/O Timer → 16-bit Free-run Timer
■ ELECTRICAL CHARACTERISTICS	Changed the remarks of “parameter: Power supply voltage”.
2. Recommended Conditions	
3. DC Characteristics	Changed the maximum value of symbol : VILM of parameter: Input voltage. $V_{CC} + 0.3 \rightarrow V_{SS} + 0.3$ Added the following remarks for parameter : Pull-down resistance. Except Flash device
4. AC Characteristics	Added the value when using an external clock in Oscillation frequency and Clock cycle time on (1) Clock Timing for parameter.
(1) Clock Timing	Added the item of A/D converter operation range in figure of “■ Guaranteed PLL operation range”
(3) Reset and Hardware Standby Input Timing	Changed the following item. (3) Reset and Hardware Standby Input Timing Remarks: In sub-clock mode, sub-sleep mode, timer mode $2t_{CP} \rightarrow 2t_{LCP}$
(4) Power On Reset	Changed as follows; Due to repetitive operation → Waiting time until power-on
5. A/D Converter	Changed the unit of Zero transition voltage and Full scale transition voltage. mV → V
■ ORDERING INFORMATION	Added the MB90F548GLPMC in Part Numbers.

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB90F543G(S)/546G(S)/548G(S)/549G(S)/549G(S)/V540G/MB90543G(S)/547G(S)/548G(S)/F548GL(S) CMOS F2MC-16LX MB90540G/545G Series 16-bit Proprietary Microcontroller Document Number: 002-07696				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	11/13/2008	Migrated to Cypress and assigned document number 002-07696. No change to document contents or format.
*A	5537115	AKIH	11/30/2016	Updated to Cypress template