Infineon Technologies - MB90F543GSPF-GS-9005 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspf-gs-9005

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*2 : It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*3 : Operating Voltage Range

Products	Operation guarantee range
MB90F543G(S)/F546G(S)/F548G(S)/ MB90549G(S)/F549G(S)/V540/V540G	4.5 V to 5.5 V
MB90F548GL(S)/543G(S)/547G(S)/548G(S)	3.5 V to 5.5 V

Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
11	13	P33	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode, external bus 8-bit mode or when WRH pin output is disabled.
		$\overline{\text{WRH}}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{\text{WRH}}$ output pin is enabled.
12	14	P34	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.
13	15	P35	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.
14	16	P36	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.
		RDY		Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.
15	17	P37	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the CLK output is disabled.
		CLK		CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled.
16	18	P40	G	General I/O port. This function is enabled when UART0 disables the serial data output.
		SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.
17	19	P41	G	General I/O port. This function is enabled when UART0 disables serial clock output.
		SCK0		Serial clock I/O pin for UART0. This function is enabled when UART0 enables the serial clock output.
18	20	P42	G	General I/O port. This function is always enabled.
		SIN0		Serial data input pin for UART0. Set the corresponding Port Direction Register to input if this function is used.
19	21	P43	G	General I/O port. This function is always enabled.
		SIN1		Serial data input pin for UART1. Set the corresponding Port Direction Register to input if this function is used.

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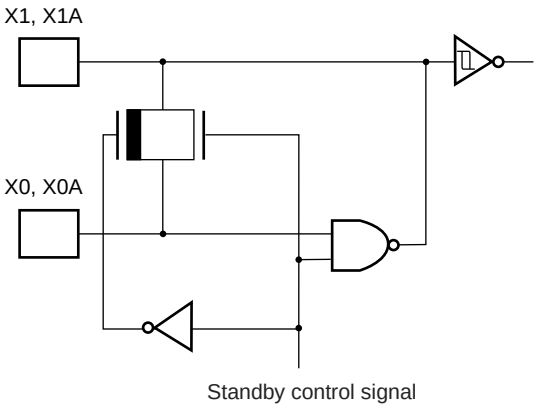
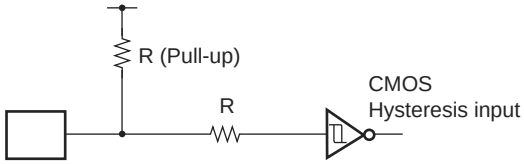
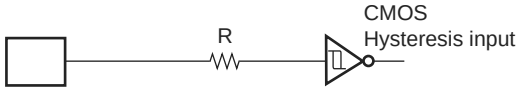
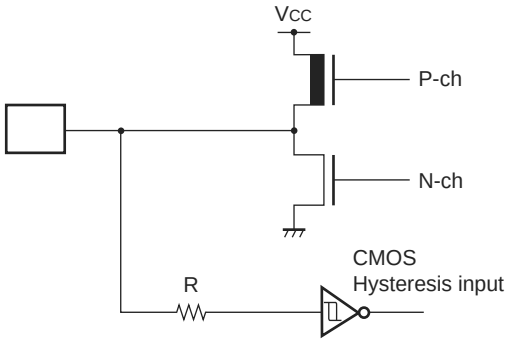
Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
72	74	P95	D	General I/O port. This function is always enabled.
		RX0		RX input pin for CAN0 Interface. When the CAN function is used, output from the other functions must be stopped.
73	75	P96	D	General I/O port. This function is enabled when CAN1 disables the output.
		TX1		TX output pin for CAN1. This function is enabled when CAN1 enables the output (only MB90540G series) .
74	76	P97	D	General I/O port. This function is always enabled.
		RX1		RX input pin for CAN1 Interface. When the CAN function is used, output from the other functions must be stopped (only MB90540G series) .
76	78	PA0	D	General I/O port. This function is always enabled.
32	34	AV_{CC}	Power supply	Power supply pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AV_{CC} is applied to V_{CC}.
35	37	AV_{SS}	Power supply	Power supply pin for the A/D Converter.
33	35	AVRH	Power supply	External reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV_{CC}.
34	36	AVRL	Power supply	External reference voltage input pin for the A/D Converter.
47, 48	49, 50	MD0, MD1	C	Input pins for specifying the operating mode. The pins must be directly connected to V_{CC} or V_{SS}.
49	51	MD2	F	Input pin for specifying the operating mode. The pin must be directly connected to V_{CC} or V_{SS}.
25	27	C	—	Power supply stabilization capacitor pin. It should be connected externally to an 0.1 µF ceramic capacitor.
21, 82	23, 84	V_{CC}	Power supply	Input pin for power supply (5.0 V) .
9, 40, 79	11, 42, 81	V_{SS}	Power supply	Input pin for power supply (0.0 V) .

*1 : FPT-100P-M06

*2 : FPT-100P-M20

4. I/O Circuit Type

Circuit type	Diagram	Remarks
A		■ High-speed oscillation feedback resistor : 1 MΩ approx. ■ Low-speed oscillation feedback resistor: 10 MΩ approx.
B		■ CMOS Hysteresis input ■ Pull-up resistor : 50 kΩ approx.
C		■ CMOS Hysteresis input
D		■ CMOS level output ■ CMOS Hysteresis input

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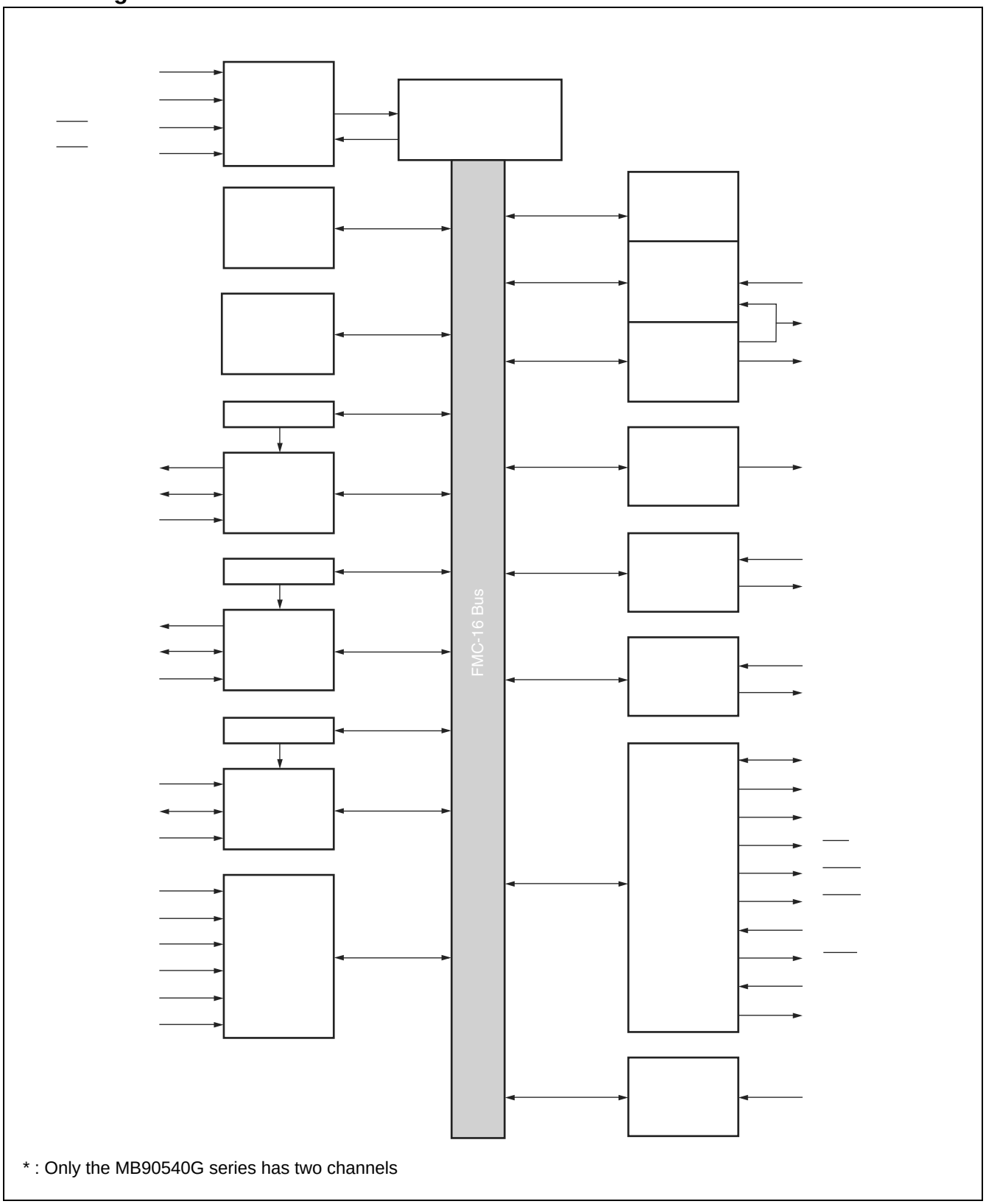
6. Block Diagram



* : Only the MB90540G series has two channels

8. I/O Map

Address	Register	Abbreviation	Access	Resource name	Initial value
00_H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX$_B$
01_H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX$_B$
02_H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX$_B$
03_H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX$_B$
04_H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX$_B$
05_H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX$_B$
06_H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX$_B$
07_H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXX$_B$
08_H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX$_B$
09_H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX$_B$
$0A_H$	Port A data register	PDRA	R/W	Port A	_ _ _ _ _ _ _X$_B$
$0B_H$ to $0F_H$	Reserved				
10_H	Port 0 direction register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0$_B$
11_H	Port 1 direction register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0$_B$
12_H	Port 2 direction register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0$_B$
13_H	Port 3 direction register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0$_B$
14_H	Port 4 direction register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0$_B$
15_H	Port 5 direction register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0$_B$
16_H	Port 6 direction register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0$_B$
17_H	Port 7 direction register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0$_B$
18_H	Port 8 direction register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0$_B$
19_H	Port 9 direction register	DDR9	R/W	Port 9	0 0 0 0 0 0 0 0$_B$
$1A_H$	Port A direction register	DDRA	R/W	Port A	_ _ _ _ _ _ _0$_B$
$1B_H$	Analog Input Enable register	ADER	R/W	Port 6, A/D	1 1 1 1 1 1 1 1$_B$
$1C_H$	Port 0 Pullup control register	PUCR0	R/W	Port 0	0 0 0 0 0 0 0 0$_B$
$1D_H$	Port 1 Pullup control register	PUCR1	R/W	Port 1	0 0 0 0 0 0 0 0$_B$
$1E_H$	Port 2 Pullup control register	PUCR2	R/W	Port 2	0 0 0 0 0 0 0 0$_B$
$1F_H$	Port 3 Pullup control register	PUCR3	R/W	Port 3	0 0 0 0 0 0 0 0$_B$
20_H	Serial Mode Control Register 0	UMC0	R/W	UART0	0 0 0 0 0 1 0 0$_B$
21_H	Serial Status Register 0	USR0	R/W		0 0 0 1 0 0 0 0$_B$
22_H	Serial input data register 0/ Serial output data register 0	UIDR0/UODR0	R/W		XXXXXXXX$_B$
23_H	Rate and data register 0	URD0	R/W		0 0 0 0 0 0 0X$_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
24H	Serial mode register 1	SMR1	R/W	UART1	0 0 0 0 0 0 0 0B
25H	Serial control register 1	SCR1	R/W		0 0 0 0 0 1 0 0B
26H	Serial input data register 1/ Serial output data register 1	SIDR1/SODR1	R/W		XXXXXXXXB
27H	Serial status register 1	SSR1	R/W		0 0 0 0 1_0 0B
28H	UART1 prescaler control register	CDCR	R/W		0_ _ _1 1 1 1B
29H	Serial Edge select register	SES1	R/W		_ _ _ _ _ _ _0B
2AH	Prohibited				
2BH	Serial I/O prescaler	SCDCR	R/W	Extended I/O Serial Interface	0_ _ _1 1 1 1B
2CH	Serial mode control register	SMCS	R/W		_ _ _ _0 0 0 0B
2DH	Serial mode control register	SMCS	R/W		0 0 0 0 0 0 1 0B
2EH	Serial data register	SDR	R/W		XXXXXXXXB
2FH	Serial Edge select register	SES2	R/W		_ _ _ _ _ _ _0B
30H	External interrupt enable register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0B
31H	External interrupt request register	EIRR	R/W		XXXXXXXXB
32H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0B
33H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0B
34H	A/D control status register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0B
35H	A/D control status register 1	ADCS1	R/W		0 0 0 0 0 0 0 0B
36H	A/D data register 0	ADCR0	R		XXXXXXXXB
37H	A/D data register 1	ADCR1	R/W		0 0 0 0 1 _ XXB
38H	PPG0 operation mode control register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 0 _ _ 1B
39H	PPG1 operation mode control register	PPGC1	R/W		0 _ 0 0 0 0 0 1B
3AH	PPG0/1 clock selection register	PPG01	R/W		0 0 0 0 0 0 _ _B
3BH	Prohibited				
3CH	PPG2 operation mode control register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 0 _ _1B
3DH	PPG3 operation mode control register	PPGC3	R/W		0 _ 0 0 0 0 0 1B
3EH	PPG2/3 Clock Selection Register	PPG23	R/W		0 0 0 0 0 0 _ _B
3FH	Prohibited				
40H	PPG4 operation mode control register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 0 _ _ 1B
41H	PPG5 operation mode control register	PPGC5	R/W		0 _ 0 0 0 0 0 1B
42H	PPG4/5 clock selection register	PPG45	R/W		0 0 0 0 0 0 _ _B
43H	Prohibited				
44H	PPG6 operation mode control register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 0 _ _ 1B
45H	PPG7 operation mode control register	PPGC7	R/W		0 _ 0 0 0 0 0 1B
46H	PPG6/7 clock selection register	PPG67	R/W		0 0 0 0 0 0 _ _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
$A2_H$ to $A4_H$	Prohibited				
$A5_H$	Automatic ready function select register	ARSR	W	External Memory Access	0 0 1 1 _ _ 0 0_B
$A6_H$	External address output control register	HACR	W		0 0 0 0 0 0 0 0_B
$A7_H$	Bus control signal selection register	ECSR	W		0 0 0 0 0 0 0 $_B$
$A8_H$	Watchdog Timer control register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1_B
$A9_H$	Time Base Timer Control register	TBTC	R/W	Time Base Timer	1 - - 0 0 1 0 0_B
AA_H	Watch timer control register	WTC	R/W	Watch Timer	1 X 0 0 0 0 0 0_B
AB_H to AD_H	Prohibited				
AE_H	Flash memory control status register (Flash only, otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0_B
AF_H	Prohibited				
$B0_H$	Interrupt control register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1_B
$B1_H$	Interrupt control register 01	ICR01	R/W		0 0 0 0 0 1 1 1_B
$B2_H$	Interrupt control register 02	ICR02	R/W		0 0 0 0 0 1 1 1_B
$B3_H$	Interrupt control register 03	ICR03	R/W		0 0 0 0 0 1 1 1_B
$B4_H$	Interrupt control register 04	ICR04	R/W		0 0 0 0 0 1 1 1_B
$B5_H$	Interrupt control register 05	ICR05	R/W		0 0 0 0 0 1 1 1_B
$B6_H$	Interrupt control register 06	ICR06	R/W		0 0 0 0 0 1 1 1_B
$B7_H$	Interrupt control register 07	ICR07	R/W		0 0 0 0 0 1 1 1_B
$B8_H$	Interrupt control register 08	ICR08	R/W		0 0 0 0 0 1 1 1_B
$B9_H$	Interrupt control register 09	ICR09	R/W		0 0 0 0 0 1 1 1_B
BA_H	Interrupt control register 10	ICR10	R/W		0 0 0 0 0 1 1 1_B
BB_H	Interrupt control register 11	ICR11	R/W		0 0 0 0 0 1 1 1_B
BC_H	Interrupt control register 12	ICR12	R/W		0 0 0 0 0 1 1 1_B
BD_H	Interrupt control register 13	ICR13	R/W		0 0 0 0 0 1 1 1_B
BE_H	Interrupt control register 14	ICR14	R/W		0 0 0 0 0 1 1 1_B
BF_H	Interrupt control register 15	ICR15	R/W		0 0 0 0 0 1 1 1_B
$C0_H$ to FF_H	External				

Address	Register	Abbreviation	Access	Resource name	Initial value
$1FF0_H$	Program address detection register 0	PADR0	R/W	Address Match Detection Function	$XXXXXXXX_B$
$1FF1_H$	Program address detection register 0	PADR0	R/W		$XXXXXXXX_B$
$1FF2_H$	Program address detection register 0	PADR0	R/W		$XXXXXXXX_B$
$1FF3_H$	Program address detection register 1	PADR1	R/W		$XXXXXXXX_B$
$1FF4_H$	Program address detection register 1	PADR1	R/W		$XXXXXXXX_B$
$1FF5_H$	Program address detection register 1	PADR1	R/W		$XXXXXXXX_B$

(Continued)

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003B00H	003D00H	Control status register	CSR	R/W, R	00---000 0----0-1B
003B01H	003D01H				
003B02H	003D02H	Last event indicator register	LEIR	R/W	-------- 000-0000B
003B03H	003D03H				
003B04H	003D04H	Receive/transmit error counter register	RTEC	R	00000000 00000000B
003B05H	003D05H				
003B06H	003D06H	Bit timing register	BTR	R/W	-1111111 11111111B
003B07H	003D07H				
003B08H	003D08H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXXB
003B09H	003D09H				
003B0AH	003D0AH	Transmit RTR register	TRTRR	R/W	00000000 00000000B
003B0BH	003D0BH				
003B0CH	003D0CH	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXXB
003B0DH	003D0DH				
003B0EH	003D0EH	Transmit request enable register	TIER	R/W	00000000 00000000B
003B0FH	003D0FH				
003B10H	003D10H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXXB
003B11H	003D11H				
003B12H	003D12H				XXXXXXXX XXXXXXXXB
003B13H	003D13H				
003B14H	003D14H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXXB
003B15H	003D15H				
003B16H	003D16H				XXXXX--- XXXXXXXXB
003B17H	003D17H				
003B18H	003D18H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXXB
003B19H	003D19H				
003B1AH	003D1AH				XXXXX--- XXXXXXXXB
003B1BH	003D1BH				

List of Message Buffers (ID Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A00H to 003A1FH	003C00H to 003C1FH	General-purpose RAM	—	R/W	XXXXXXXXB to XXXXXXXXB
003A20H	003C20H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXXB
003A21H	003C21H				
003A22H	003C22H				XXXXX--- XXXXXXXXB
003A23H	003C23H				

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A24H	003C24H	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXXB
003A25H	003C25H				
003A26H	003C26H				XXXXX--- XXXXXXXXB
003A27H	003C27H				
003A28H	003C28H	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXXB
003A29H	003C29H				
003A2AH	003C2AH				XXXXX--- XXXXXXXXB
003A2BH	003C2BH				
003A2CH	003C2CH	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXXB
003A2DH	003C2DH				
003A2EH	003C2EH				XXXXX--- XXXXXXXXB
003A2FH	003C2FH				
003A30H	003C30H	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXXB
003A31H	003C31H				
003A32H	003C32H				XXXXX--- XXXXXXXXB
003A33H	003C33H				
003A34H	003C34H	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXXB
003A35H	003C35H				
003A36H	003C36H				XXXXX--- XXXXXXXXB
003A37H	003C37H				
003A38H	003C38H	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXXB
003A39H	003C39H				
003A3AH	003C3AH				XXXXX--- XXXXXXXXB
003A3BH	003C3BH				

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A88H to 003A8FH	003C88H to 003C8FH	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXXB to XXXXXXXXB
003A90H to 003A97H	003C90H to 003C97H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXXB to XXXXXXXXB
003A98H to 003A9FH	003C98H to 003C9FH	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXXB to XXXXXXXXB
003AA0H to 003AA7H	003CA0H to 003CA7H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXXB to XXXXXXXXB
003AA8H to 003AAFH	003CA8H to 003CAFH	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXXB to XXXXXXXXB
003AB0H to 003AB7H	003CB0H to 003CB7H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXXB to XXXXXXXXB
003AB8H to 003ABFH	003CB8H to 003CBFH	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXXB to XXXXXXXXB
003AC0H to 003AC7H	003CC0H to 003CC7H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXXB to XXXXXXXXB
003AC8H to 003ACFH	003CC8H to 003CCFH	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXXB to XXXXXXXXB
003AD0H to 003AD7H	003CD0H to 003CD7H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXXB to XXXXXXXXB
003AD8H to 003ADFH	003CD8H to 003CDFH	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXXB to XXXXXXXXB
003AE0H to 003AE7H	003CE0H to 003CE7H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXXB to XXXXXXXXB
003AE8H to 003AEFH	003CE8H to 003CEFH	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXXB to XXXXXXXXB
003AF0H to 003AF7H	003CF0H to 003CF7H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXXB to XXXXXXXXB
003AF8H to 003AFFH	003CF8H to 003CFFH	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXXB to XXXXXXXXB

10. Interrupt Map

Interrupt cause	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC$_H$	—	—
INT9 instruction	N/A	#09	FFFFD8$_H$	—	—
Exception	N/A	#10	FFFFD4$_H$	—	—
CAN 0 RX	N/A	#11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN 0 TX/NS	N/A	#12	FFFFCC$_H$		
CAN 1 RX	N/A	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 1 TX/NS	N/A	#14	FFFFC4$_H$		
External Interrupt INT0/INT1	*1	#15	FFFFC0$_H$	ICR02	0000B2$_H$
Time Base Timer	N/A	#16	FFFFBC$_H$		
16-bit Reload Timer 0	*1	#17	FFFFB8$_H$	ICR03	0000B3$_H$
8/10-bit A/D Converter	*1	#18	FFFFB4$_H$		
16-bit Free-run Timer	N/A	#19	FFFFB0$_H$	ICR04	0000B4$_H$
External Interrupt INT2/INT3	*1	#20	FFFFAC$_H$		
Serial I/O	*1	#21	FFFFA8$_H$	ICR05	0000B5$_H$
8/16-bit PPG 0/1	N/A	#22	FFFFA4$_H$		
Input Capture 0	*1	#23	FFFFA0$_H$	ICR06	0000B6$_H$
External Interrupt INT4/INT5	*1	#24	FFFF9C$_H$		
Input Capture 1	*1	#25	FFFF98$_H$	ICR07	0000B7$_H$
8/16-bit PPG 2/3	N/A	#26	FFFF94$_H$		
External Interrupt INT6/INT7	*1	#27	FFFF90$_H$	ICR08	0000B8$_H$
Watch Timer	N/A	#28	FFFF8C$_H$		
8/16-bit PPG 4/5	N/A	#29	FFFF88$_H$	ICR09	0000B9$_H$
Input Capture 2/3	*1	#30	FFFF84$_H$		
8/16-bit PPG 6/7	N/A	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 0	*1	#32	FFFF7C$_H$		
Output Compare 1	*1	#33	FFFF78$_H$	ICR11	0000BB$_H$
Input Capture 4/5	*1	#34	FFFF74$_H$		
Output Compare 2/3 - Input Capture 6/7	*1	#35	FFFF70$_H$	ICR12	0000BC$_H$
16-bit Reload Timer 1	*1	#36	FFFF6C$_H$		
UART 0 RX	*2	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 0 TX	*1	#38	FFFF64$_H$		
UART 1 RX	*2	#39	FFFF60$_H$	ICR14	0000BE$_H$
UART 1 TX	*1	#40	FFFF5C$_H$		
Flash Memory	N/A	#41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed interrupt	N/A	#42	FFFF54$_H$		

(Continued)

11.2 Recommended Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value			Units	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.5	5.0	5.5	V	Under normal operation : Other than MB90F548GL(S)/543G(S)/547G(S)/548G(S)
						Under normal operation when A/D conveter is used : MB90F548GL(S)/543G(S)/547G(S)/548G(S)
		3.5	5.0	5.5	V	Under normal operation when A/D conveter is not used : MB90F548GL(S)/543G(S)/547G(S)/548G(S)
		3.0	−	5.5	V	Maintain RAM data in stop mode
Smooth capacitor	C_S	0.022	0.1	1.0	µF	*
Operating temperature	T_A	−40	−	+105	°C	

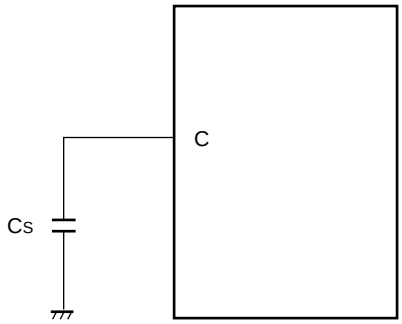
*: Use a ceramic capacitor or a capacitor of better 4. AC characteristics. The bypass capacitor should be greater than this capacitor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ **C Pin Connection Diagram**



(Continued)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Power supply current*	I_{CC}	V_{CC}	Internal frequency : 16 MHz, At normal operating	—	40	55	mA	
			Internal frequency : 16 MHz, At Flash programming/erasing	—	50	70	mA	Flash device
	I_{CCS}		Internal frequency : 16 MHz, At sleep mode	—	12	20	mA	
	I_{CTS}		V_{CC} = 5.0 V ± 10%, Internal frequency : 2 MHz, At pseudo timer mode	—	300	600	µA	
				—	600	1100	µA	MB90F548GL (S) only
				—	200	400	µA	MB90543G(S)/547G(S)/548(S) only
	I_{CCL}		Internal frequency : 8 kHz, At sub operation, T_A = 25 °C	—	400	750	µA	MB90F548GL only
				—	50	100	µA	MASK ROM
				—	150	300	µA	Flash device
	I_{CCLS}		Internal frequency : 8 kHz, At sub sleep, T_A = 25 °C	—	15	40	µA	
	I_{CCT}		Internal frequency : 8 kHz, At timer mode, T_A = 25 °C	—	7	25	µA	
	I_{CCH1}		At stop, T_A = 25 °C	—	5	20	µA	
	I_{CCH2}		At hardware standby mode, T_A = 25 °C	—	50	100	µA	
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVRH, AVRL, C, V_{CC}, V_{SS}	—	—	5	15	pF	

* : The power supply current testing conditions are when using the external clock.

11.4 AC Characteristics

11.4.1 Clock Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Oscillation frequency	f_C	X0, X1	3	—	16	MHz	No multiplier When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			8	—	16	MHz	PLL multiplied by 1 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			4	—	8	MHz	PLL multiplied by 2 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			3	—	5.33	MHz	PLL multiplied by 3 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			3	—	4	MHz	PLL multiplied by 4 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			3	—	5	MHz	When using an oscillator circuit V_{CC} < 4.5 V(MB90F548GL(S)/543G(S)/547G(S)/548G(S))
			3	—	16	MHz	No multiplier When using an external clock
			8	—	16	MHz	PLL multiplied by 1 When using an external clock
			4	—	8	MHz	PLL multiplied by 2 When using an external clock
			3	—	5.33	MHz	PLL multiplied by 3 When using an external clock
			3	—	4	MHz	PLL multiplied by 4 When using an external clock
	f_{CL}	X0A, X1A	—	32.768	—	kHz	

(Continued)

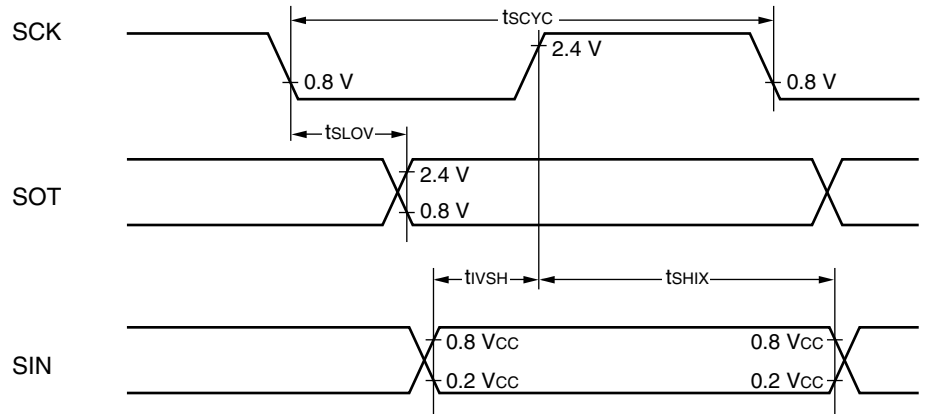
11.4.5 Bus Timing (Read)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

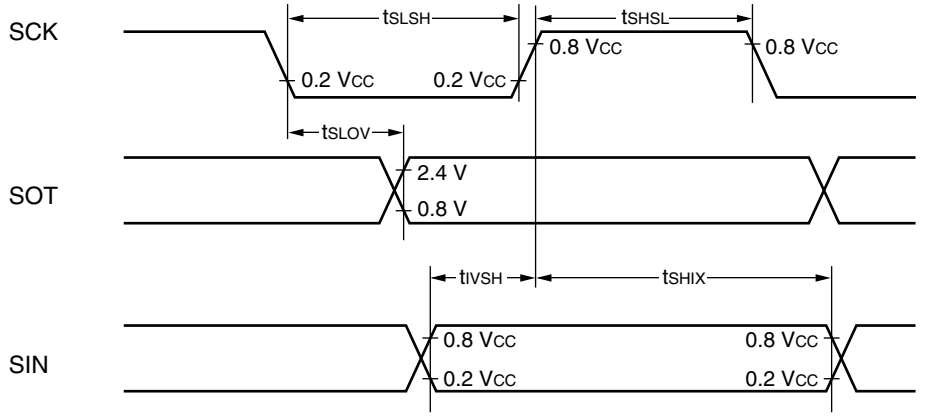
(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE		$t_{CP}/2 - 20$	−	ns	
Valid address → ALE↓ time	t_{AVLL}	ALE, A16 to A23, AD00 to AD15		$t_{CP}/2 - 20$	−	ns	
ALE↓ → Address valid time	t_{LLAX}	ALE, AD00 to AD15		$t_{CP}/2 - 15$	−	ns	
Valid address → $\overline{RD}$↓ time	t_{AVRL}	A16 toA23, AD00 to AD15, $\overline{RD}$		$t_{CP} - 15$	−	ns	
Valid address → Valid data input	t_{AVDV}	A16 to A23, AD00 to AD15		−	$5\ t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	RD	−	$3\ t_{CP}/2 - 20$	−	ns	
$\overline{RD}$↓ → Valid data input	t_{RLDV}	$\overline{RD}$, AD00 to AD15		−	$3\ t_{CP}/2 - 60$	ns	
$\overline{RD}$↑ → Data hold time	t_{RHDX}	$\overline{RD}$, AD00 to AD15		0	−	ns	
$\overline{RD}$↑ → ALE↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	−	ns	
$\overline{RD}$↑ → Address valid time	t_{RHAX}	$\overline{RD}$, A16 to A23		$t_{CP}/2 - 10$	−	ns	
Valid address → CLK↑ time	t_{AVCH}	A16 to A23, AD00 to AD15, CLK		$t_{CP}/2 - 20$	−	ns	
$\overline{RD}$↓ → CLK↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 20$	−	ns	
ALE↓ → $\overline{RD}$↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	−	ns	

■ Internal Shift Clock Mode

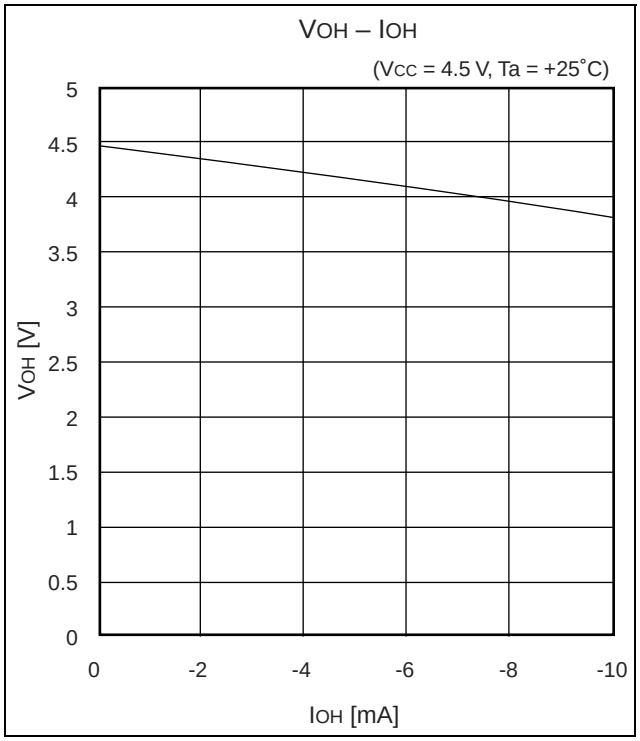


■ External Shift Clock Mode

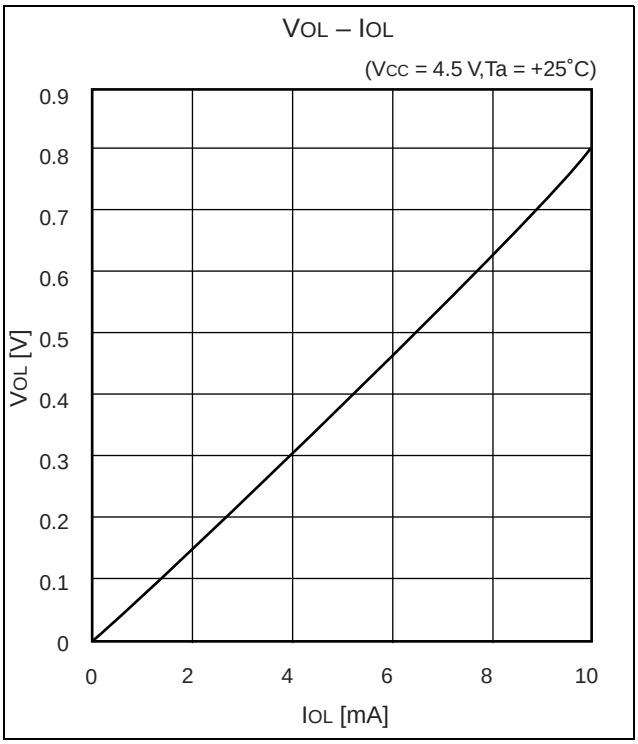


12. Example Characteristics

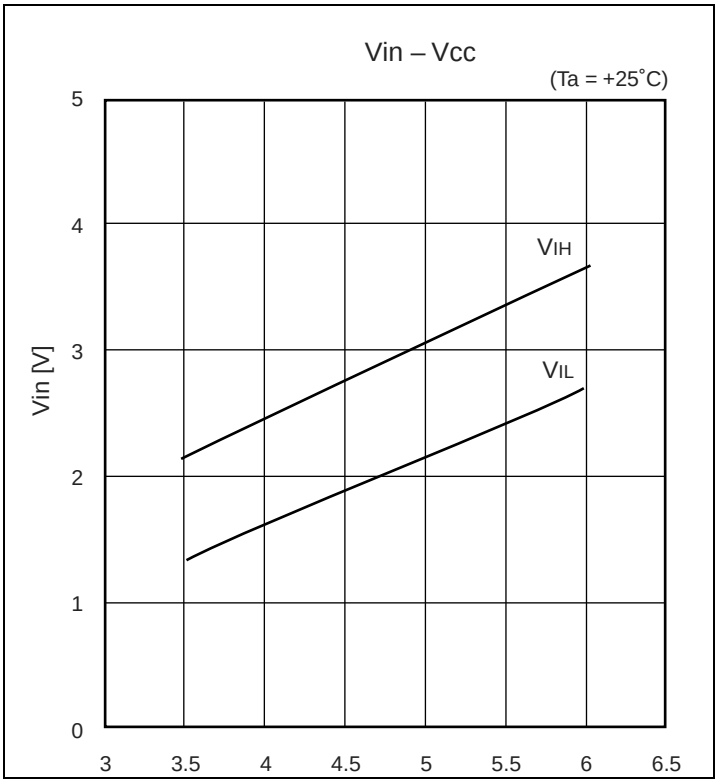
■ “H” level output voltage

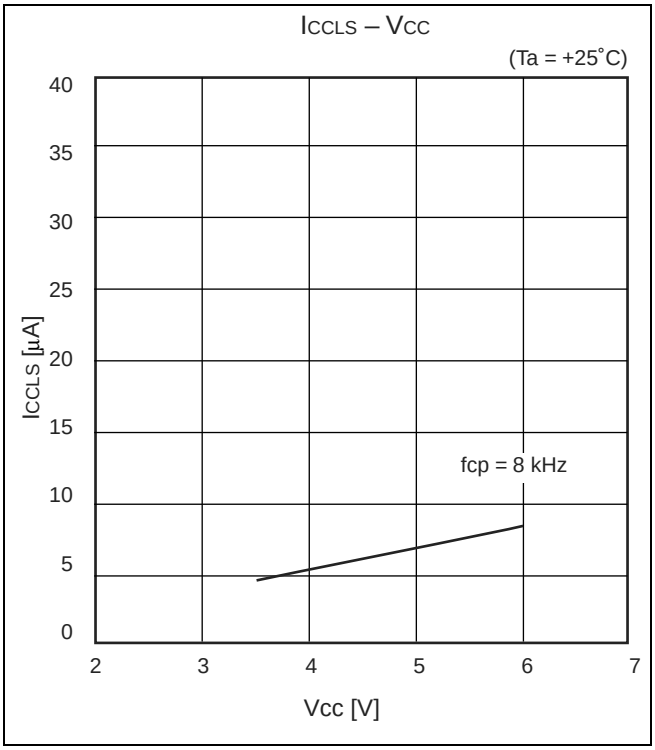


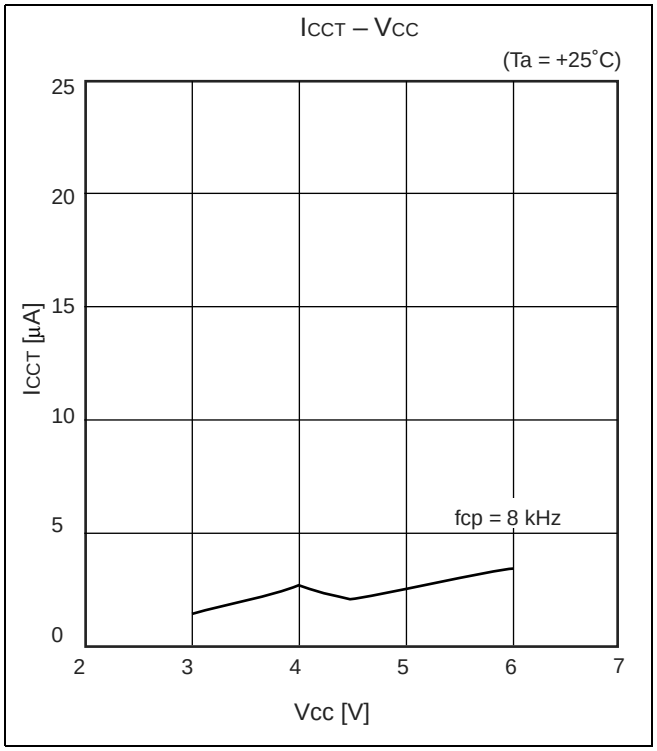
■ “L” level output voltage

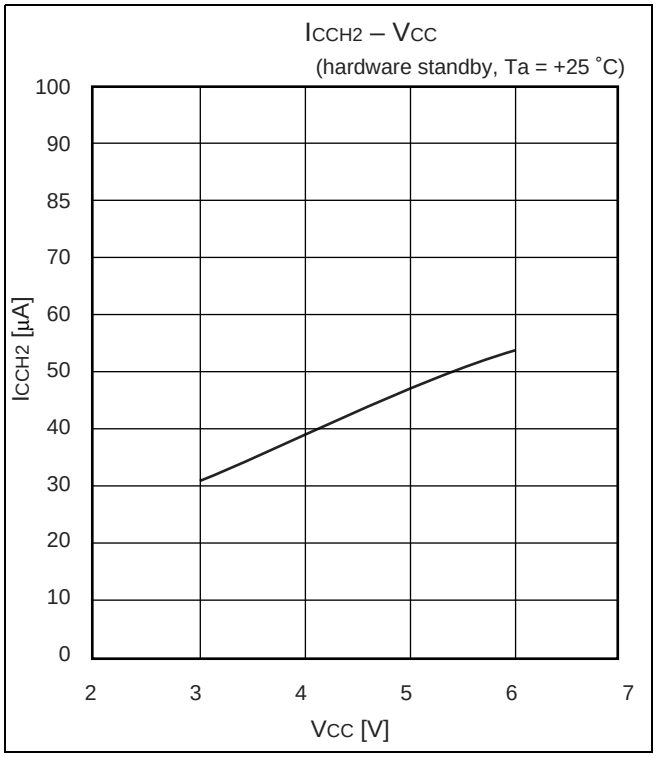


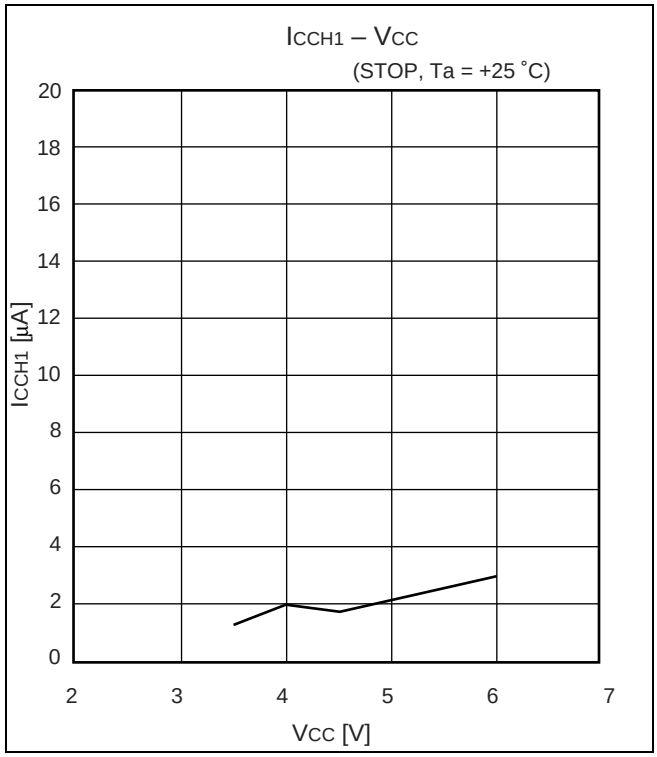
■ “H” level input voltage/ “L” level input voltage (Hysterisis inpiut)




ICCLS – VCC
(Ta = +25˚C)
ICCLS [µA]
40
35
30
25
20
15
10
5
0
fcp = 8 kHz
2
3
4
5
6
7
Vcc [V]


ICCT – VCC
(Ta = +25˚C)
ICCT [µA]
25
20
15
10
5
0
fcp = 8 kHz
2
3
4
5
6
7
Vcc [V]


ICCH2 – VCC
(hardware standby, Ta = +25 ˚C)
ICCH2 [µA]
100
90
85
70
60
50
40
30
20
10
0
2
3
4
5
6
7
VCC [V]


ICCH1 – VCC
(STOP, Ta = +25 ˚C)
ICCH1 [µA]
20
18
16
14
12
10
8
6
4
2
0
2
3
4
5
6
7
VCC [V]