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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

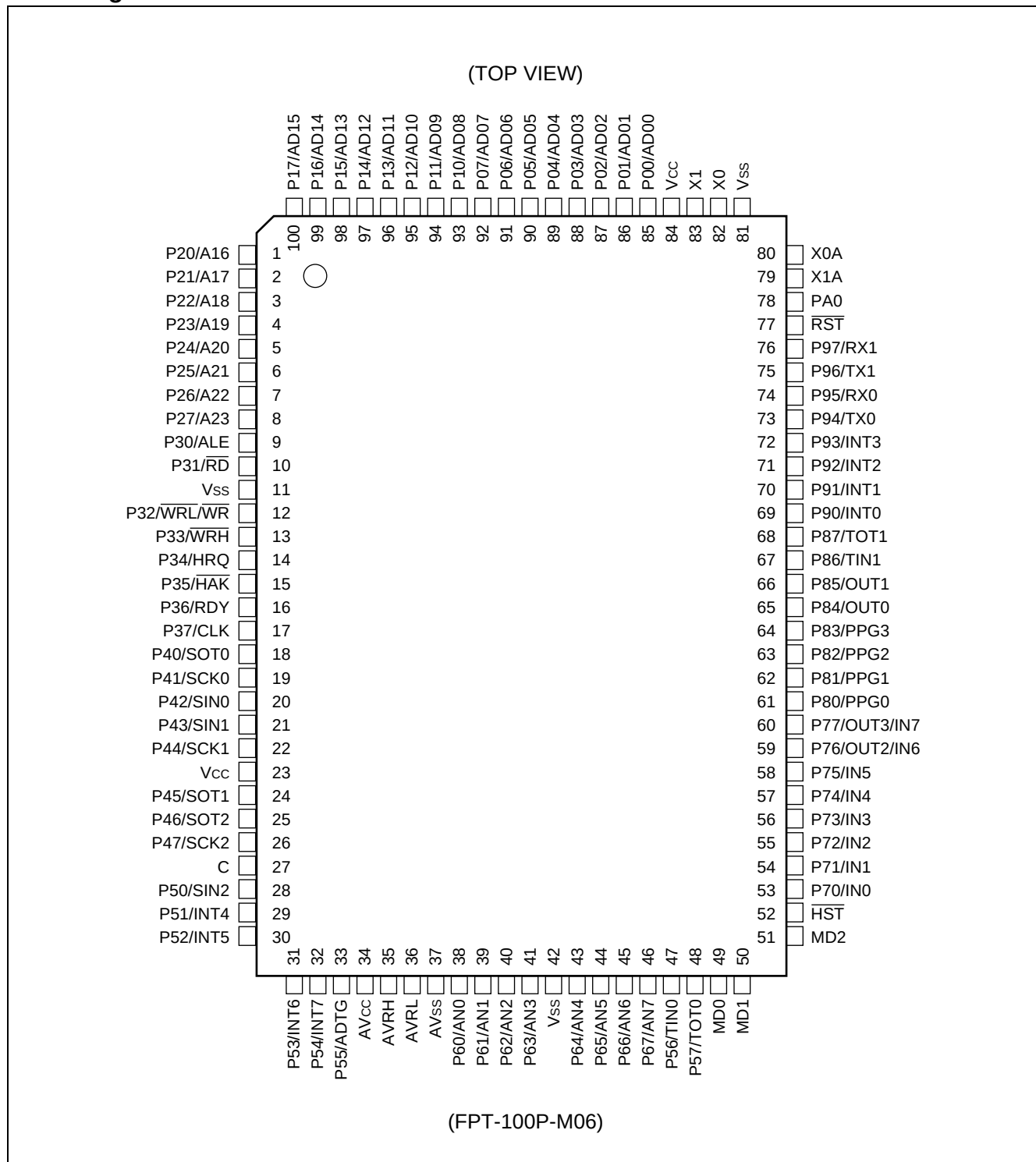
Product Status	Active
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspf-gs-9010

1. Product Lineup

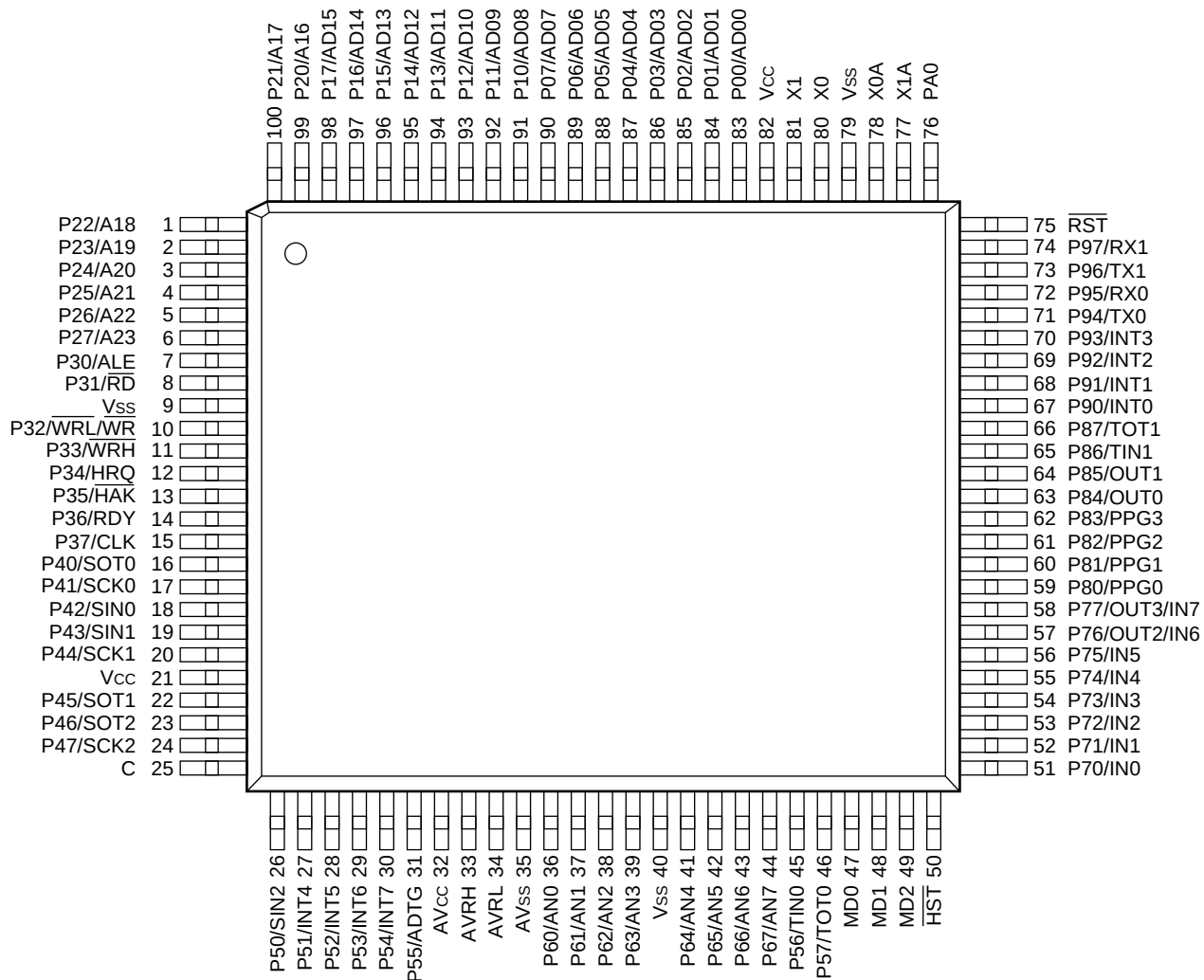
Features	MB90F543G (S) /F548G (S) MB90F549G (S) /F546G (S) MB90F548GL(S)	MB90543G (S) MB90547G (S) MB90548G (S) MB90549G (S)	MB90V540G
CPU	F ² MC-16LX CPU		
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, 1/2 when PLL stop) Minimum instruction execution time : 62.5 ns (machine clock 16MHz, 4MHz osc. four times multiplied by PLL)		
ROM	Flash memory MB90F543G(S)/F548G(S) / F548GL(S) : 128 Kbytes MB90F549G(S)/F546G(S) : 256 Kbytes	MASK ROM : MB90547G(S): 64 Kbytes MB90543G(S)/548G(S): 128 Kbytes MB90549G(S): 256 Kbytes	External
RAM	MB90F548G(S)/F548GL(S): 4 Kbytes MB90F543G (S) /F549G(S) : 6 Kbytes MB90F546G(S) : 8 Kbytes	MB90547G(S): 2 Kbytes MB90548G(S): 4 Kbytes MB90543G(S)/549G(S): 6 Kbytes	8 Kbytes
Clocks	MB90F543G/F548G/F549G/F546G/ F548GL : Two clocks system MB90F543GS/F548GS/F549GS/ F546GS/F548GLS : One clock system	MB90543G/547G/548G/549G : Two clocks system MB90543GS/547GS/548GS/ 549GS : One clock system	Two clocks system*1
Operating voltage range	*3		
Temperature range	−40 °C to 105 °C		
Package	QFP100, LQFP100		PGA-256
Emulator-specify power supply*2	—		None
UART0	Full duplex double buffer Support asynchronous/synchronous (with start/stop bit) transfer Baud rate : 4808/5208/9615/10417/19230/38460/62500/500000 bps (asynchronous) 500 K/1 M/2 Mbps (synchronous) at System clock = 16 MHz		
UART1 (SCI)	Full duplex double buffer Asynchronous (start-stop synchronized) and CLK-synchronous communication Baud rate : 1202/2404/4808/9615/19230/31250/38460/62500 bps (asynchronous) 62.5 K/125 K/250 K/500 K/1 M/2 Mbps (synchronous) at 6, 8, 10, 12, 16 MHz		
Serial I/O	Transfer can be started from MSB or LSB Supports internal clock synchronized transfer and external clock synchronized transfer Supports positive-edge and negative-edge clock synchronization Baud rate : 31.25 K/62.5 K/125 K/500 K/1 Mbps at System clock = 16 MHz		
A/D Converter	10-bit or 8-bit resolution 8 input channels Conversion time : 26.3 μs (per one channel)		

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2. Pin Assignment



(TOP VIEW)



(FPT-100P-M20)

Pin No.		Pin name	Circuit type	Function
LQFP ²	QFP ¹			
20	22	P44	G	General I/O port. This function is enabled when UART1 disables the clock output.
		SCK1		Serial clock pulse I/O pin for UART1. This function is enabled when UART1 enables the serial clock output.
22	24	P45	G	General I/O port. This function is enabled when UART1 disables the serial data output.
		SOT1		Serial data output pin for UART1. This function is enabled when UART1 enables the serial data output.
23	25	P46	G	General I/O port. This function is enabled when the Extended I/O serial interface disables the serial data output.
		SOT2		Serial data output pin for the Extended I/O serial interface. This function is enabled when the Extended I/O serial interface enables the serial data output.
24	26	P47	G	General I/O port. This function is enabled when the Extended I/O serial interface disables the clock output.
		SCK2		Serial clock pulse I/O pin for the Extended I/O serial interface. This function is enabled when the Extended I/O serial interface enables the Serial clock output.
26	28	P50	D	General I/O port. This function is always enabled.
		SIN2		Serial data input pin for the Extended I/O serial interface. Set the corresponding Port Direction Register to input if this function is used.
27 to 30	29 to 32	P51 to P54	D	General I/O port. This function is always enabled.
		INT4 to INT7		External interrupt request input pins for INT4 to INT7. Set the corresponding Port Direction Register to input if this function is used.
31	33	P55	D	General I/O port. This function is always enabled.
		ADTG		Trigger input pin for the A/D converter. Set the corresponding Port Direction Register to input if this function is used.
36 to 39	38 to 41	P60 to P63	E	General I/O port. This function is enabled when the analog input enable register specifies a port.
		AN0 to AN3		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.
41 to 44	43 to 46	P64 to P67	E	General I/O port. The function is enabled when the analog input enable register specifies a port.
		AN4 to AN7		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.
45	47	P56	D	General I/O port. This function is always enabled.
		TINO		Event input pin for the 16-bit reload timers 0. Set the corresponding Port Direction Register to input if this function is used.

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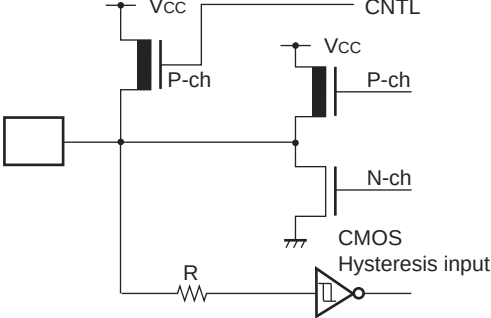
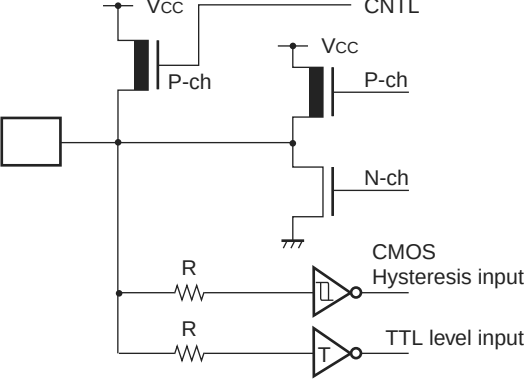
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Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
72	74	P95	D	General I/O port. This function is always enabled.
		RX0		RX input pin for CAN0 Interface. When the CAN function is used, output from the other functions must be stopped.
73	75	P96	D	General I/O port. This function is enabled when CAN1 disables the output.
		TX1		TX output pin for CAN1. This function is enabled when CAN1 enables the output (only MB90540G series) .
74	76	P97	D	General I/O port. This function is always enabled.
		RX1		RX input pin for CAN1 Interface. When the CAN function is used, output from the other functions must be stopped (only MB90540G series) .
76	78	PA0	D	General I/O port. This function is always enabled.
32	34	AV _{CC}	Power supply	Power supply pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AV _{CC} is applied to V _{CC} .
35	37	AV _{SS}	Power supply	Power supply pin for the A/D Converter.
33	35	AVRH	Power supply	External reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVR _H is applied to AV _{CC} .
34	36	AVRL	Power supply	External reference voltage input pin for the A/D Converter.
47, 48	49, 50	MD0, MD1	C	Input pins for specifying the operating mode. The pins must be directly connected to V _{CC} or V _{SS} .
49	51	MD2	F	Input pin for specifying the operating mode. The pin must be directly connected to V _{CC} or V _{SS} .
25	27	C	—	Power supply stabilization capacitor pin. It should be connected externally to an 0.1 μF ceramic capacitor.
21, 82	23, 84	V _{CC}	Power supply	Input pin for power supply (5.0 V) .
9, 40, 79	11, 42, 81	V _{SS}	Power supply	Input pin for power supply (0.0 V) .

*1 : FPT-100P-M06

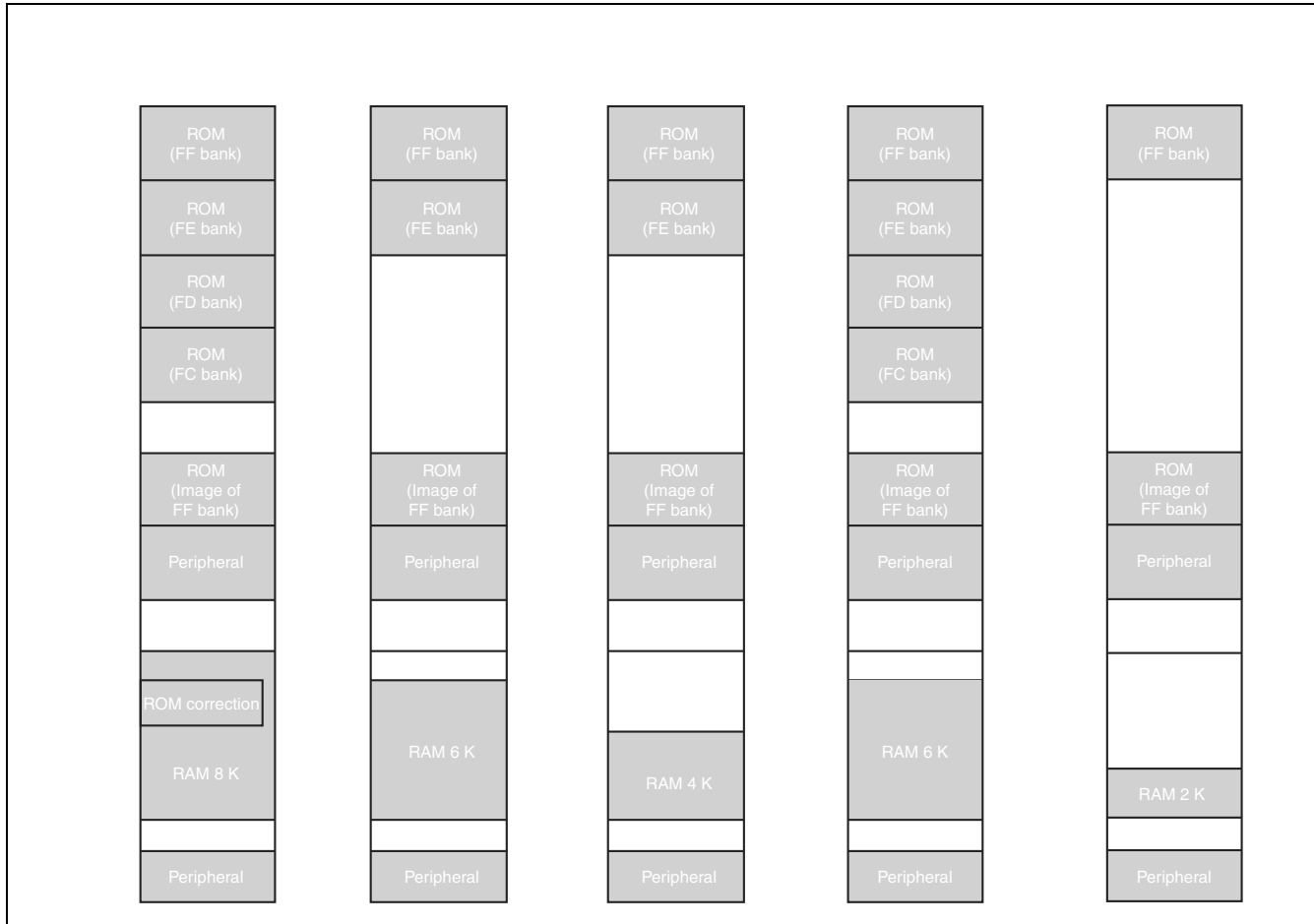
*2 : FPT-100P-M20

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Circuit type	Diagram	Remarks
H		■ CMOS level output ■ CMOS Hysteresis input ■ Programmable pull-up resistor : 50 kΩ approx.
I		■ CMOS level output ■ CMOS Hysteresis input ■ TTL level input (Flash devices in Flash writer mode only) ■ Programmable pullup resistor : 50 kΩ approx.

7. Memory Map

The memory space of the MB90540G/545G Series is shown below.



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits address are the same, the table in ROM can be referenced without using the “far” specification in the pointer declaration.

For example, an attempt to access 00C000_H accesses the value at FFC000_H in ROM. The ROM area in bank FF exceeds 48 Kbytes, and its entire image cannot be shown in bank 00. The image between FF4000_H and FFFFFFF_H is visible in bank 00, while the image between FF0000_H and FF3FFF_H is visible only in bank FF.

Address	Register	Abbreviation	Access	Resource name	Initial value
47 _H to 4B _H	Prohibited				
4C _H	Input capture control status register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0 _B
4D _H	Input capture control status register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0 _B
4E _H	Input capture control status register 4/5	ICS45	R/W	Input Capture 4/5	0 0 0 0 0 0 0 0 _B
4F _H	Input capture control status register 6/7	ICS67	R/W	Input Capture 6/7	0 0 0 0 0 0 0 0 _B
50 _H	Timer control status register 0	TMCSR0	R/W	16-bit Reload Timer 0	0 0 0 0 0 0 0 0 _B
51 _H	Timer control status register 0	TMCSR0	R/W		____ 0 0 0 0 _B
52 _H	Timer register 0/reload register 0	TMR0/TMRLR0	R/W		XXXXXXXX _B
53 _H	Timer register 0/reload register 0	TMR0/TMRLR0	R/W		XXXXXXXX _B
54 _H	Timer control status register 1	TMCSR1	R/W	16-bit Reload Timer 1	0 0 0 0 0 0 0 0 _B
55 _H	Timer control status register 1	TMCSR1	R/W		____ 0 0 0 0 _B
56 _H	Timer register 1/reload register 1	TMR1/TMRLR1	R/W		XXXXXXXX _B
57 _H	Timer register 1/reload register 1	TMR1/TMRLR1	R/W		XXXXXXXX _B
58 _H	Output compare control status register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 __ 0 0 _B
59 _H	Output compare control status register 1	OCS1	R/W		__ __ 0 0 0 0 0 _B
5A _H	Output compare control status register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 __ 0 0 _B
5B _H	Output compare control status register 3	OCS3	R/W		__ __ 0 0 0 0 0 _B
5C _H to 6B _H	Prohibited				
6C _H	Timer Data register	TCDT	R/W	I/O Timer	0 0 0 0 0 0 0 0 _B
6D _H	Timer Data register	TCDT	R/W		0 0 0 0 0 0 0 0 _B
6E _H	Timer Control register	TCCS	R/W		0 0 0 0 0 0 0 0 _B
6F _H	ROM mirror function selection register	ROMM	R/W	ROM Mirror	_____ 1 _B
70 _H to 7F _H	Reserved for CAN 0 Interface.				
80 _H to 8F _H	Reserved for CAN 1 Interface.				
90 _H to 9D _H	Prohibited				
9E _H	Program address detection control status register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0 _B
9F _H	Delayed interrupt/release register	DIRR	R/W	Delayed Interrupt	_____ 0 _B
A0 _H	Low-power mode control register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0 _B
A1 _H	Clock selection register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0 _B

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003B00 _H	003D00 _H	Control status register	CSR	R/W, R	00---000 0---0-1 _B
003B01 _H	003D01 _H				
003B02 _H	003D02 _H	Last event indicator register	LEIR	R/W	----- 000-0000 _B
003B03 _H	003D03 _H				
003B04 _H	003D04 _H	Receive/transmit error counter register	RTEC	R	00000000 00000000 _B
003B05 _H	003D05 _H				
003B06 _H	003D06 _H	Bit timing register	BTR	R/W	-1111111 11111111 _B
003B07 _H	003D07 _H				
003B08 _H	003D08 _H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXX _B
003B09 _H	003D09 _H				
003B0A _H	003D0A _H	Transmit RTR register	TRTRR	R/W	00000000 00000000 _B
003B0B _H	003D0B _H				
003B0C _H	003D0C _H	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXX _B
003B0D _H	003D0D _H				
003B0E _H	003D0E _H	Transmit request enable register	TIER	R/W	00000000 00000000 _B
003B0F _H	003D0F _H				
003B10 _H	003D10 _H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXX _B
003B11 _H	003D11 _H				XXXXXXXX XXXXXXXX _B
003B12 _H	003D12 _H				
003B13 _H	003D13 _H				
003B14 _H	003D14 _H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXX _B
003B15 _H	003D15 _H				XXXXXX--- XXXXXXXX _B
003B16 _H	003D16 _H				
003B17 _H	003D17 _H				
003B18 _H	003D18 _H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXX _B
003B19 _H	003D19 _H				XXXXXX--- XXXXXXXX _B
003B1A _H	003D1A _H				
003B1B _H	003D1B _H				

List of Message Buffers (ID Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A00 _H to 003A1F _H	003C00 _H to 003C1F _H	General-purpose RAM	—	R/W	XXXXXXXX _B to XXXXXXXX _B
003A20 _H	003C20 _H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXX _B
003A21 _H	003C21 _H				XXXXXX--- XXXXXXXX _B
003A22 _H	003C22 _H				
003A23 _H	003C23 _H				

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A24 _H	003C24 _H	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXX _B
003A25 _H	003C25 _H				XXXXXX--- XXXXXXXX _B
003A26 _H	003C26 _H				
003A27 _H	003C27 _H				
003A28 _H	003C28 _H	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXX _B
003A29 _H	003C29 _H				XXXXXX--- XXXXXXXX _B
003A2A _H	003C2A _H				
003A2B _H	003C2B _H				
003A2C _H	003C2C _H	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX _B
003A2D _H	003C2D _H				XXXXXX--- XXXXXXXX _B
003A2E _H	003C2E _H				
003A2F _H	003C2F _H				
003A30 _H	003C30 _H	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX _B
003A31 _H	003C31 _H				XXXXXX--- XXXXXXXX _B
003A32 _H	003C32 _H				
003A33 _H	003C33 _H				
003A34 _H	003C34 _H	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX _B
003A35 _H	003C35 _H				XXXXXX--- XXXXXXXX _B
003A36 _H	003C36 _H				
003A37 _H	003C37 _H				
003A38 _H	003C38 _H	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX _B
003A39 _H	003C39 _H				XXXXXX--- XXXXXXXX _B
003A3A _H	003C3A _H				
003A3B _H	003C3B _H				

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A3C _H	003C3C _H	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX _B
003A3D _H	003C3D _H				
003A3E _H	003C3E _H				XXXXX--- XXXXXXXX _B
003A3F _H	003C3F _H				
003A40 _H	003C40 _H	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX _B
003A41 _H	003C41 _H				
003A42 _H	003C42 _H				XXXXX--- XXXXXXXX _B
003A43 _H	003C43 _H				
003A44 _H	003C44 _H	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX _B
003A45 _H	003C45 _H				
003A46 _H	003C46 _H				XXXXX--- XXXXXXXX _B
003A47 _H	003C47 _H				
003A48 _H	003C48 _H	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX _B
003A49 _H	003C49 _H				
003A4A _H	003C4A _H				XXXXX--- XXXXXXXX _B
003A4B _H	003C4B _H				
003A4C _H	003C4C _H	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX _B
003A4D _H	003C4D _H				
003A4E _H	003C4E _H				XXXXX--- XXXXXXXX _B
003A4F _H	003C4F _H				
003A50 _H	003C50 _H	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX _B
003A51 _H	003C51 _H				
003A52 _H	003C52 _H				XXXXX--- XXXXXXXX _B
003A53 _H	003C53 _H				
003A54 _H	003C54 _H	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX _B
003A55 _H	003C55 _H				
003A56 _H	003C56 _H				XXXXX--- XXXXXXXX _B
003A57 _H	003C57 _H				
003A58 _H	003C58 _H	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX _B
003A59 _H	003C59 _H				
003A5A _H	003C5A _H				XXXXX--- XXXXXXXX _B
003A5B _H	003C5B _H				
003A5C _H	003C5C _H	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX _B
003A5D _H	003C5D _H				
003A5E _H	003C5E _H				XXXXX--- XXXXXXXX _B
003A5F _H	003C5F _H				

List of Message Buffers (DLC Registers and Data Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A60 _H	003C60 _H	DLC register 0	DLCR0	R/W	----XXXX _B
003A61 _H	003C61 _H				
003A62 _H	003C62 _H	DLC register 1	DLCR1	R/W	----XXXX _B
003A63 _H	003C63 _H				
003A64 _H	003C64 _H	DLC register 2	DLCR2	R/W	----XXXX _B
003A65 _H	003C65 _H				
003A66 _H	003C66 _H	DLC register 3	DLCR3	R/W	----XXXX _B
003A67 _H	003C67 _H				
003A68 _H	003C68 _H	DLC register 4	DLCR4	R/W	----XXXX _B
003A69 _H	003C69 _H				
003A6A _H	003C6A _H	DLC register 5	DLCR5	R/W	----XXXX _B
003A6B _H	003C6B _H				
003A6C _H	003C6C _H	DLC register 6	DLCR6	R/W	----XXXX _B
003A6D _H	003C6D _H				
003A6E _H	003C6E _H	DLC register 7	DLCR7	R/W	----XXXX _B
003A6F _H	003C6F _H				
003A70 _H	003C70 _H	DLC register 8	DLCR8	R/W	----XXXX
003A71 _H	003C71 _H				
003A72 _H	003C72 _H	DLC register 9	DLCR9	R/W	----XXXX _B
003A73 _H	003C73 _H				
003A74 _H	003C74 _H	DLC register 10	DLCR10	R/W	----XXXX _B
003A75 _H	003C75 _H				
003A76 _H	003C76 _H	DLC register 11	DLCR11	R/W	----XXXX _B
003A77 _H	003C77 _H				
003A78 _H	003C78 _H	DLC register 12	DLCR12	R/W	----XXXX _B
003A79 _H	003C79 _H				
003A7A _H	003C7A _H	DLC register 13	DLCR13	R/W	----XXXX _B
003A7B _H	003C7B _H				
003A7C _H	003C7C _H	DLC register 14	DLCR14	R/W	----XXXX _B
003A7D _H	003C7D _H				
003A7E _H	003C7E _H	DLC register 15	DLCR15	R/W	----XXXX _B
003A7F _H	003C7F _H				
003A80 _H to 003A87 _H	003C80 _H to 003C87 _H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B

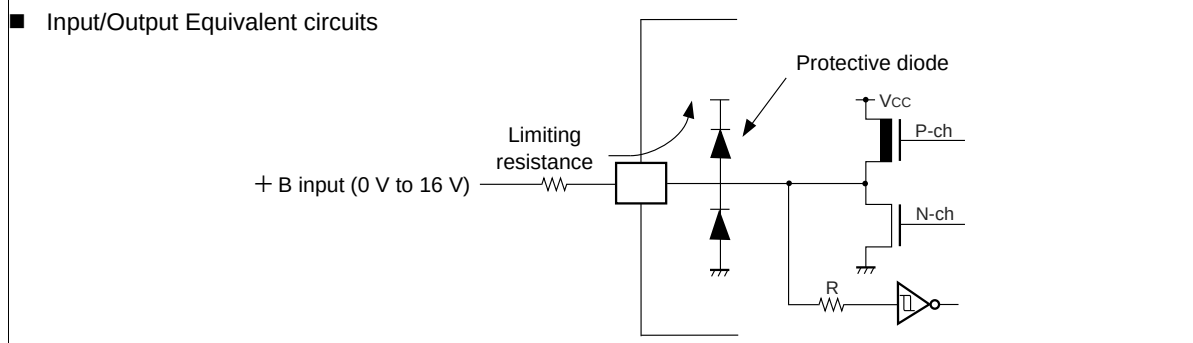
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10. Interrupt Map

Interrupt cause	EI ² OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC _H	—	—
INT9 instruction	N/A	#09	FFFFD8 _H	—	—
Exception	N/A	#10	FFFFD4 _H	—	—
CAN 0 RX	N/A	#11	FFFFD0 _H	ICR00	0000B0 _H
CAN 0 TX/NS	N/A	#12	FFFFCC _H		
CAN 1 RX	N/A	#13	FFFFC8 _H	ICR01	0000B1 _H
CAN 1 TX/NS	N/A	#14	FFFFC4 _H		
External Interrupt INT0/INT1	*1	#15	FFFFC0 _H	ICR02	0000B2 _H
Time Base Timer	N/A	#16	FFFFBC _H		
16-bit Reload Timer 0	*1	#17	FFFFB8 _H	ICR03	0000B3 _H
8/10-bit A/D Converter	*1	#18	FFFFB4 _H		
16-bit Free-run Timer	N/A	#19	FFFFB0 _H	ICR04	0000B4 _H
External Interrupt INT2/INT3	*1	#20	FFFFAC _H		
Serial I/O	*1	#21	FFFFA8 _H	ICR05	0000B5 _H
8/16-bit PPG 0/1	N/A	#22	FFFFA4 _H		
Input Capture 0	*1	#23	FFFFA0 _H	ICR06	0000B6 _H
External Interrupt INT4/INT5	*1	#24	FFFF9C _H		
Input Capture 1	*1	#25	FFFF98 _H	ICR07	0000B7 _H
8/16-bit PPG 2/3	N/A	#26	FFFF94 _H		
External Interrupt INT6/INT7	*1	#27	FFFF90 _H	ICR08	0000B8 _H
Watch Timer	N/A	#28	FFFF8C _H		
8/16-bit PPG 4/5	N/A	#29	FFFF88 _H	ICR09	0000B9 _H
Input Capture 2/3	*1	#30	FFFF84 _H		
8/16-bit PPG 6/7	N/A	#31	FFFF80 _H	ICR10	0000BA _H
Output Compare 0	*1	#32	FFFF7C _H		
Output Compare 1	*1	#33	FFFF78 _H	ICR11	0000BB _H
Input Capture 4/5	*1	#34	FFFF74 _H		
Output Compare 2/3 - Input Capture 6/7	*1	#35	FFFF70 _H	ICR12	0000BC _H
16-bit Reload Timer 1	*1	#36	FFFF6C _H		
UART 0 RX	*2	#37	FFFF68 _H	ICR13	0000BD _H
UART 0 TX	*1	#38	FFFF64 _H		
UART 1 RX	*2	#39	FFFF60 _H	ICR14	0000BE _H
UART 1 TX	*1	#40	FFFF5C _H		
Flash Memory	N/A	#41	FFFF58 _H	ICR15	0000BF _H
Delayed interrupt	N/A	#42	FFFF54 _H		

(Continued)

- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept + B signal input.
- Sample recommended circuits :



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

(Continued)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

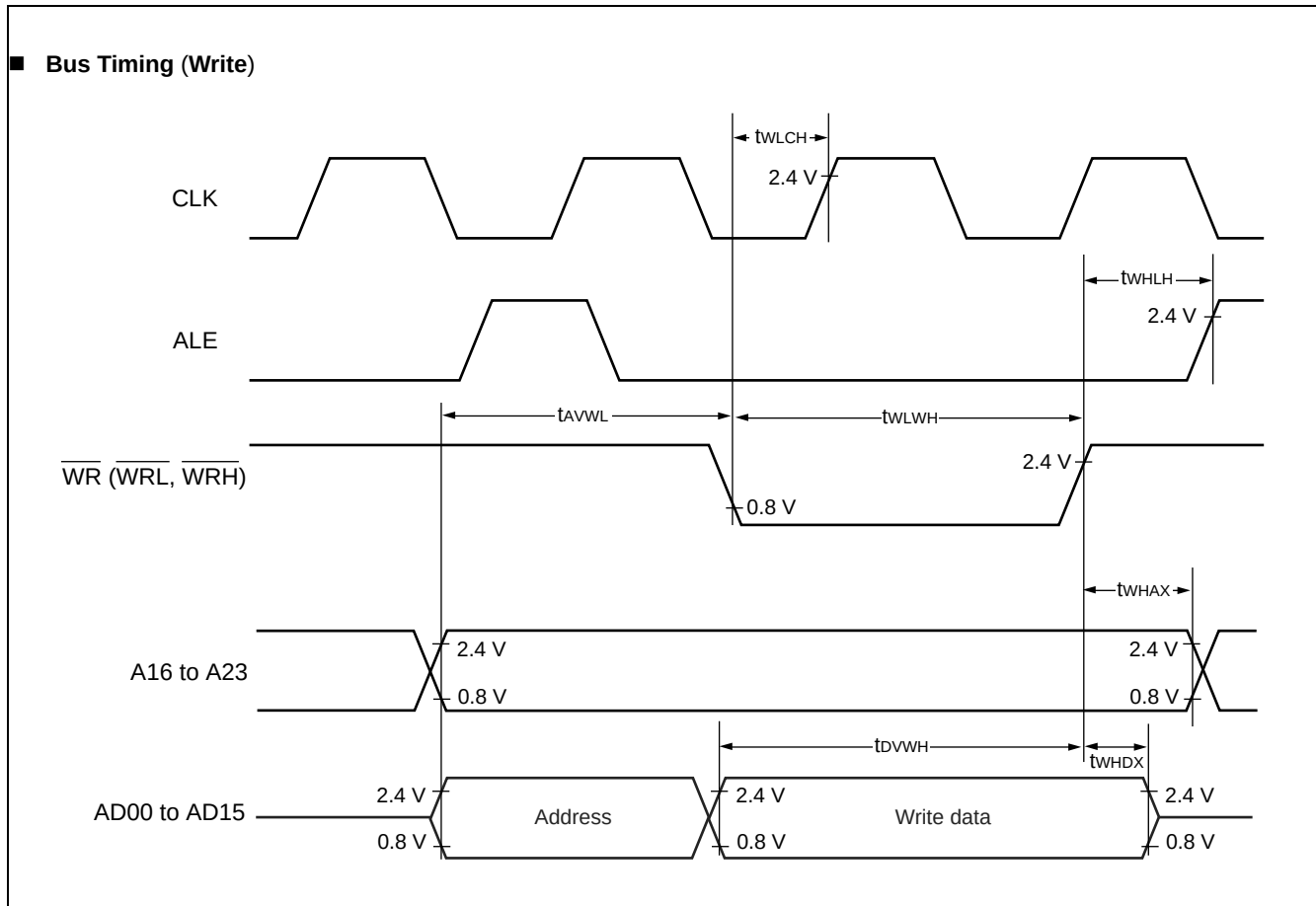
Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	No multiplier When using an oscillator circuit $V_{CC} = 5.0 \text{ V} \pm 10\%$
			62.5	—	125	ns	PLL multiplied by 1 When using an oscillator circuit $V_{CC} = 5.0 \text{ V} \pm 10\%$
			125	—	250	ns	PLL multiplied by 2 When using an oscillator circuit $V_{CC} = 5.0 \text{ V} \pm 10\%$
			187.5	—	333	ns	PLL multiplied by 3 When using an oscillator circuit $V_{CC} = 5.0 \text{ V} \pm 10\%$
			250	—	333	ns	PLL multiplied by 4 When using an oscillator circuit $V_{CC} = 5.0 \text{ V} \pm 10\%$
			200	—	333	ns	When using an oscillator circuit $V_{CC} < 4.5 \text{ V}$ (MB90F548GL(S)/543G(S)/ 547G(S)/548G(S))
			62.5	—	333	ns	No multiplier When using an external clock
			62.5	—	125	ns	PLL multiplied by 1 When using an external clock
			125	—	250	ns	PLL multiplied by 2 When using an external clock
			187.5	—	333	ns	PLL multiplied by 3 When using an external clock
			250	—	333	ns	PLL multiplied by 4 When using an external clock
	t_{LCYL}	X0A, X1A	—	30.5	—	μs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WLH}, P_{WLL}	X0A	—	15.2	—	μs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using an external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	When using main clock
	f_{LCP}	—	—	8.192	—	kHz	When using sub-clock
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	When using main clock
	t_{LCP}	—	—	122.1	—	μs	When using sub-clock

11.4.6 Bus Timing (Write)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Valid address $\rightarrow \overline{WR}\downarrow$ time	t_{AVWL}	A16 to A23 AD00 to AD15, $\overline{WR}$	—	$t_{CP} - 15$	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	WR		$3 t_{CP}/2 - 20$	—	ns	
Valid data output $\rightarrow \overline{WR}\uparrow$ time	t_{DVWH}	AD00 to AD15, $\overline{WR}$		$3 t_{CP}/2 - 20$	—	ns	
$\overline{WR}\uparrow \rightarrow$ Data hold time	t_{WHDX}	AD00 to AD15, $\overline{WR}$		20	—	ns	
$\overline{WR}\uparrow \rightarrow$ Address valid time	t_{WHAX}	A16 to A23, $\overline{WR}$		$t_{CP}/2 - 10$	—	ns	
$\overline{WR}\uparrow \rightarrow$ ALE $\uparrow$ time	t_{WHLH}	WR, ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{WR}\uparrow \rightarrow$ CLK $\uparrow$ time	t_{WLCH}	WR, CLK		$t_{CP}/2 - 20$	—	ns	



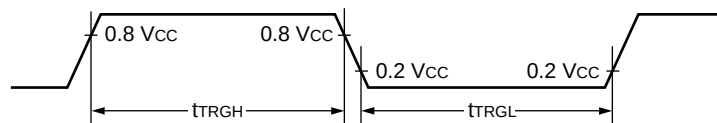
11.4.12 Trigger Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Input pulse width	t_{TRGH}	INT0 to INT7, ADTG	—	5 t_{CP}	—	ns	Under normal operation
	t_{TRGL}			1	—	μs	In stop mode

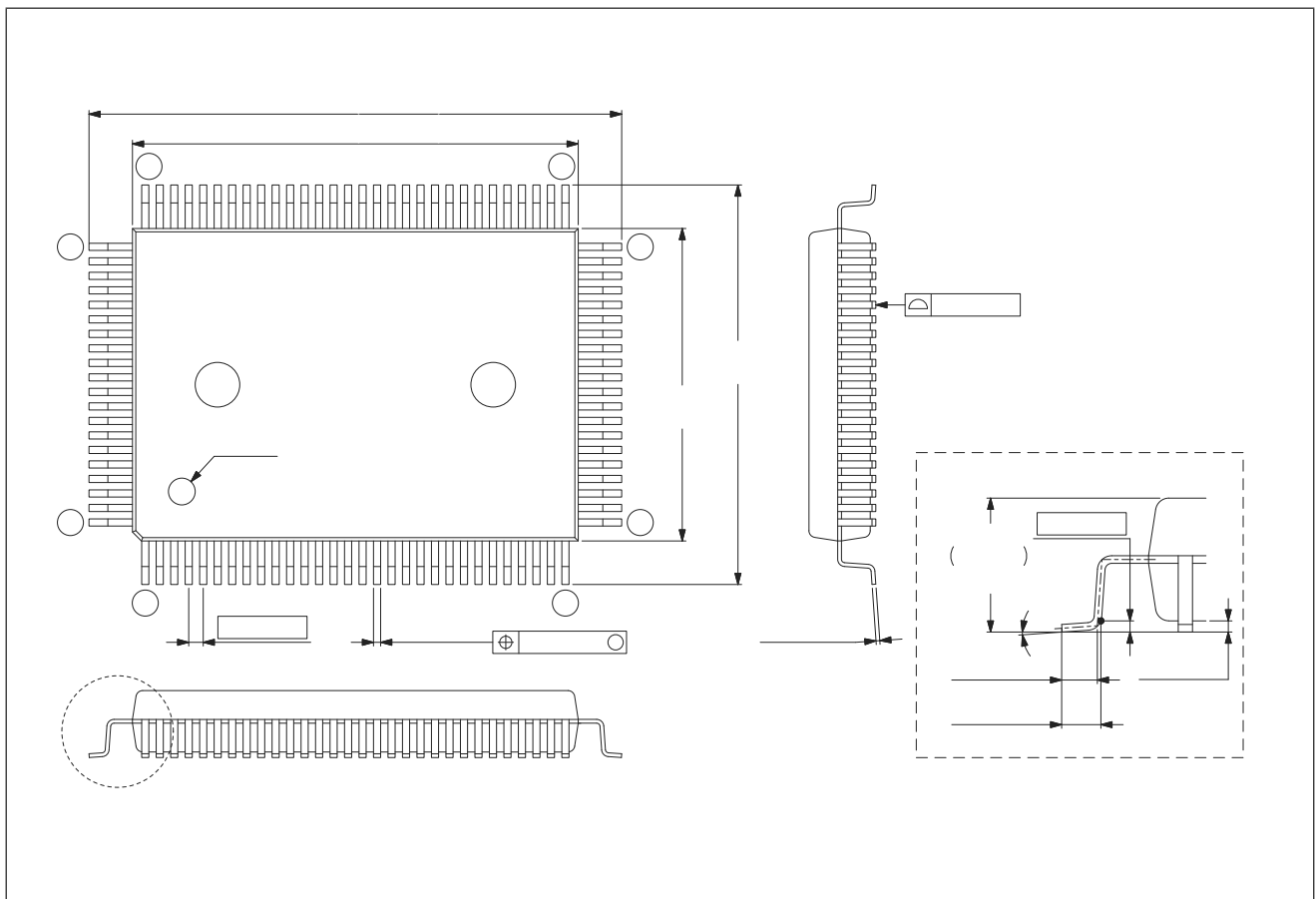
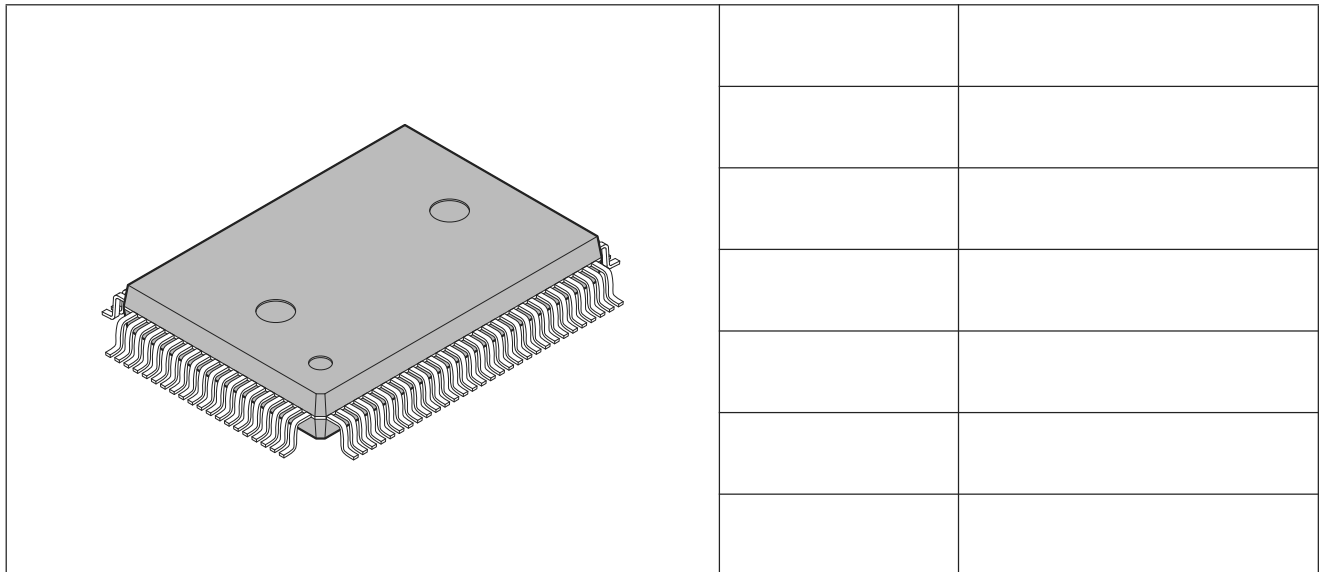
■ Trigger Input Timing



13. Ordering Information

Part number	Package	Remarks
MB90F543GPF MB90F543GSPF MB90F546GPF MB90F546GSPF MB90F548GPF MB90F548GSPF MB90F548GLPF MB90F548GLSPF MB90F549GPF MB90F549GSPF MB90543GPF MB90543GSPF MB90547GPF MB90547GSPF MB90548GPF MB90548GSPF MB90549GPF MB90549GSPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90F543GPMC MB90F543GSPMC MB90F546GPMC MB90F546GSPMC MB90F548GPMC MB90F548GSPMC MB90F548GLPMC MB90F548GLSPMC MB90F549GPMC MB90F549GSPMC MB90543GPMC MB90543GSPMC MB90547GPMC MB90547GSPMC MB90548GPMC MB90548GSPMC MB90549GPMC MB90549GSPMC	100-pin Plastic LQFP (FPT-100P-M20)	

14. Package Dimensions



(Continued)

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