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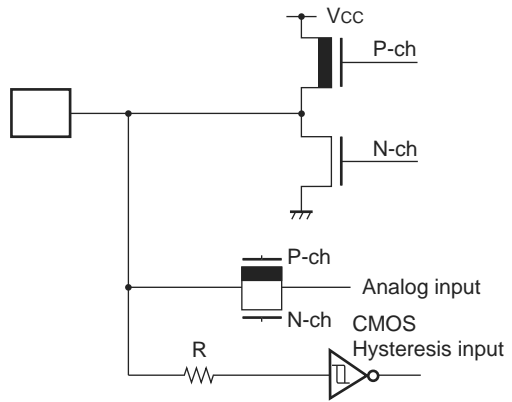
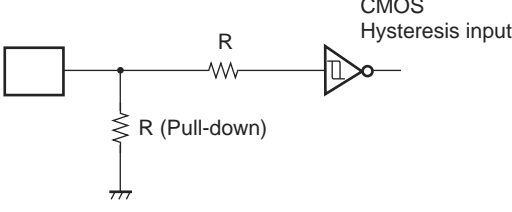
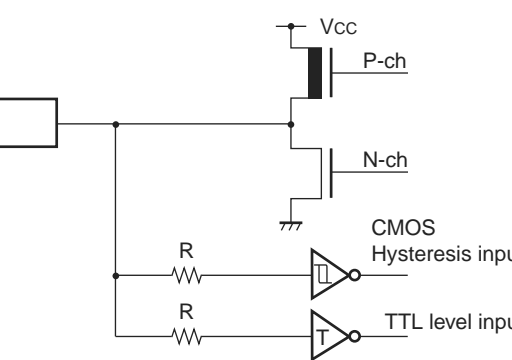
What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

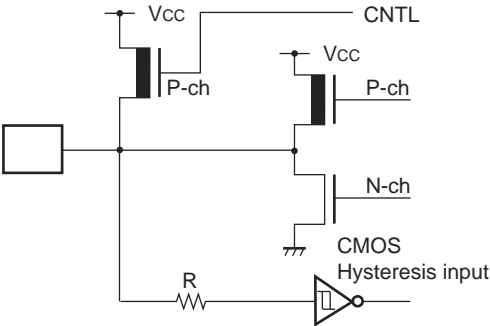
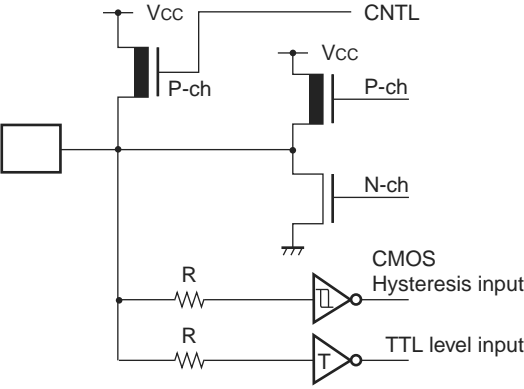
Details

Product Status	Active
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspf-gs-9017

Circuit type	Diagram	Remarks
E		<ul style="list-style-type: none"> ■ CMOS level output ■ CMOS Hysteresis input ■ Analog input
F		<ul style="list-style-type: none"> ■ CMOS Hysteresis input ■ Pull-down Resistor : 50 kΩ approx. (except Flash devices)
G		<ul style="list-style-type: none"> ■ CMOS level output ■ CMOS Hysteresis input ■ TTL level input (Flash devices in Flash writer mode only)

(Continued)

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Circuit type	Diagram	Remarks
H		<ul style="list-style-type: none"> ■ CMOS level output ■ CMOS Hysteresis input ■ Programmable pull-up resistor : 50 kΩ approx.
I		<ul style="list-style-type: none"> ■ CMOS level output ■ CMOS Hysteresis input ■ TTL level input (Flash devices in Flash writer mode only) ■ Programmable pullup resistor : 50 kΩ approx.

5. Handling Devices

(1) Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} .
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, care must also be taken in not allowing the analog power-supply voltage (AV_{CC} , $AVRH$) to exceed the digital power-supply voltage.

(2) Handling unused pins

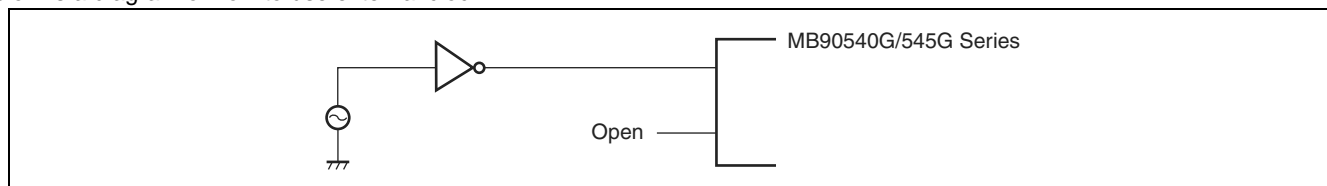
Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 k Ω .

Unused bi-directional pins should be set to the output state and can be left open, or the input state with the above described connection.

(3) Using external clock

To use external clock, drive X0 pin only and leave X1 pin unconnected.

Below is a diagram of how to use external clock.



(4) Use of the sub-clock

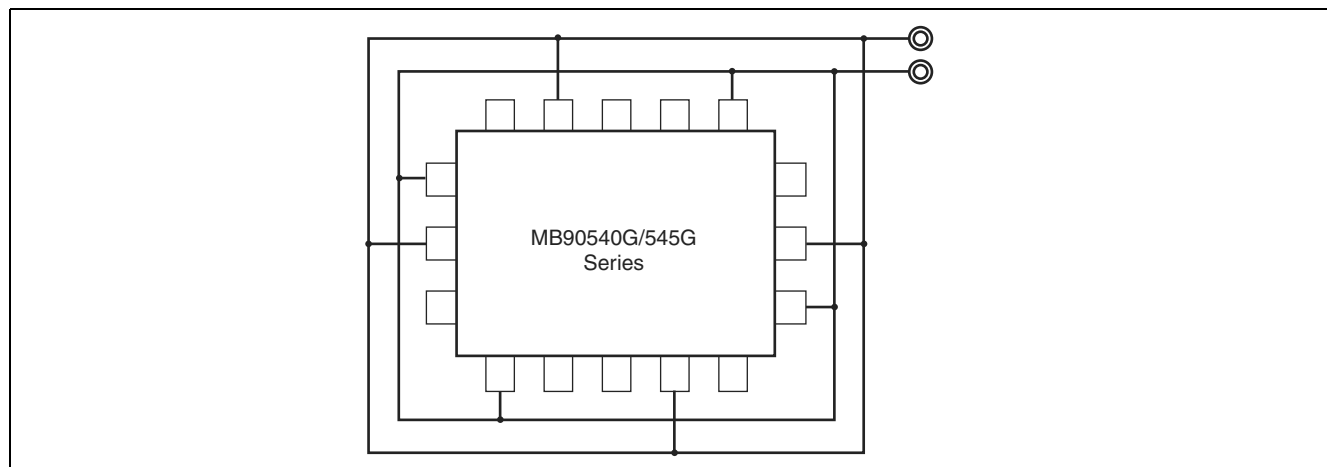
Use one clock system parts when the sub-clock is not used. In that case, pull-down the pin X0A and leave the pin X1A open. When using two clock system parts, a 32 kHz oscillator has to be connected to the X0A and X1A pins.

(5) Power supply pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect V_{CC} and V_{SS} pins via the lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 μF between V_{CC} and V_{SS} pins near the device.

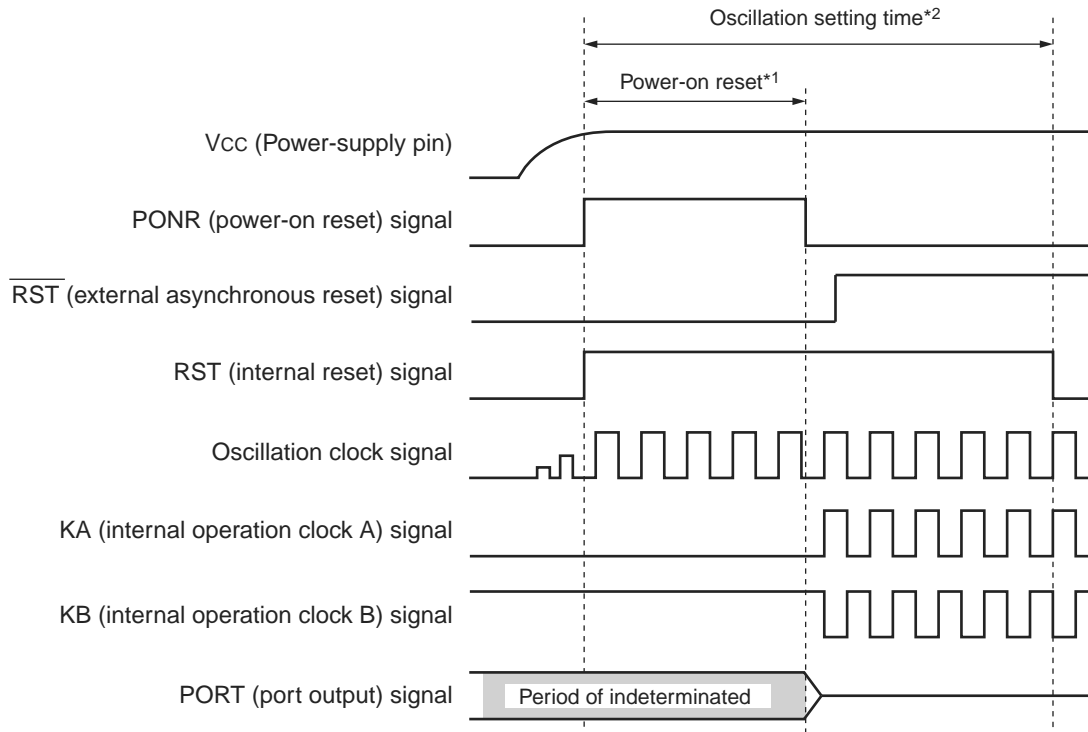


(12) Indeterminate outputs from ports 0 and 1 (MB90V540G only)

During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

- If $\overline{\text{RST}}$ pin is "H", the outputs become indeterminate.
- If $\overline{\text{RST}}$ pin is "L", the outputs become high-impedance.

Pay attention to the port output timing shown as follow.

■ $\overline{\text{RST}}$ pin is "H"


*1 : Power-on reset time : "Period of clock frequency" $\times 2^{17}$ (Clock frequency of 16 MHz : 8.19 ms)

*2 : Oscillation setting time : "Period of clock frequency" $\times 2^{18}$ (Clock frequency of 16 MHz : 16.38 ms)

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
3928 _H	Output Compare Register 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX _B
3929 _H	Output Compare Register 0	OCCP0	R/W		XXXXXXXX _B
392A _H	Output Compare Register 1	OCCP1	R/W		XXXXXXXX _B
392B _H	Output Compare Register 1	OCCP1	R/W		XXXXXXXX _B
392C _H	Output Compare Register 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX _B
392D _H	Output Compare Register 2	OCCP2	R/W		XXXXXXXX _B
392E _H	Output Compare Register 3	OCCP3	R/W		XXXXXXXX _B
392F _H	Output Compare Register 3	OCCP3	R/W		XXXXXXXX _B
3930 _H to 39FF _H	Reserved				
3A00 _H to 3AFF _H	Reserved for CAN 0 Interface.				
3B00 _H to 3BFF _H	Reserved for CAN 0 Interface.				
3C00 _H to 3CFF _H	Reserved for CAN 1 Interface.				
3D00 _H to 3DFF _H	Reserved for CAN 1 Interface.				
3E00 _H to 3FFF _H	Reserved				

■ Read/write notation

R/W : Reading and writing permitted
R : Read-only
W : Write-only

■ Initial value notation

0 : Initial value is "0".
1 : Initial value is "1".
X : Initial value is undefined.
_ : Initial value is unused.

Note: Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading "X".

9. CAN Controller

The MB90540G series contains two CAN controllers (CAN0 and CAN1) , the MB90545G series contains only one (CAN0) . The Evaluation Chip MB90V540G also has two CAN controllers.

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
 - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
 - 29-bit ID and 8-byte data
 - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
 - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 1 Mbps (when input clock is at 16 MHz)

List of Control Registers

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070 _H	000080 _H	Message buffer valid register	BVALR	R/W	00000000 00000000 _B
000071 _H	000081 _H				
000072 _H	000082 _H	Transmit request register	TREQR	R/W	00000000 00000000 _B
000073 _H	000083 _H				
000074 _H	000084 _H	Transmit cancel register	TCANR	W	00000000 00000000 _B
000075 _H	000085 _H				
000076 _H	000086 _H	Transmit complete register	TCR	R/W	00000000 00000000 _B
000077 _H	000087 _H				
000078 _H	000088 _H	Receive complete register	RCR	R/W	00000000 00000000 _B
000079 _H	000089 _H				
00007A _H	00008A _H	Remote request receiving register	RRTRR	R/W	00000000 00000000 _B
00007B _H	00008B _H				
00007C _H	00008C _H	Receive overrun register	ROVRR	R/W	00000000 00000000 _B
00007D _H	00008D _H				
00007E _H	00008E _H	Receive interrupt enable register	RIER	R/W	00000000 00000000 _B
00007F _H	00008F _H				

(Continued)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A24 _H	003C24 _H	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXX _B
003A25 _H	003C25 _H				
003A26 _H	003C26 _H				XXXXXX--- XXXXXXXX _B
003A27 _H	003C27 _H				
003A28 _H	003C28 _H	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXX _B
003A29 _H	003C29 _H				
003A2A _H	003C2A _H				XXXXXX--- XXXXXXXX _B
003A2B _H	003C2B _H				
003A2C _H	003C2C _H	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX _B
003A2D _H	003C2D _H				
003A2E _H	003C2E _H				XXXXXX--- XXXXXXXX _B
003A2F _H	003C2F _H				
003A30 _H	003C30 _H	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX _B
003A31 _H	003C31 _H				
003A32 _H	003C32 _H				XXXXXX--- XXXXXXXX _B
003A33 _H	003C33 _H				
003A34 _H	003C34 _H	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX _B
003A35 _H	003C35 _H				
003A36 _H	003C36 _H				XXXXXX--- XXXXXXXX _B
003A37 _H	003C37 _H				
003A38 _H	003C38 _H	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX _B
003A39 _H	003C39 _H				
003A3A _H	003C3A _H				XXXXXX--- XXXXXXXX _B
003A3B _H	003C3B _H				

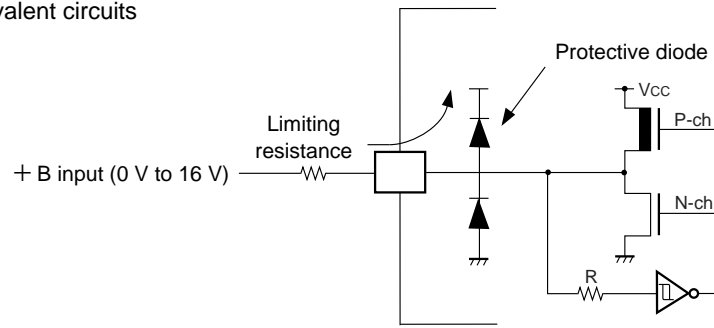
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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A3C _H	003C3C _H	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX _B
003A3D _H	003C3D _H				
003A3E _H	003C3E _H				XXXXX--- XXXXXXXX _B
003A3F _H	003C3F _H				
003A40 _H	003C40 _H	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX _B
003A41 _H	003C41 _H				
003A42 _H	003C42 _H				XXXXX--- XXXXXXXX _B
003A43 _H	003C43 _H				
003A44 _H	003C44 _H	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX _B
003A45 _H	003C45 _H				
003A46 _H	003C46 _H				XXXXX--- XXXXXXXX _B
003A47 _H	003C47 _H				
003A48 _H	003C48 _H	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX _B
003A49 _H	003C49 _H				
003A4A _H	003C4A _H				XXXXX--- XXXXXXXX _B
003A4B _H	003C4B _H				
003A4C _H	003C4C _H	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX _B
003A4D _H	003C4D _H				
003A4E _H	003C4E _H				XXXXX--- XXXXXXXX _B
003A4F _H	003C4F _H				
003A50 _H	003C50 _H	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX _B
003A51 _H	003C51 _H				
003A52 _H	003C52 _H				XXXXX--- XXXXXXXX _B
003A53 _H	003C53 _H				
003A54 _H	003C54 _H	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX _B
003A55 _H	003C55 _H				
003A56 _H	003C56 _H				XXXXX--- XXXXXXXX _B
003A57 _H	003C57 _H				
003A58 _H	003C58 _H	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX _B
003A59 _H	003C59 _H				
003A5A _H	003C5A _H				XXXXX--- XXXXXXXX _B
003A5B _H	003C5B _H				
003A5C _H	003C5C _H	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX _B
003A5D _H	003C5D _H				
003A5E _H	003C5E _H				XXXXX--- XXXXXXXX _B
003A5F _H	003C5F _H				

- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept + B signal input.
- Sample recommended circuits :

■ Input/Output Equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

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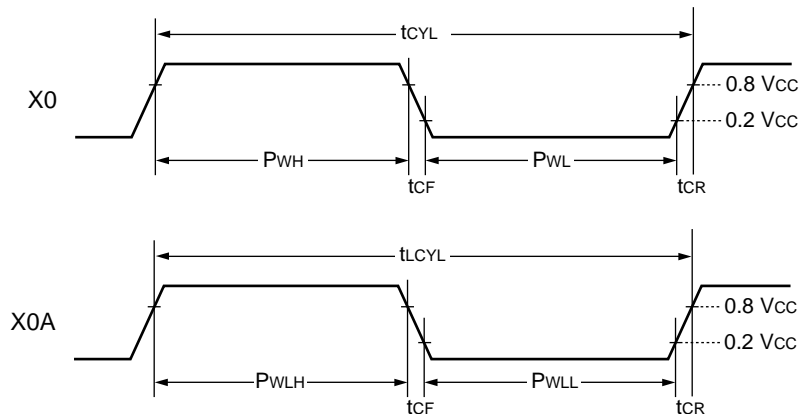
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

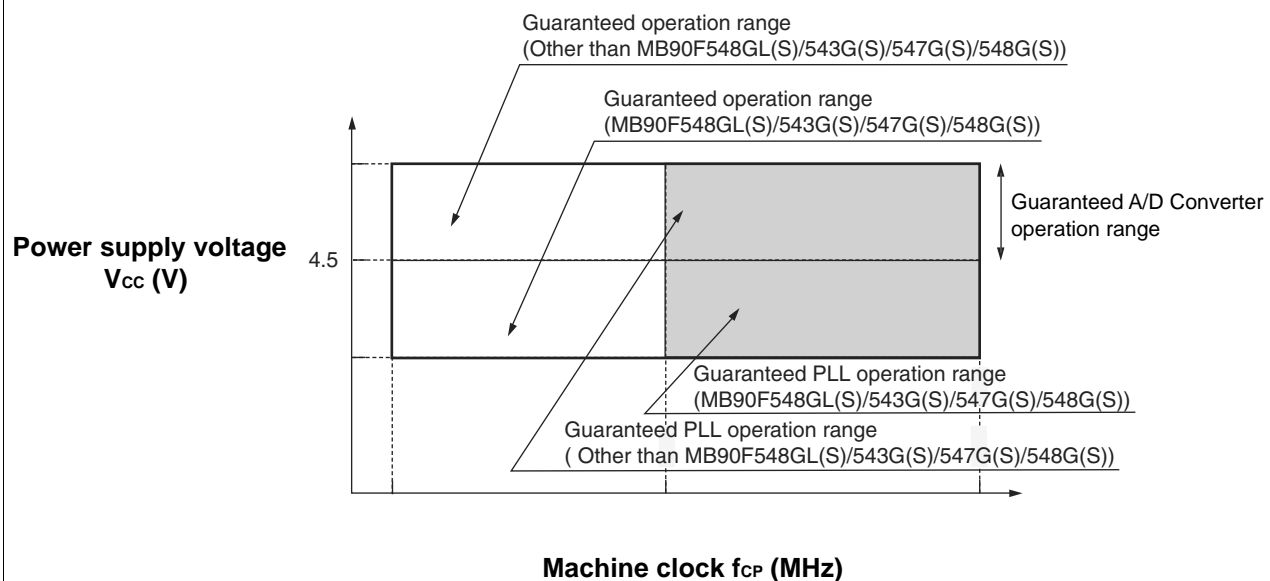
Parameter	Sym- bol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Power supply current*	I _{CC}	V _{CC}	Internal frequency : 16 MHz, At normal operating	—	40	55	mA	
			Internal frequency : 16 MHz, At Flash programming/erasing	—	50	70	mA	Flash device
	I _{CCS}		Internal frequency : 16 MHz, At sleep mode	—	12	20	mA	
	I _{CTS}		V _{CC} = 5.0 V ± 10%, Internal frequency : 2 MHz, At pseudo timer mode	—	300	600	μA	
				—	600	1100	μA	MB90F548GL (S) only
				—	200	400	μA	MB90543G(S)/547G(S)/548(S) only
	I _{CCL}		Internal frequency : 8 kHz, At sub operation, T _A = 25 °C	—	400	750	μA	MB90F548GL only
				—	50	100	μA	MASK ROM
				—	150	300	μA	Flash device
	I _{CCLS}		Internal frequency : 8 kHz, At sub sleep, T _A = 25 °C	—	15	40	μA	
I _{CCT}	Internal frequency : 8 kHz, At timer mode, T _A = 25 °C	—	7	25	μA			
I _{CH1}	At stop, T _A = 25 °C	—	5	20	μA			
I _{CH2}	At hardware standby mode, T _A = 25 °C	—	50	100	μA			
Input capacity	C _{IN}	Other than AV _{CC} , AV _{SS} , AV _{RH} , AV _{RL} , C, V _{CC} , V _{SS}	—	—	5	15	pF	

* : The power supply current testing conditions are when using the external clock.

■ Clock Timing



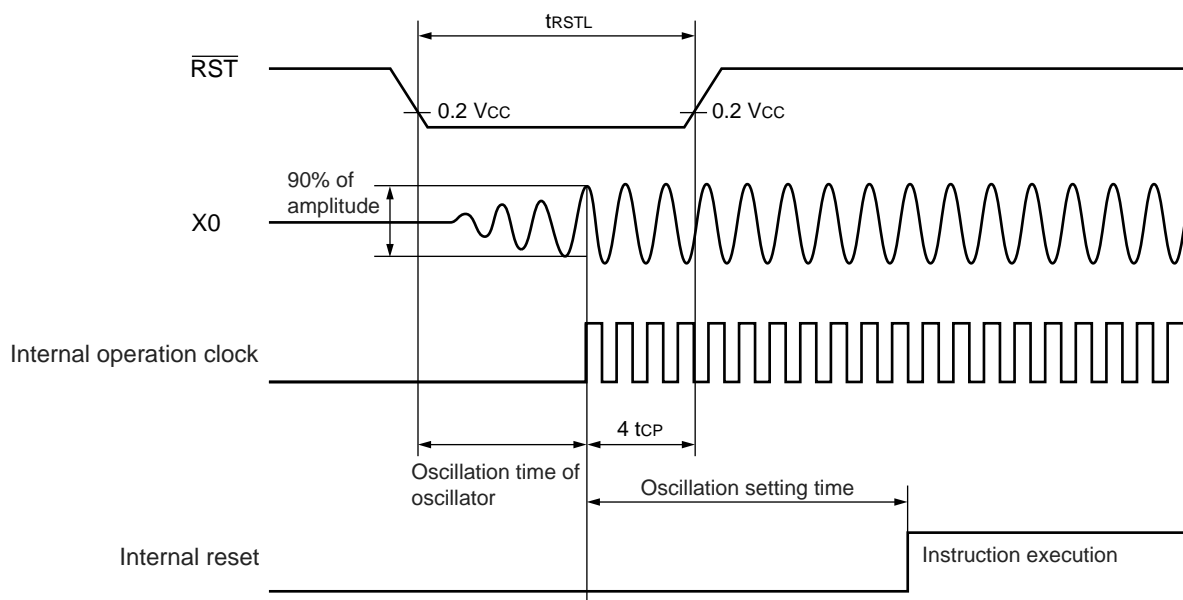
■ Guaranteed PLL operation range



- In under normal operation, pseudo timer mode, sub-clock mode, sub-sleep mode, timer mode



- In stop mode

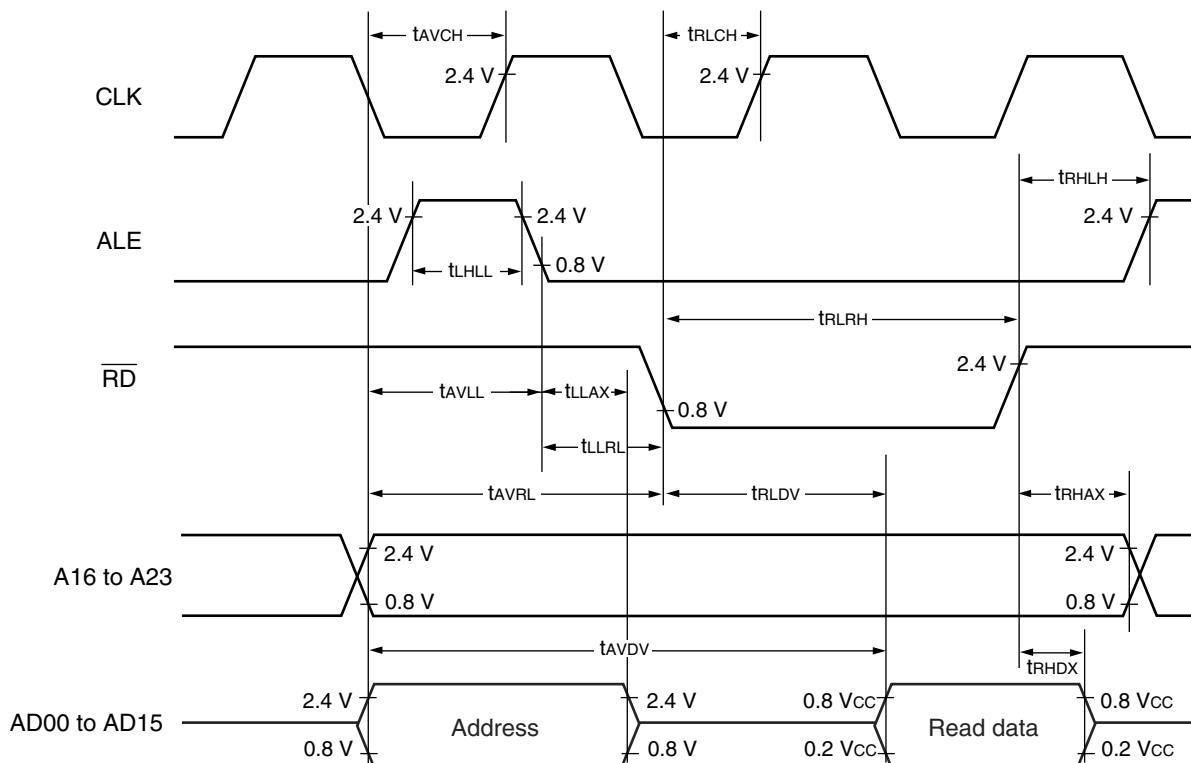


11.4.5 Bus Timing (Read)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 20$	—	ns	
Valid address → ALE↓ time	t_{AVLL}	ALE, A16 to A23, AD00 to AD15		$t_{CP}/2 - 20$	—	ns	
ALE↓ → Address valid time	t_{LLAX}	ALE, AD00 to AD15		$t_{CP}/2 - 15$	—	ns	
Valid address → \overline{RD} ↓ time	t_{AVRL}	A16 to A23, AD00 to AD15, RD		$t_{CP} - 15$	—	ns	
Valid address → Valid data input	t_{AVDV}	A16 to A23, AD00 to AD15		—	$5 t_{CP}/2 - 60$	ns	
\overline{RD} pulse width	t_{RLRH}	RD		$3 t_{CP}/2 - 20$	—	ns	
\overline{RD} ↓ → Valid data input	t_{RLDV}	\overline{RD} , AD00 to AD15		—	$3 t_{CP}/2 - 60$	ns	
\overline{RD} ↑ → Data hold time	t_{RHDX}	\overline{RD} , AD00 to AD15		0	—	ns	
\overline{RD} ↑ → ALE↑ time	t_{RHLH}	\overline{RD} , ALE		$t_{CP}/2 - 15$	—	ns	
\overline{RD} ↑ → Address valid time	t_{RHAX}	\overline{RD} , A16 to A23		$t_{CP}/2 - 10$	—	ns	
Valid address → CLK↑ time	t_{AVCH}	A16 to A23, AD00 to AD15, CLK		$t_{CP}/2 - 20$	—	ns	
\overline{RD} ↓ → CLK↑ time	t_{RLCH}	\overline{RD} , CLK		$t_{CP}/2 - 20$	—	ns	
ALE↓ → \overline{RD} ↓ time	t_{LLRL}	ALE, \overline{RD}		$t_{CP}/2 - 15$	—	ns	

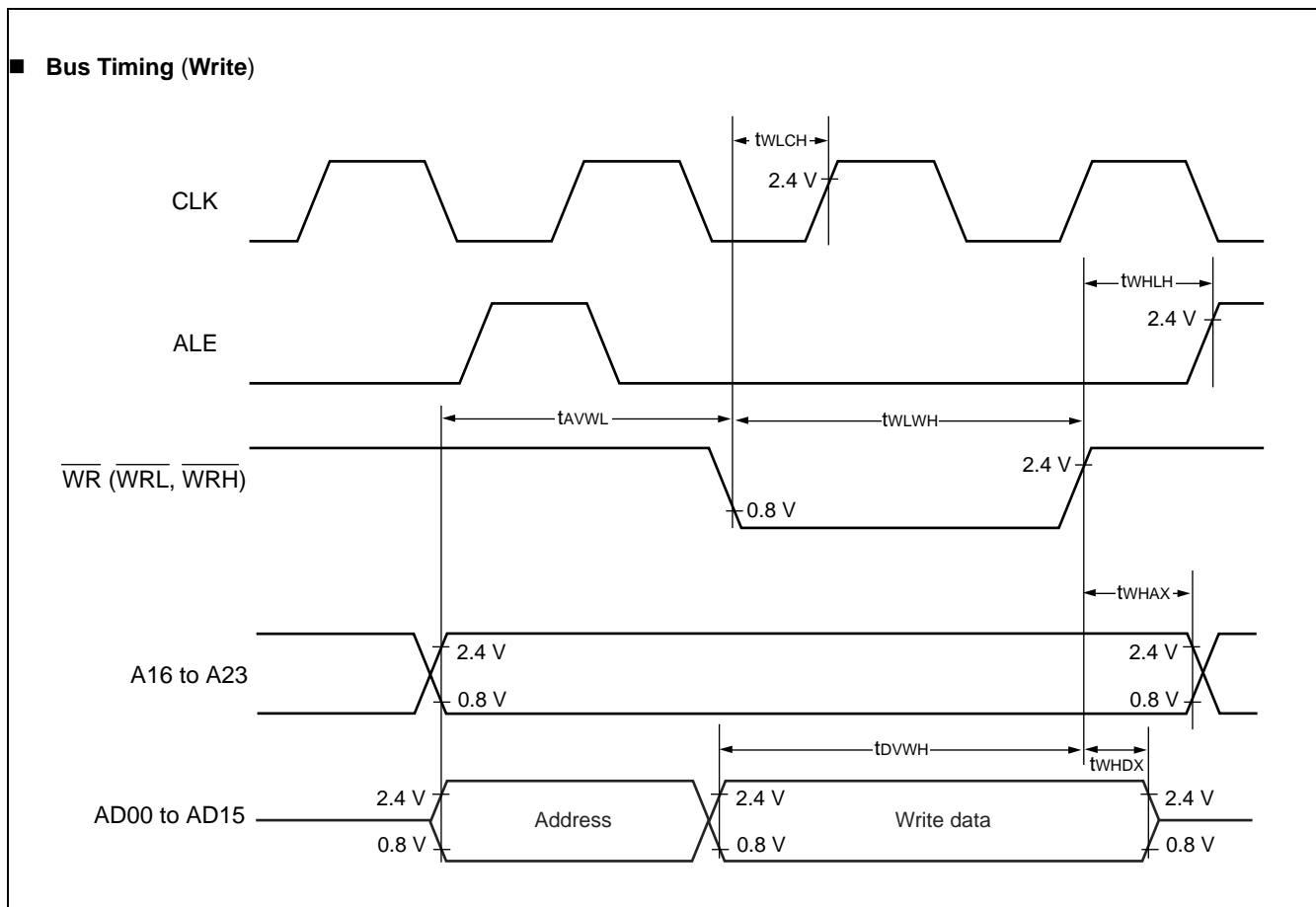
■ Bus Timing (Read)


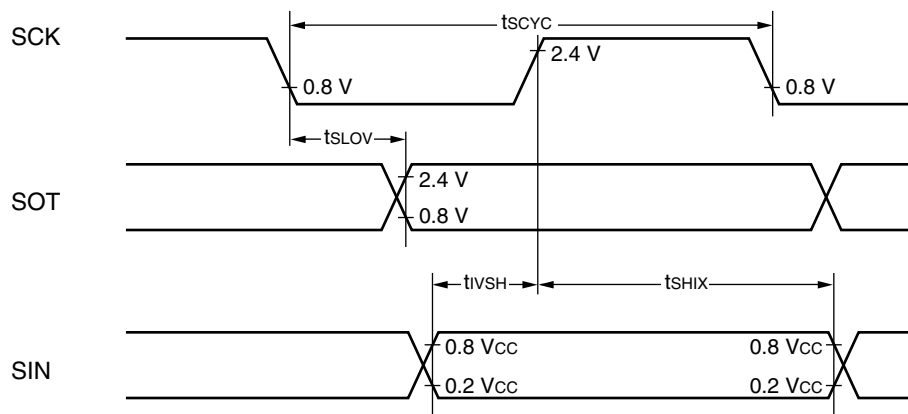
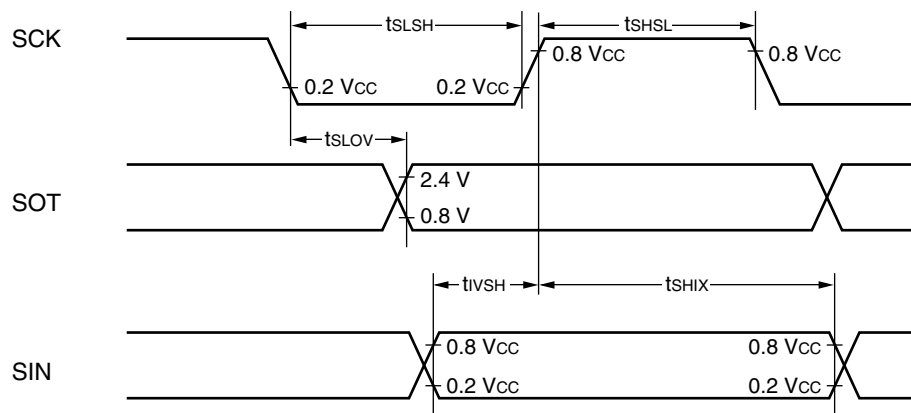
11.4.6 Bus Timing (Write)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Valid address $\rightarrow \overline{WR}\downarrow$ time	t_{AVWL}	A16 to A23 AD00 to AD15, \overline{WR}	—	$t_{CP} - 15$	—	ns	
\overline{WR} pulse width	t_{WLWH}	WR		$3 t_{CP}/2 - 20$	—	ns	
Valid data output $\rightarrow \overline{WR}\uparrow$ time	t_{DVWH}	AD00 to AD15, \overline{WR}		$3 t_{CP}/2 - 20$	—	ns	
$\overline{WR}\uparrow \rightarrow$ Data hold time	t_{WHDX}	AD00 to AD15, \overline{WR}		20	—	ns	
$\overline{WR}\uparrow \rightarrow$ Address valid time	t_{WHAX}	A16 to A23, \overline{WR}		$t_{CP}/2 - 10$	—	ns	
$\overline{WR}\uparrow \rightarrow$ ALE \uparrow time	t_{WHLH}	\overline{WR} , ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{WR}\uparrow \rightarrow$ CLK \uparrow time	t_{WLCH}	\overline{WR} , CLK		$t_{CP}/2 - 20$	—	ns	



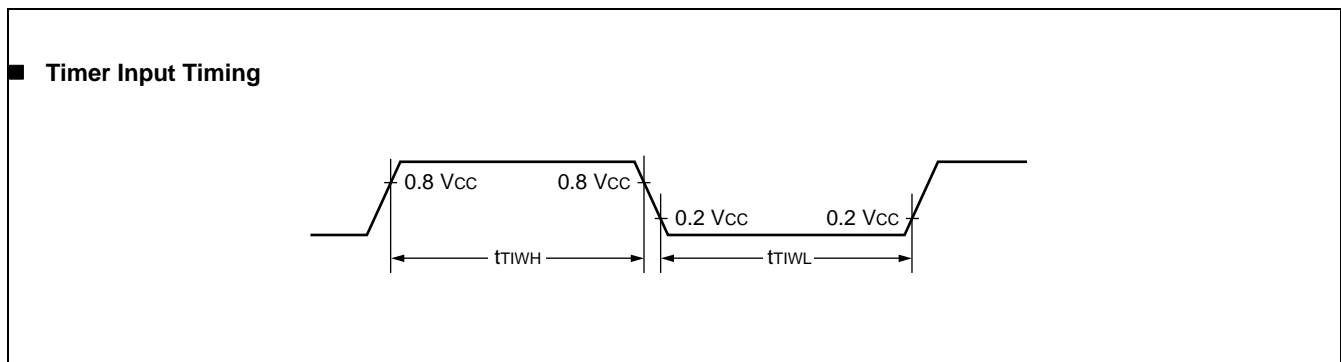
Internal Shift Clock Mode

External Shift Clock Mode


11.4.10 Timer Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	$4\ t_{CP}$	—	ns	
	t_{TIWL}	IN0 to IN7					

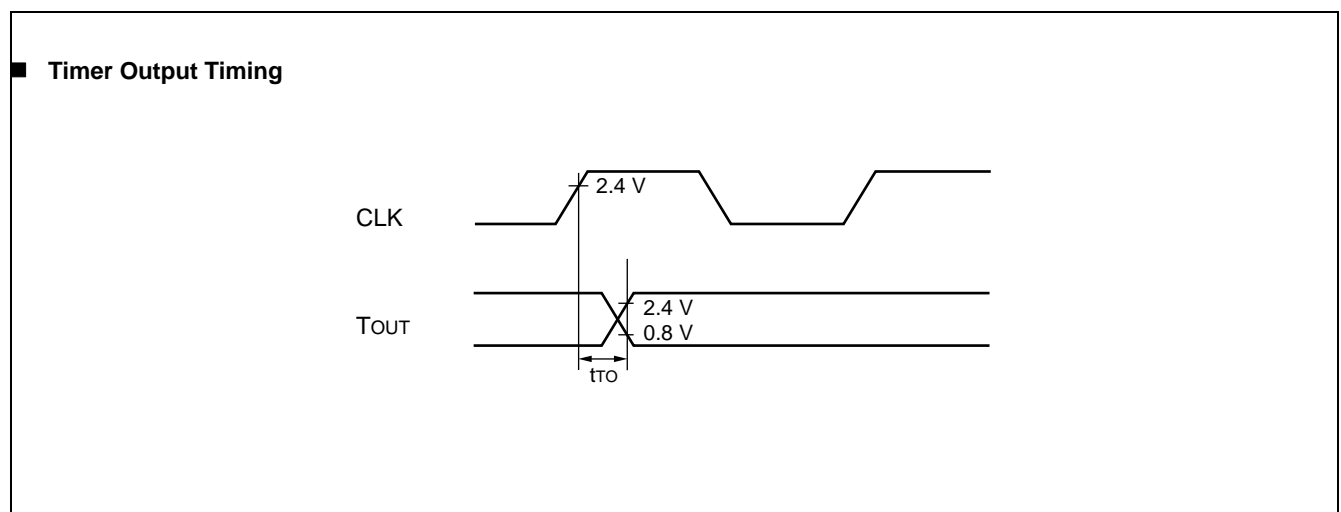


11.4.11 Timer Output Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
CLK \uparrow → TOUT change time	t_{TO}	TOT0, TOT1, PPG0 to PPG3	—	30	—	ns	



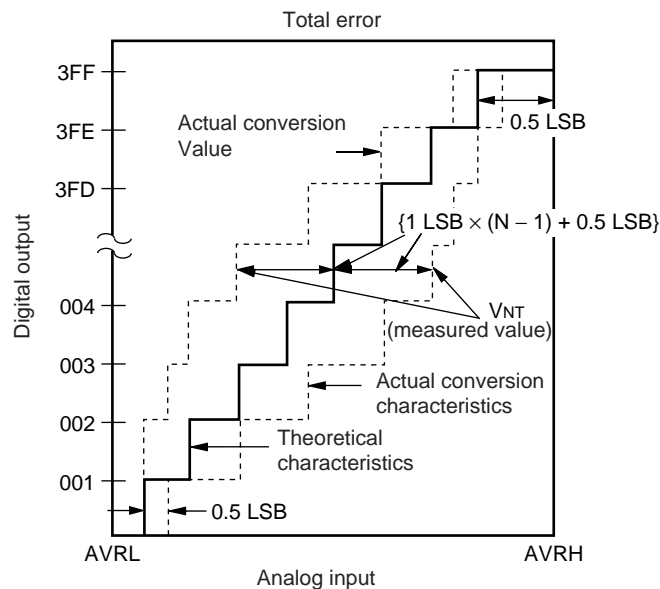
11.5.2 A/D Converter Glossary

Resolution : Analog changes that are identifiable with the A/D converter

Linearity error : The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ↔ "11 1111 1111") from actual conversion characteristics

Differential linearity error : The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error : The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1 \text{ LSB} = (\text{Theoretical value}) \frac{AVRH - AVRL}{1024} [\text{V}]$$

$$V_{OT} (\text{Theoretical value}) = AVRL + 0.5 \text{ LSB} [\text{V}]$$

$$V_{FST} (\text{Theoretical value}) = AVRH - 1.5 \text{ LSB} [\text{V}]$$

$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} [\text{LSB}]$$

V_{NT} : Voltage at a transition of digital output from (N - 1) to N

(Continued)

13. Ordering Information

Part number	Package	Remarks
MB90F543GPF MB90F543GSPF MB90F546GPF MB90F546GSPF MB90F548GPF MB90F548GSPF MB90F548GLPF MB90F548GLSPF MB90F549GPF MB90F549GSPF MB90543GPF MB90543GSPF MB90547GPF MB90547GSPF MB90548GPF MB90548GSPF MB90549GPF MB90549GSPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90F543GPMC MB90F543GSPMC MB90F546GPMC MB90F546GSPMC MB90F548GPMC MB90F548GSPMC MB90F548GLPMC MB90F548GLSPMC MB90F549GPMC MB90F549GSPMC MB90543GPMC MB90543GSPMC MB90547GPMC MB90547GSPMC MB90548GPMC MB90548GSPMC MB90549GPMC MB90549GSPMC	100-pin Plastic LQFP (FPT-100P-M20)	

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