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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspf-gs-9018

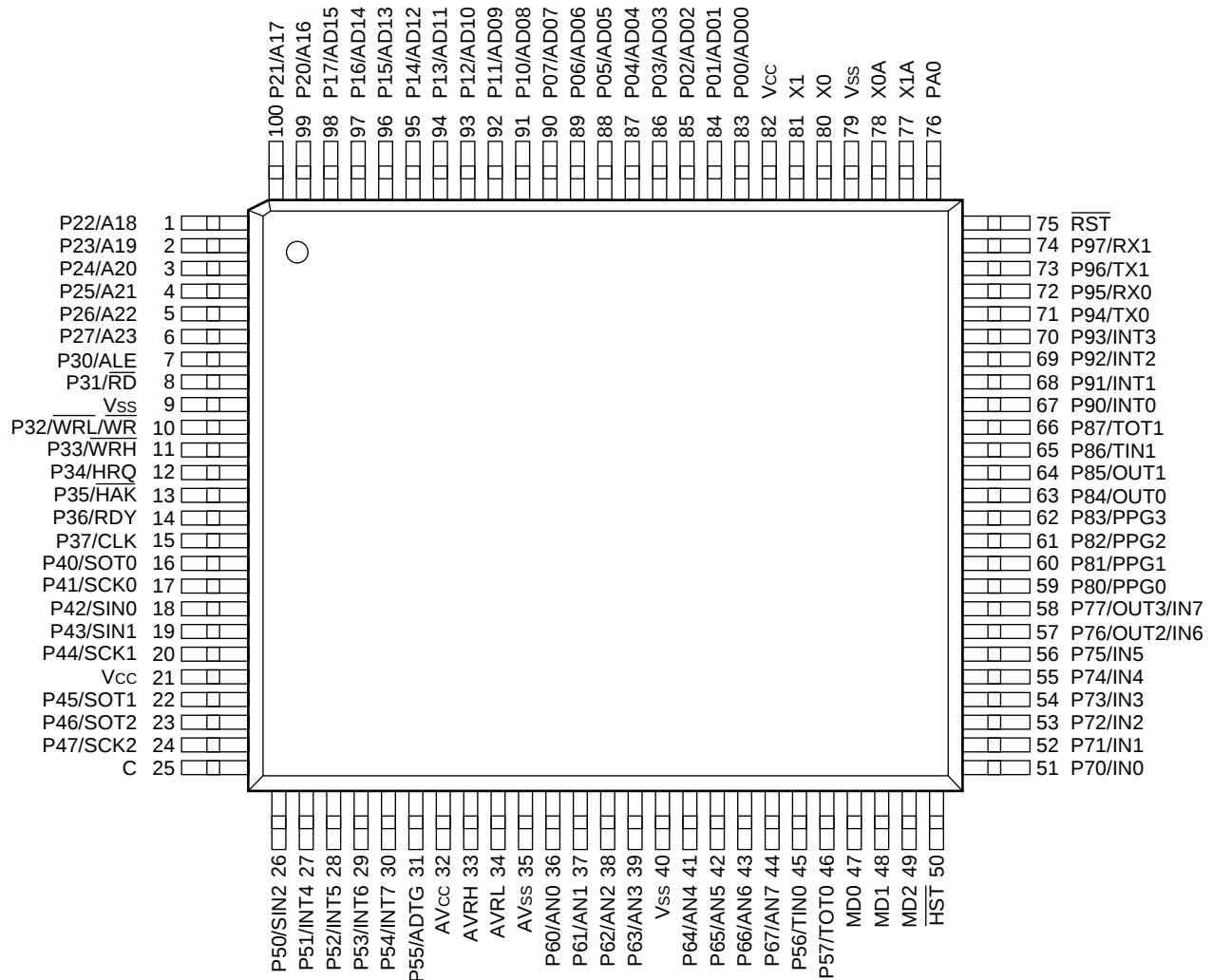
Starting by an external trigger input.
Conversion time : 26.3 μ s

- FULL-CAN interfaces
MB90540G series : 2 channels
MB90545G series : 1 channel
Conforming to Version 2.0 Part A and Part B

Flexible message buffering (mailbox and FIFO buffering can be mixed)

- External bus interface : Maximum address space 16 Mbytes
- Package: QFP-100, LQFP-100

(TOP VIEW)

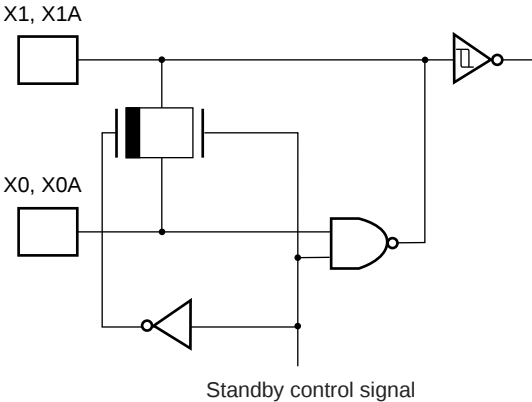
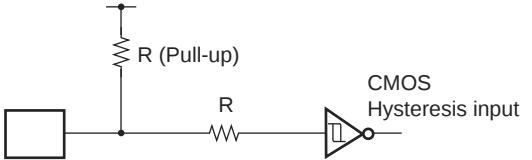
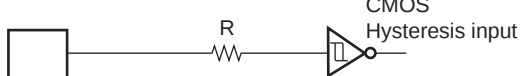
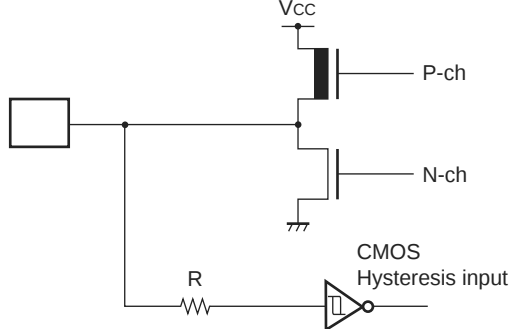


(FPT-100P-M20)

Pin No.		Pin name	Circuit type	Function
LQFP ²	QFP ¹			
46	48	P57	D	General I/O port. This function is enabled when the 16-bit reload timers 0 disables the output.
		TOT0		Output pin for the 16-bit reload timers 0. This function is enabled when the 16-bit reload timers 0 enables the output.
51 to 56	53 to 58	P70 to P75	D	General I/O ports. This function is always enabled.
		IN0 to IN5		Trigger input pins for input captures ICU0 to ICU5. Set the corresponding Port Direction Register to input if this function is used.
57 , 58	59 , 60	P76 , P77	D	General I/O ports. This function is enabled when the OCU disables the waveform output.
		OUT2 , OUT3		Event output pins for output compares OCU2 and OCU3. This function is enabled when the OCU enables the waveform output.
		IN6 , IN7		Trigger input pins for input captures ICU6 and ICU7. Set the corresponding Port Direction Register to input and disable the OCU waveform output if this function is used.
59 to 62	61 to 64	P80 to P83	D	General I/O ports. This function is enabled when 8/16-bit PPG disables the waveform output.
		PPG0 to PPG3		Output pins for 8/16-bit PPGs. This function is enabled when 8/16-bit PPG enables the waveform output.
63 , 64	65 , 66	P84 , P85	D	General I/O ports. This function is enabled when the OCU disables the waveform output.
		OUT0 , OUT1		Waveform output pins for output compares OCU0 and OCU1. This function is enabled when the OCU enables the waveform output.
65	67	P86	D	General I/O port. This function is always enabled.
		TIN1		Input pin for the 16-bit reload timers 1. Set the corresponding Port Direction Register to input if this function is used.
66	68	P87	D	General I/O port. This function is enabled when the 16-bit reload timers 1 disables the output.
		TOT1		Output pin for the 16-bit reload timers 1. This function is enabled when the 16-bit reload timers 1 enables the output.
67 to 70	69 to 72	P90 to P93	D	General I/O port. This function is always enabled.
		INT0 to INT3		External interrupt request input pins for INT0 to INT3. Set the corresponding Port Direction Register to input if this function is used.
71	73	P94	D	General I/O port. This function is enabled when CAN0 disables the output.
		TX0		TX output pin for CAN0. This function is enabled when CAN0 enables the output.

(Continued)

4. I/O Circuit Type

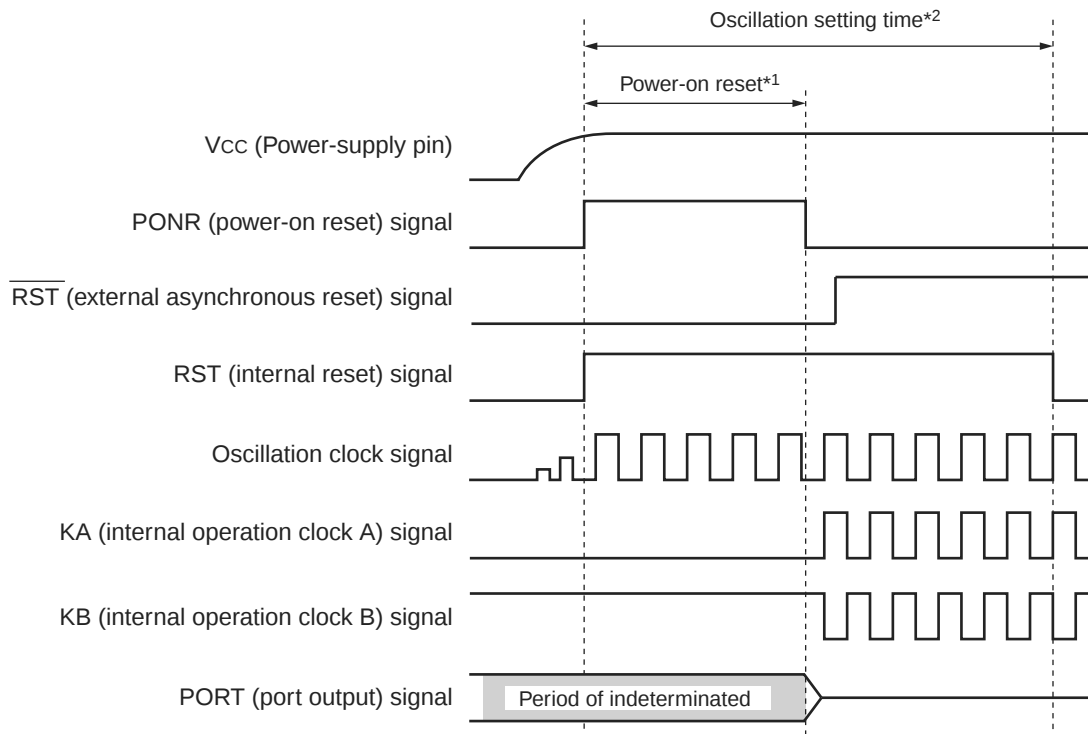
Circuit type	Diagram	Remarks
A	 Standby control signal	■ High-speed oscillation feedback resistor : 1 MΩ approx. ■ Low-speed oscillation feedback resistor: 10 MΩ approx.
B	 R (Pull-up) R CMOS Hysteresis input	■ CMOS Hysteresis input ■ Pull-up resistor : 50 kΩ approx.
C	 R CMOS Hysteresis input	■ CMOS Hysteresis input
D	 Vcc P-ch N-ch CMOS Hysteresis input R	■ CMOS level output ■ CMOS Hysteresis input

(Continued)

(12) Indeterminate outputs from ports 0 and 1 (MB90V540G only)

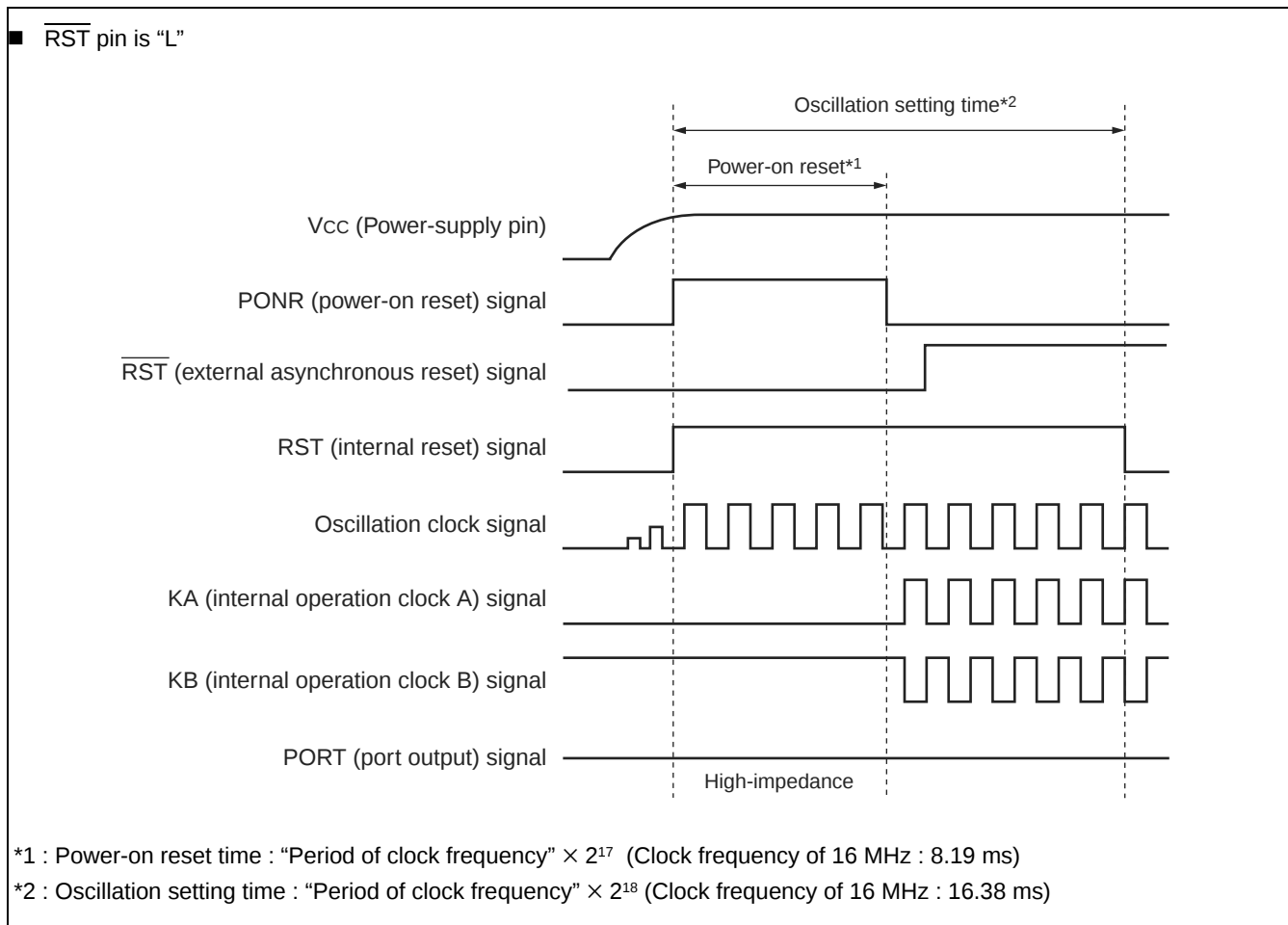
During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

- If $\overline{\text{RST}}$ pin is "H", the outputs become indeterminate.
 - If $\overline{\text{RST}}$ pin is "L", the outputs become high-impedance.
- Pay attention to the port output timing shown as follow.

■ $\overline{\text{RST}}$ pin is "H"


*1 : Power-on reset time : "Period of clock frequency" $\times 2^{17}$ (Clock frequency of 16 MHz : 8.19 ms)

*2 : Oscillation setting time : "Period of clock frequency" $\times 2^{18}$ (Clock frequency of 16 MHz : 16.38 ms)



(13) Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(14) Directions of "DIV A, Ri" and "DIVW A, RWi" instructions

In the Signed multiplication and division instructions ("DIV A, Ri" and "DIVW A, RWi"), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in "00H".

If the values of the corresponding bank registers (DTB, ADB, USB, SSB) are set to other than "00H", the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

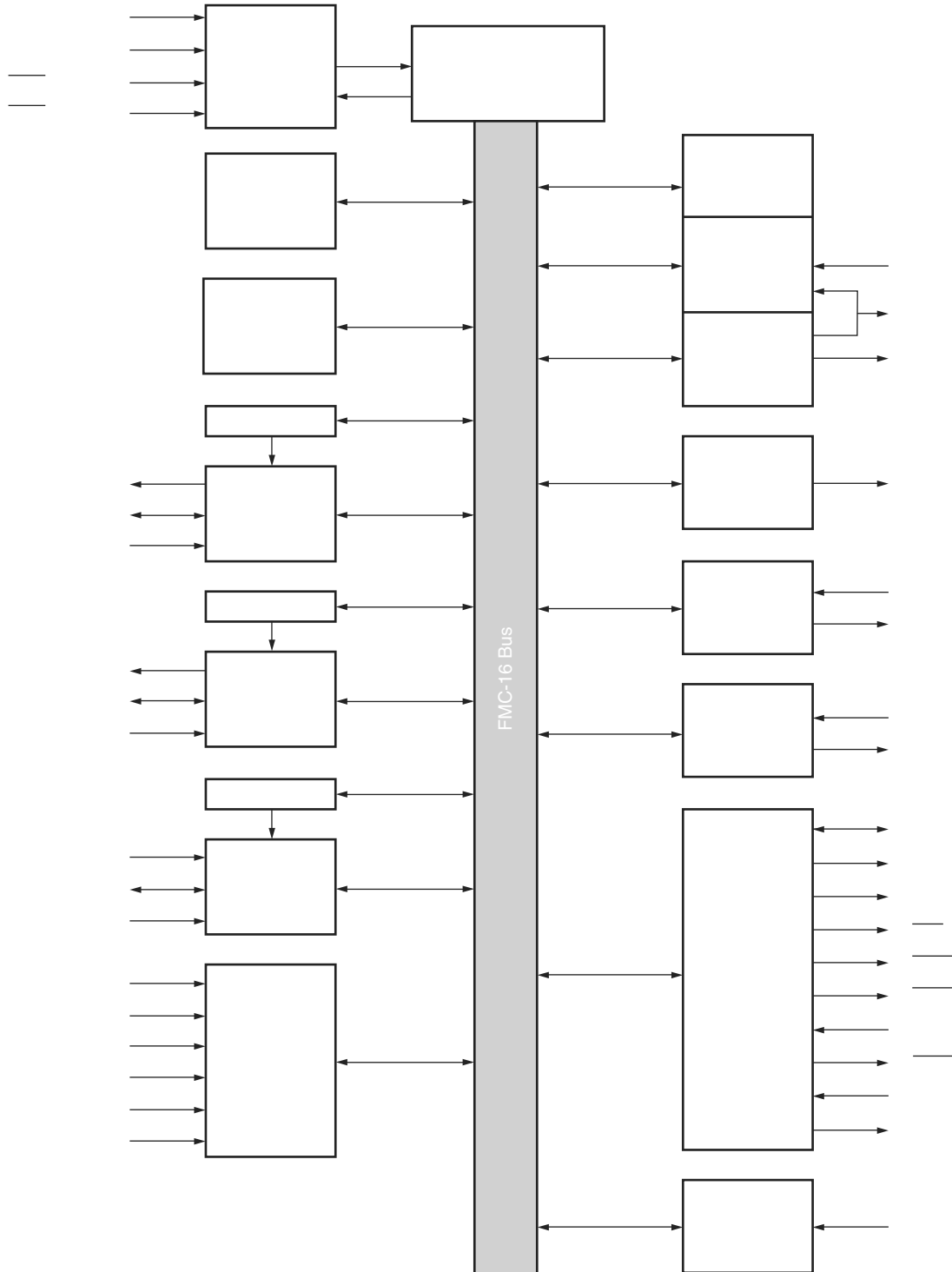
(15) Using REALOS

The use of EI²OS is not possible with the REALOS real time operating system.

(16) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

6. Block Diagram



* : Only the MB90540G series has two channels

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
3928 _H	Output Compare Register 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX _B
3929 _H	Output Compare Register 0	OCCP0	R/W		XXXXXXXX _B
392A _H	Output Compare Register 1	OCCP1	R/W		XXXXXXXX _B
392B _H	Output Compare Register 1	OCCP1	R/W		XXXXXXXX _B
392C _H	Output Compare Register 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX _B
392D _H	Output Compare Register 2	OCCP2	R/W		XXXXXXXX _B
392E _H	Output Compare Register 3	OCCP3	R/W		XXXXXXXX _B
392F _H	Output Compare Register 3	OCCP3	R/W		XXXXXXXX _B
3930 _H to 39FF _H	Reserved				
3A00 _H to 3AFF _H	Reserved for CAN 0 Interface.				
3B00 _H to 3BFF _H	Reserved for CAN 0 Interface.				
3C00 _H to 3CFF _H	Reserved for CAN 1 Interface.				
3D00 _H to 3DFF _H	Reserved for CAN 1 Interface.				
3E00 _H to 3FFF _H	Reserved				

■ Read/write notation

R/W : Reading and writing permitted
R : Read-only
W : Write-only

■ Initial value notation

0 : Initial value is "0".
1 : Initial value is "1".
X : Initial value is undefined.
— : Initial value is unused.

Note: Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading "X".

(Continued)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A88 _H to 003A8F _H	003C88 _H to 003C8F _H	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
003A90 _H to 003A97 _H	003C90 _H to 003C97 _H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
003A98 _H to 003A9F _H	003C98 _H to 003C9F _H	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
003AA0 _H to 003AA7 _H	003CA0 _H to 003CA7 _H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
003AA8 _H to 003AAF _H	003CA8 _H to 003CAF _H	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
003AB0 _H to 003AB7 _H	003CB0 _H to 003CB7 _H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
003AB8 _H to 003ABF _H	003CB8 _H to 003CBF _H	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
003AC0 _H to 003AC7 _H	003CC0 _H to 003CC7 _H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
003AC8 _H to 003ACF _H	003CC8 _H to 003CCF _H	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
003AD0 _H to 003AD7 _H	003CD0 _H to 003CD7 _H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
003AD8 _H to 003ADF _H	003CD8 _H to 003CDF _H	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
003AE0 _H to 003AE7 _H	003CE0 _H to 003CE7 _H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
003AE8 _H to 003AEF _H	003CE8 _H to 003CEF _H	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B
003AF0 _H to 003AF7 _H	003CF0 _H to 003CF7 _H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
003AF8 _H to 003AFF _H	003CF8 _H to 003CFF _H	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

11.2 Recommended Conditions

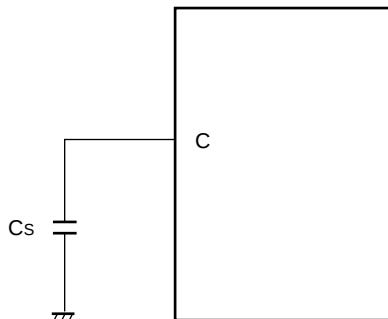
($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value			Units	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.5	5.0	5.5	V	Under normal operation : Other than MB90F548GL(S)/543G(S)/547G(S)/548G(S)
						Under normal operation when A/D converter is used : MB90F548GL(S)/543G(S)/547G(S)/548G(S)
		3.5	5.0	5.5	V	Under normal operation when A/D converter is not used : MB90F548GL(S)/543G(S)/547G(S)/548G(S)
		3.0	—	5.5	V	Maintain RAM data in stop mode
Smooth capacitor	C_S	0.022	0.1	1.0	μF	*
Operating temperature	T_A	−40	—	+105	°C	

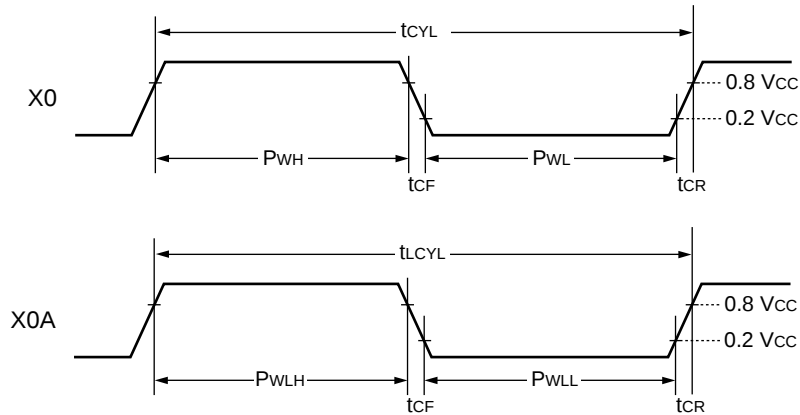
*: Use a ceramic capacitor or a capacitor of better 4. AC characteristics. The bypass capacitor should be greater than this capacitor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

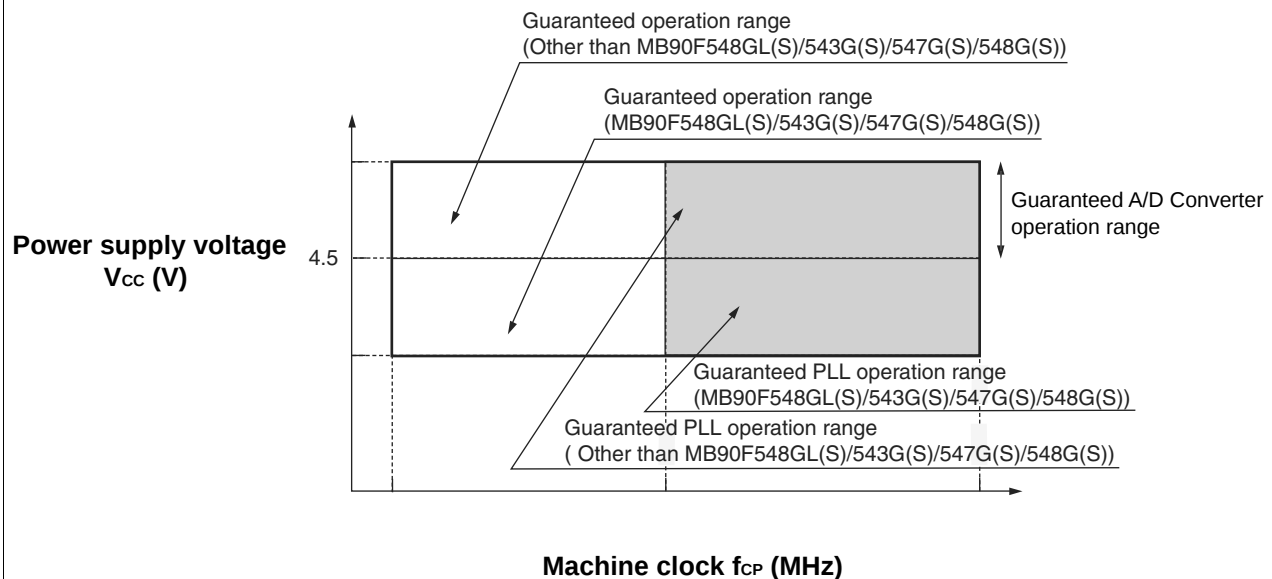
■ C Pin Connection Diagram



■ Clock Timing



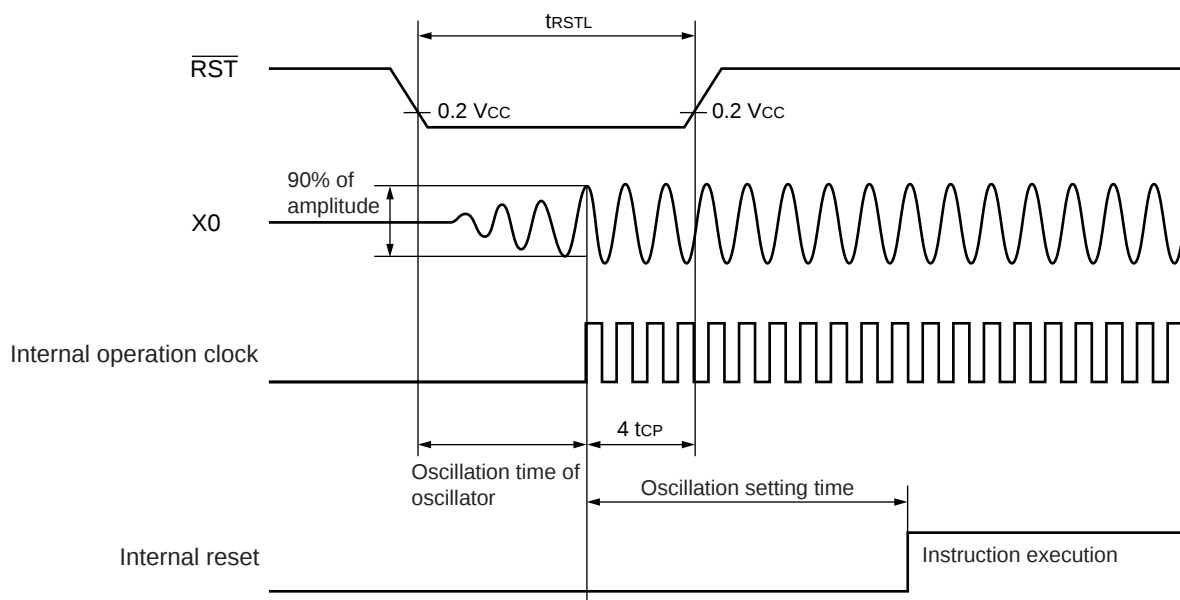
■ Guaranteed PLL operation range



- In under normal operation, pseudo timer mode, sub-clock mode, sub-sleep mode, timer mode



- In stop mode



[illegible]

11.4.8 Hold Timing

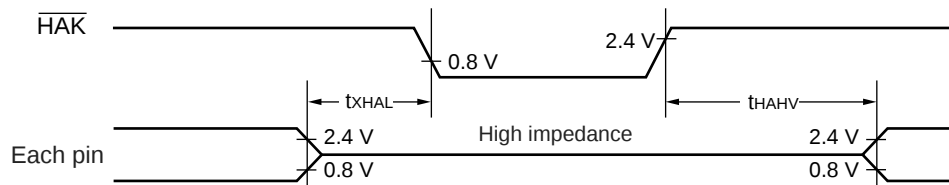
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Pin floating → $\overline{\text{HAK}}\downarrow$ time	t_{XHAL}	$\overline{\text{HAK}}$	—	30	t_{CP}	ns	
$\overline{\text{HAK}}\uparrow$ time → Pin valid time	t_{HAHV}	$\overline{\text{HAK}}$	—	t_{CP}	$2 t_{CP}$	ns	

Note : There is more than 1 cycle from the time HRQ is read to the time the $\overline{\text{HAK}}$ is changed.

■ Hold Timing



11.4.9 UART0/1, Serial I/O Timing

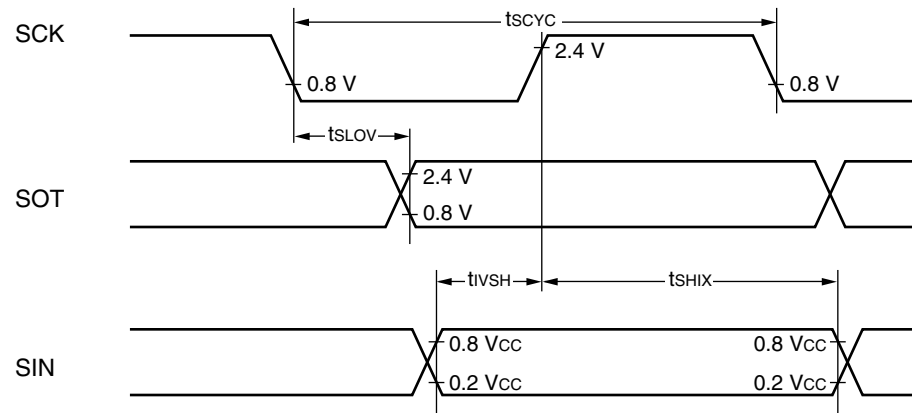
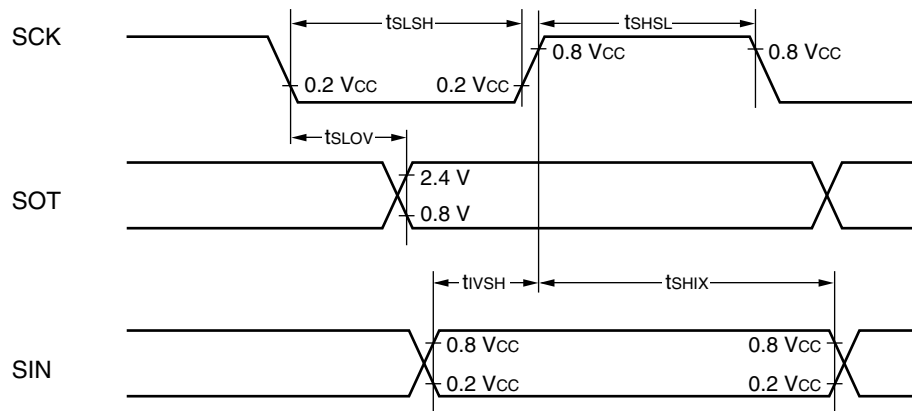
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$8 t_{CP}$	—	ns	
SCK↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		— 80	80	ns	
Valid SIN → SCK↑	t_{VSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK2	External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$4 t_{CP}$	—	ns	
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK2		$4 t_{CP}$	—	ns	
SCK↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN → SCK↑	t_{VSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

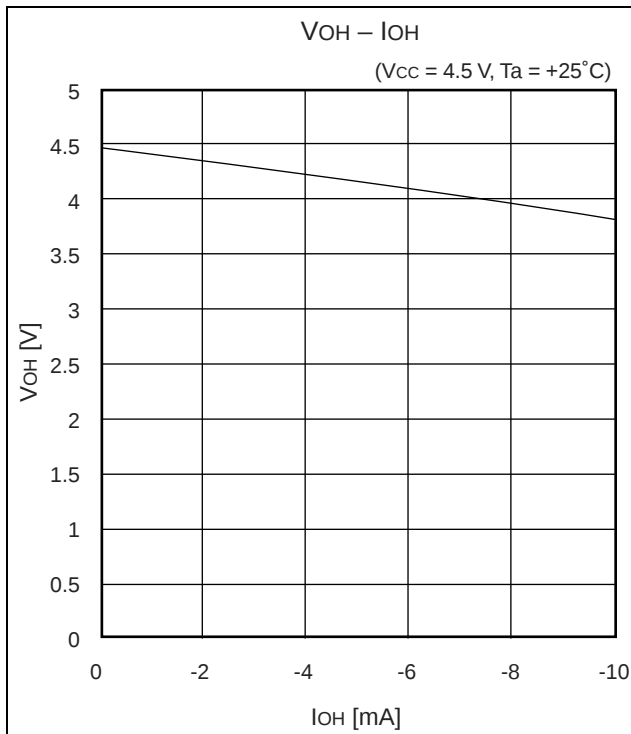
Notes :

- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- For t_{CP} (Machine clock cycle time) , refer to “ (1) Clock Timing”.

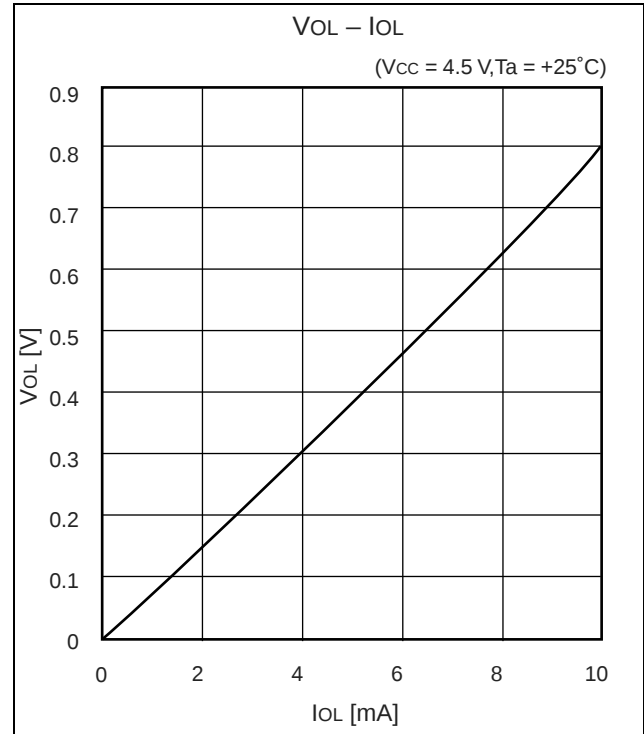
Internal Shift Clock Mode

External Shift Clock Mode


12. Example Characteristics

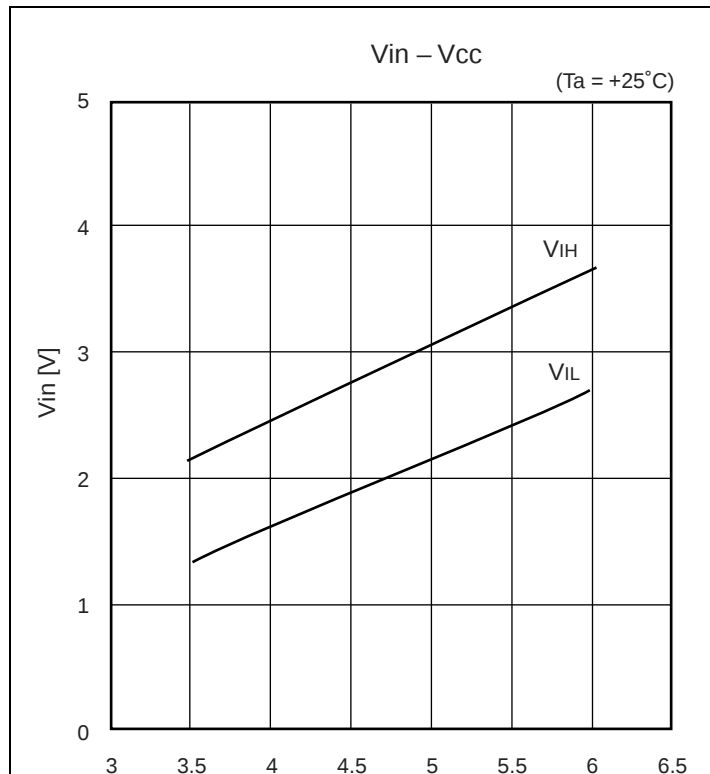
■ “H” level output voltage

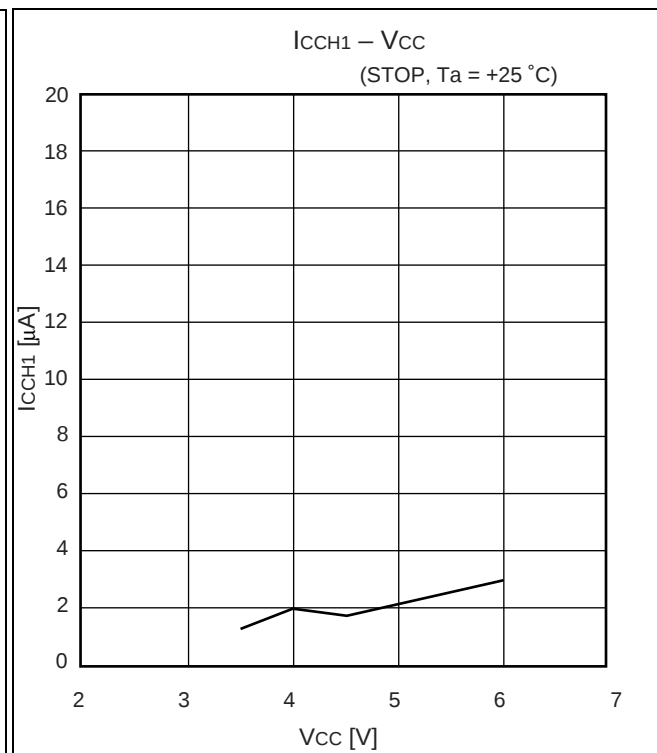
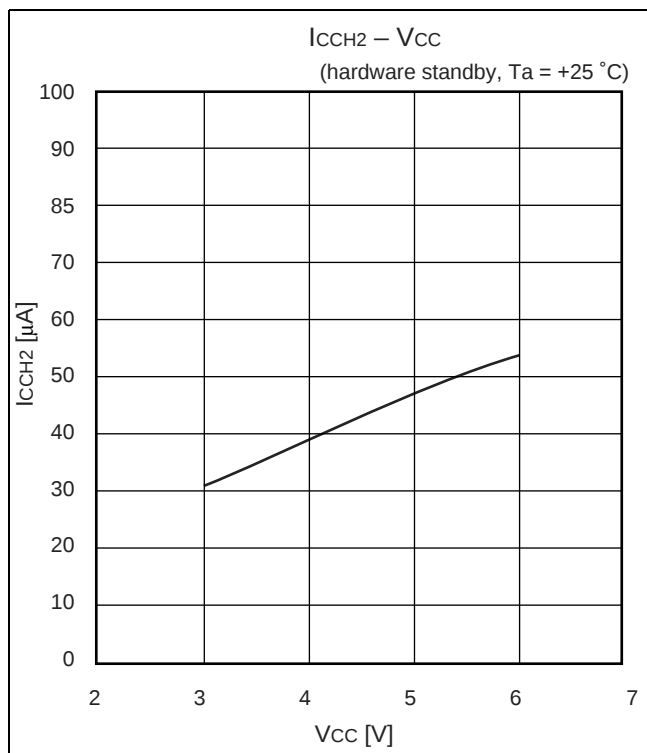
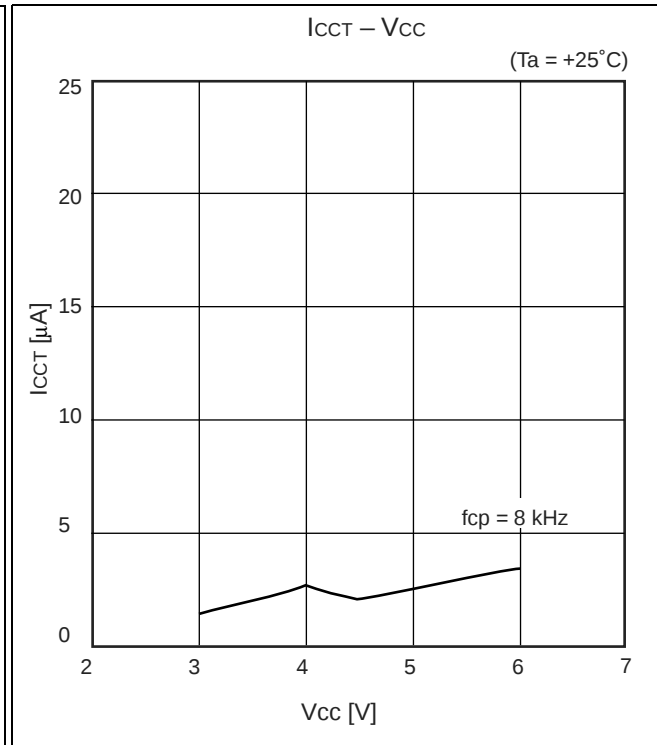
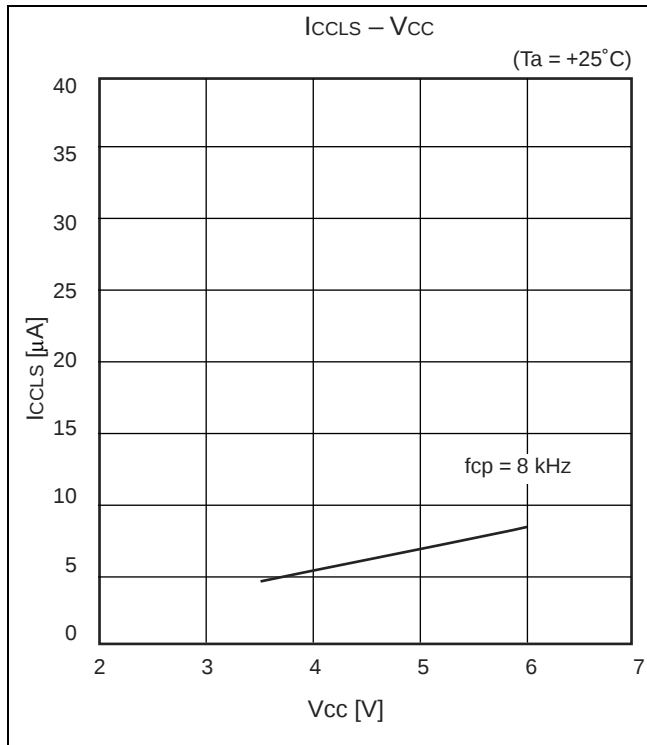


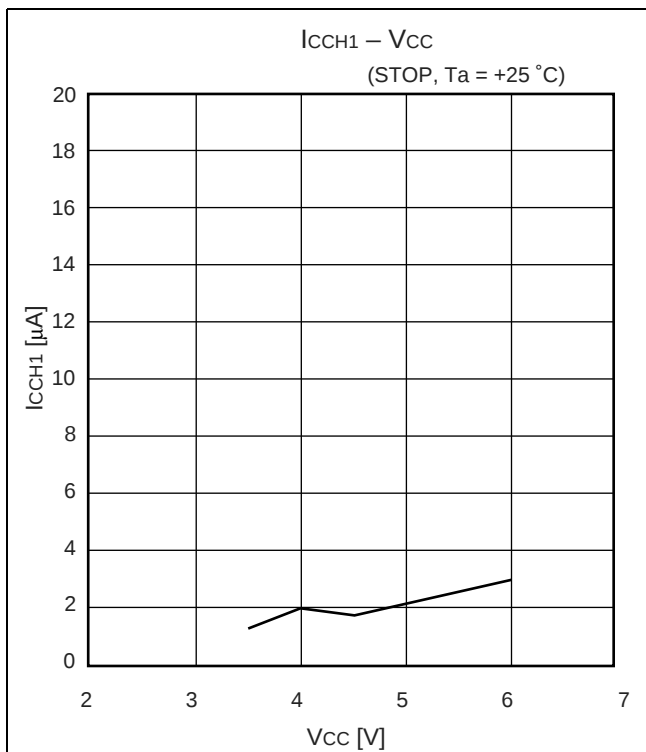
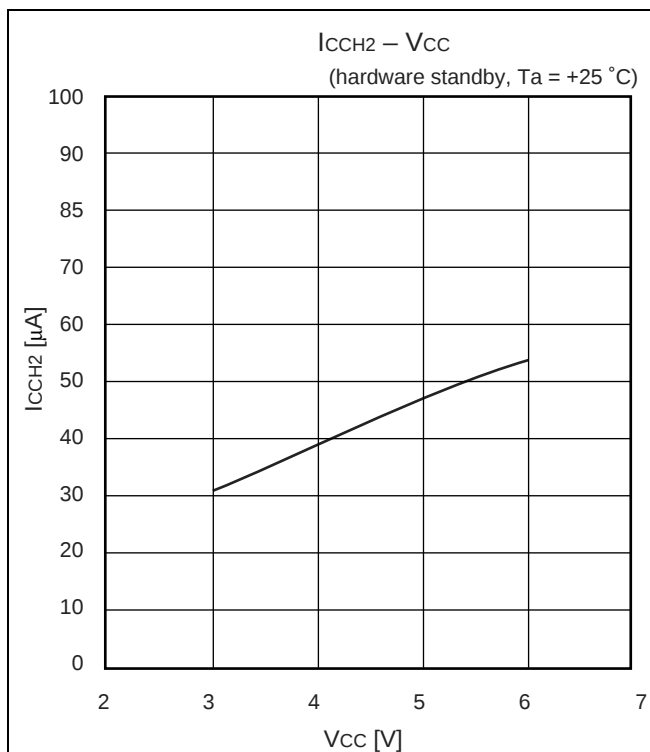
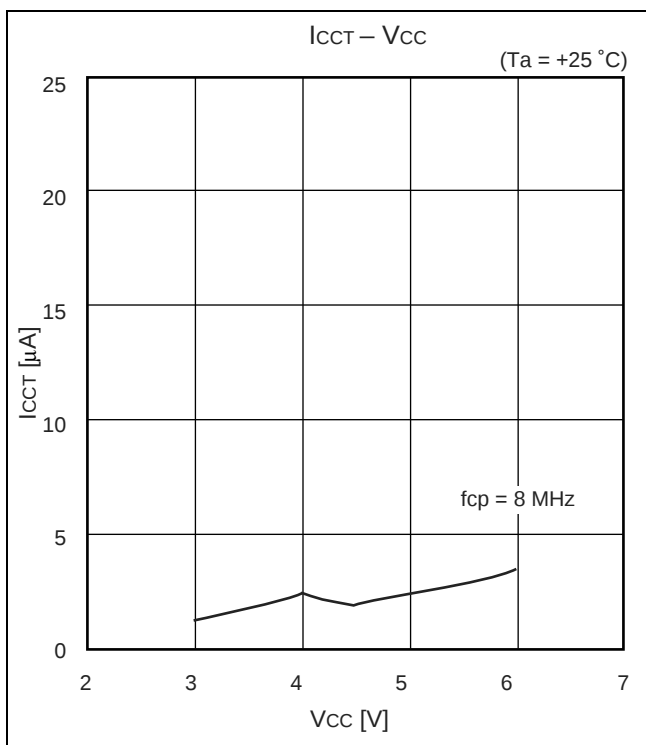
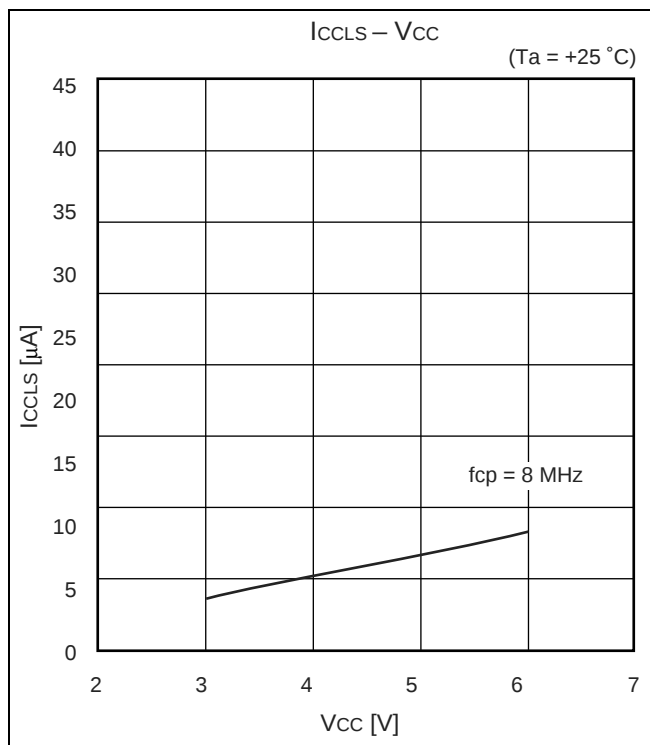
■ “L” level output voltage



■ “H” level input voltage/ “L” level input voltage
(Hysteresis input)



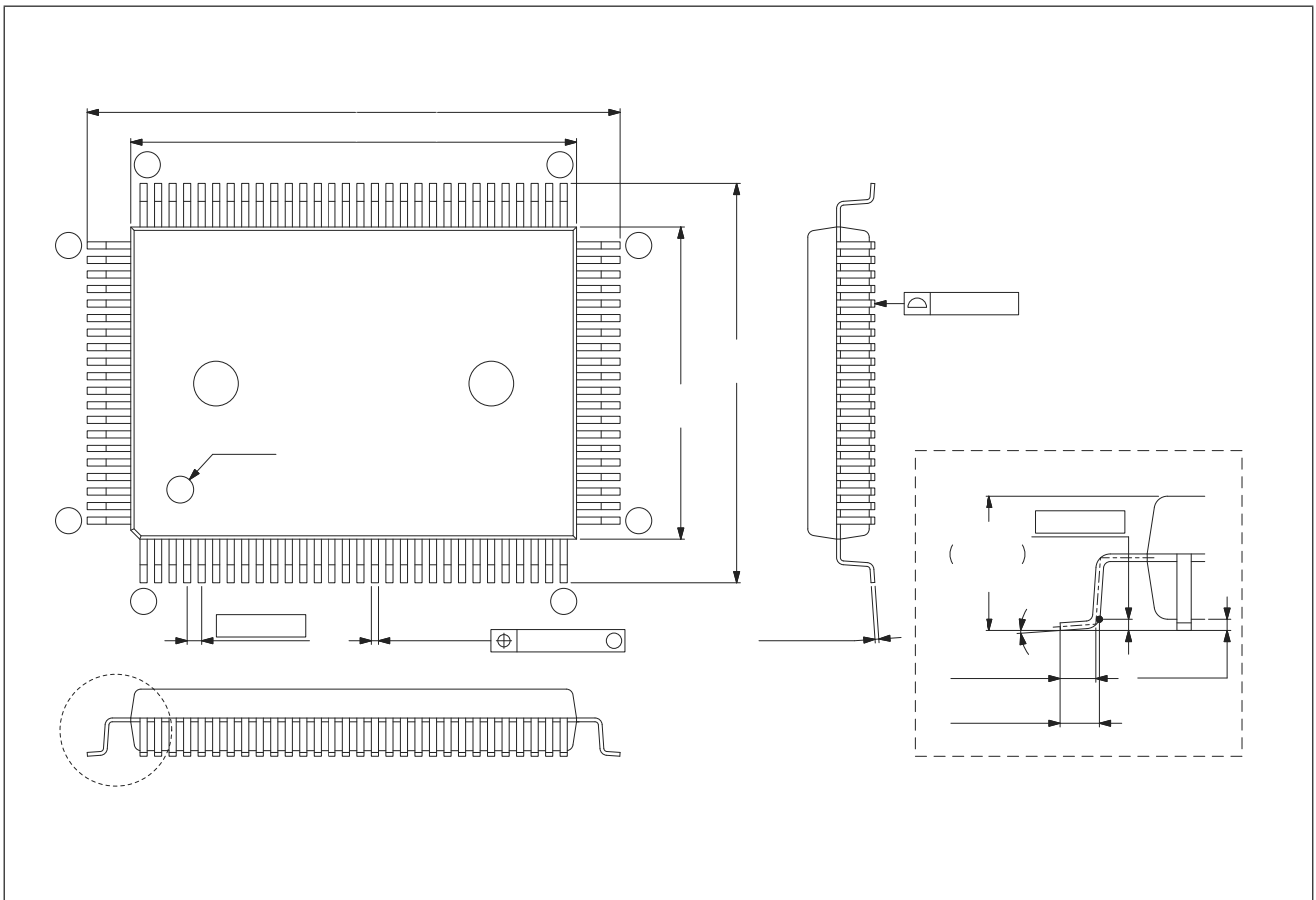
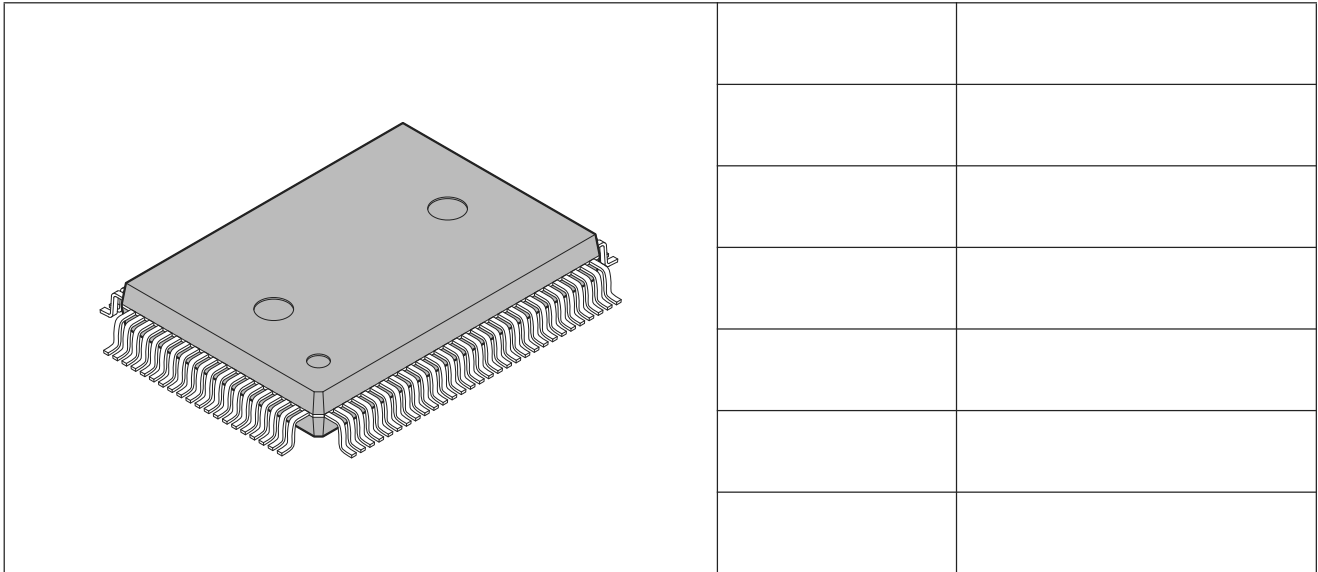




13. Ordering Information

Part number	Package	Remarks
MB90F543GPF MB90F543GSPF MB90F546GPF MB90F546GSPF MB90F548GPF MB90F548GSPF MB90F548GLPF MB90F548GLSPF MB90F549GPF MB90F549GSPF MB90543GPF MB90543GSPF MB90547GPF MB90547GSPF MB90548GPF MB90548GSPF MB90549GPF MB90549GSPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90F543GPMC MB90F543GSPMC MB90F546GPMC MB90F546GSPMC MB90F548GPMC MB90F548GSPMC MB90F548GLPMC MB90F548GLSPMC MB90F549GPMC MB90F549GSPMC MB90543GPMC MB90543GSPMC MB90547GPMC MB90547GSPMC MB90548GPMC MB90548GSPMC MB90549GPMC MB90549GSPMC	100-pin Plastic LQFP (FPT-100P-M20)	

14. Package Dimensions



(Continued)