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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspf-gs-9019

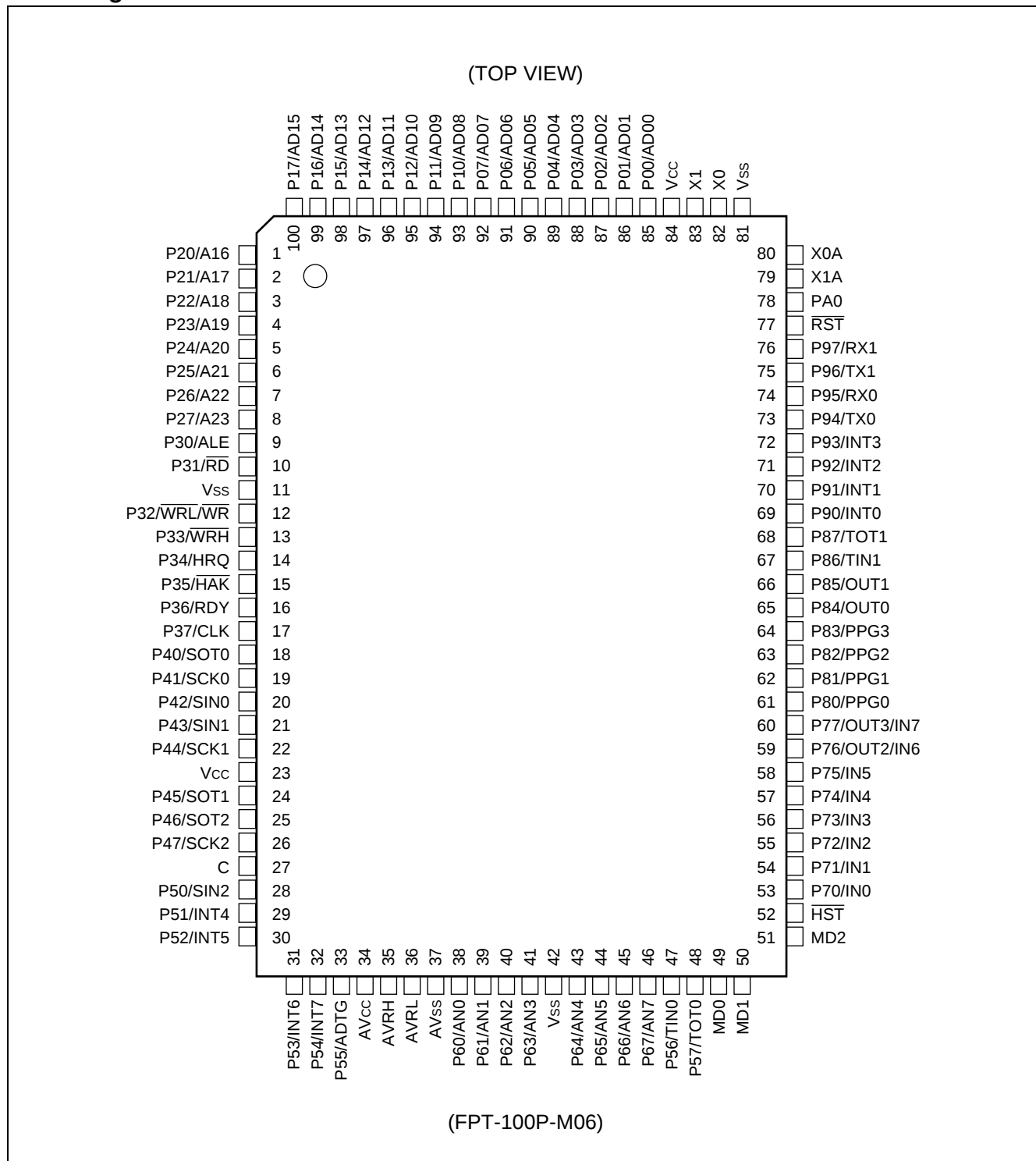
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Features	MB90F543G (S) /F548G (S) MB90F549G (S) /F546G (S) MB90F548GL(S)	MB90543G (S) MB90547G (S) MB90548G (S) MB90549G (S)	MB90V540G
16-bit Reload Timer (2 channels)	Operation clock frequency : $f_{sys}/2^1$, $f_{sys}/2^3$, $f_{sys}/2^5$ (f_{sys} = System clock frequency) Supports External Event Count function Signals an interrupt when overflow		
16-bit Free-run Timer	Supports Timer Clear when a match with Output Compare (Channel 0) Operation clock freq. : $f_{sys}/2^2$, $f_{sys}/2^4$, $f_{sys}/2^6$, $f_{sys}/2^8$ (f_{sys} = System clock freq.)		
16-bit Output Compare (4 channels)	Signals an interrupt when a match with 16-bit Free-run Timer Four 16-bit compare registers A pair of compare registers can be used to generate an output signal		
16-bit Input Capture (8 channels)	Rising edge, falling edge or rising & falling edge sensitive Four 16-bit Capture registers Signals an interrupt upon external event		
8/16-bit Programmable Pulse Generator (4 channels)	Supports 8-bit and 16-bit operation modes Eight 8-bit reload counters Eight 8-bit reload registers for L pulse width Eight 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter 4 output pins Operation clock freq. : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$ or $128 \mu s @ f_{osc} = 4 \text{ MHz}$ (f_{sys} = System clock frequency, f_{osc} = Oscillation clock frequency)		
CAN Interface MB90540G series : 2 channels MB90545G series : 1 channel	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's supports multiple messages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps		
32 kHz Sub-clock	Sub-clock for low power operation		
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive		
External bus interface	External access using the selectable 8-bit or 16-bit bus is enabled (external bus mode.)		
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs and schmitt trigger inputs Bit-wise programmable as input/output or peripheral signal Sub-clock for 32 kHz Sub clock low power operation		
Flash Memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Erase-Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block Block protection by externally programmed voltage		

*1 : If the one clock system is used, equip X0A and X1A with clocks from the tool side.

2. Pin Assignment



3. Pin Description

Pin No.		Pin name	Circuit type	Function
LQFP ²	QFP ¹			
80 81	82 83	X0 X1	A (Oscillation)	High speed crystal oscillator input pins
78	80	X0A	A (Oscillation)	Low speed crystal oscillator input pins. For the one clock system parts, perform external pull-down processing.
77	79	X1A		Low speed crystal oscillator input pins. For the one clock system parts, leave it open.
75	77	$\overline{\text{RST}}$	B	External reset request input pin
50	52	$\overline{\text{HST}}$	C	Hardware standby input pin
83 to 90	85 to 92	P00 to P07	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
91 to 98	93 to 100	P10 to P17	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		AD08 to AD15		I/O pins for 8 higher bits of the external address/data bus. This function is enabled when the external bus is enabled.
99 to 6	1 to 8	P20 to P27	I	General I/O port with programmable pullup. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to "1".
		A16 to A23		8-bit I/O pins for A16 to A23 at the external address/data bus. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to "0".
7	9	P30	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
8	10	P31	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		$\overline{\text{RD}}$		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.
10	12	P32	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the $\overline{\text{WR}}/\overline{\text{WRL}}$ pin output is disabled.
		$\overline{\text{WRL}}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{\text{WR}}/\overline{\text{WRL}}$ pin output are enabled. $\overline{\text{WRL}}$ is write-strobe output pin for the lower 8 bits of the data bus in 16-bit access.
		$\overline{\text{WR}}$		$\overline{\text{WR}}$ is write-strobe output pin for the 8 bits of the data bus in 8-bit access.

(Continued)

Pin No.		Pin name	Circuit type	Function
LQFP ²	QFP ¹			
11	13	P33	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode, external bus 8-bit mode or when WRH pin output is disabled.
		$\overline{\text{WRH}}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the WRH output pin is enabled.
12	14	P34	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.
13	15	P35	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.
14	16	P36	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.
		RDY		Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.
15	17	P37	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the CLK output is disabled.
		CLK		CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled.
16	18	P40	G	General I/O port. This function is enabled when UART0 disables the serial data output.
		SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.
17	19	P41	G	General I/O port. This function is enabled when UART0 disables serial clock output.
		SCK0		Serial clock I/O pin for UART0. This function is enabled when UART0 enables the serial clock output.
18	20	P42	G	General I/O port. This function is always enabled.
		SIN0		Serial data input pin for UART0. Set the corresponding Port Direction Register to input if this function is used.
19	21	P43	G	General I/O port. This function is always enabled.
		SIN1		Serial data input pin for UART1. Set the corresponding Port Direction Register to input if this function is used.

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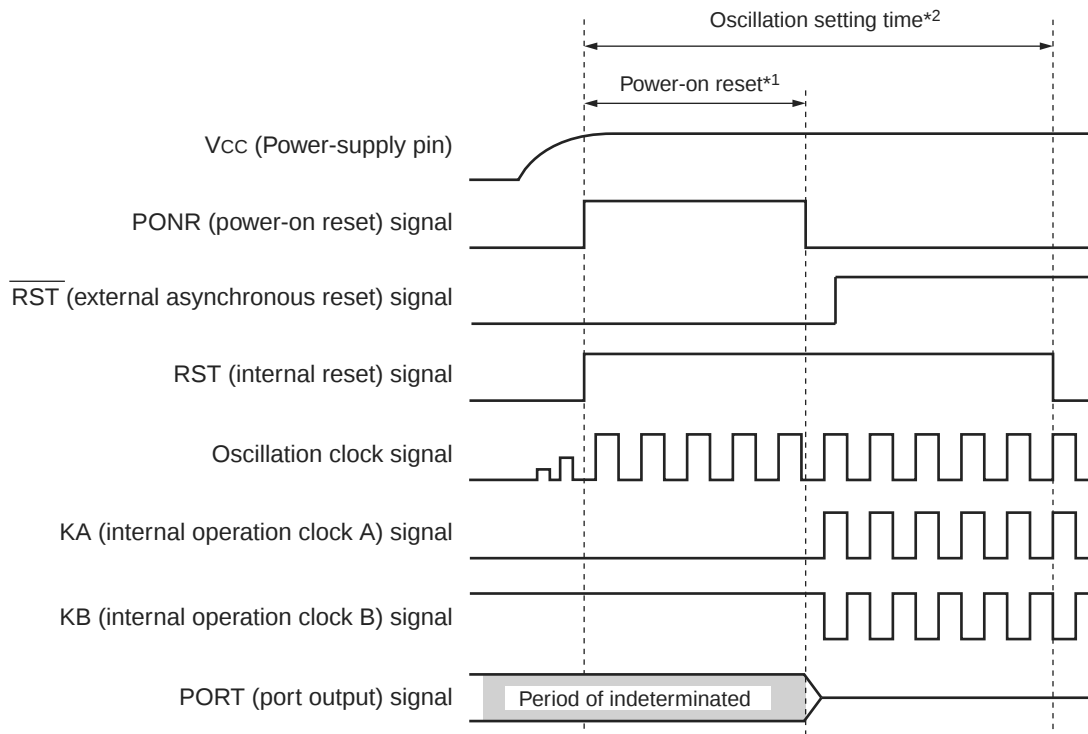
Pin No.		Pin name	Circuit type	Function
LQFP ²	QFP ¹			
20	22	P44	G	General I/O port. This function is enabled when UART1 disables the clock output.
		SCK1		Serial clock pulse I/O pin for UART1. This function is enabled when UART1 enables the serial clock output.
22	24	P45	G	General I/O port. This function is enabled when UART1 disables the serial data output.
		SOT1		Serial data output pin for UART1. This function is enabled when UART1 enables the serial data output.
23	25	P46	G	General I/O port. This function is enabled when the Extended I/O serial interface disables the serial data output.
		SOT2		Serial data output pin for the Extended I/O serial interface. This function is enabled when the Extended I/O serial interface enables the serial data output.
24	26	P47	G	General I/O port. This function is enabled when the Extended I/O serial interface disables the clock output.
		SCK2		Serial clock pulse I/O pin for the Extended I/O serial interface. This function is enabled when the Extended I/O serial interface enables the Serial clock output.
26	28	P50	D	General I/O port. This function is always enabled.
		SIN2		Serial data input pin for the Extended I/O serial interface. Set the corresponding Port Direction Register to input if this function is used.
27 to 30	29 to 32	P51 to P54	D	General I/O port. This function is always enabled.
		INT4 to INT7		External interrupt request input pins for INT4 to INT7. Set the corresponding Port Direction Register to input if this function is used.
31	33	P55	D	General I/O port. This function is always enabled.
		ADTG		Trigger input pin for the A/D converter. Set the corresponding Port Direction Register to input if this function is used.
36 to 39	38 to 41	P60 to P63	E	General I/O port. This function is enabled when the analog input enable register specifies a port.
		AN0 to AN3		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.
41 to 44	43 to 46	P64 to P67	E	General I/O port. The function is enabled when the analog input enable register specifies a port.
		AN4 to AN7		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.
45	47	P56	D	General I/O port. This function is always enabled.
		TIN0		Event input pin for the 16-bit reload timers 0. Set the corresponding Port Direction Register to input if this function is used.

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(12) Indeterminate outputs from ports 0 and 1 (MB90V540G only)

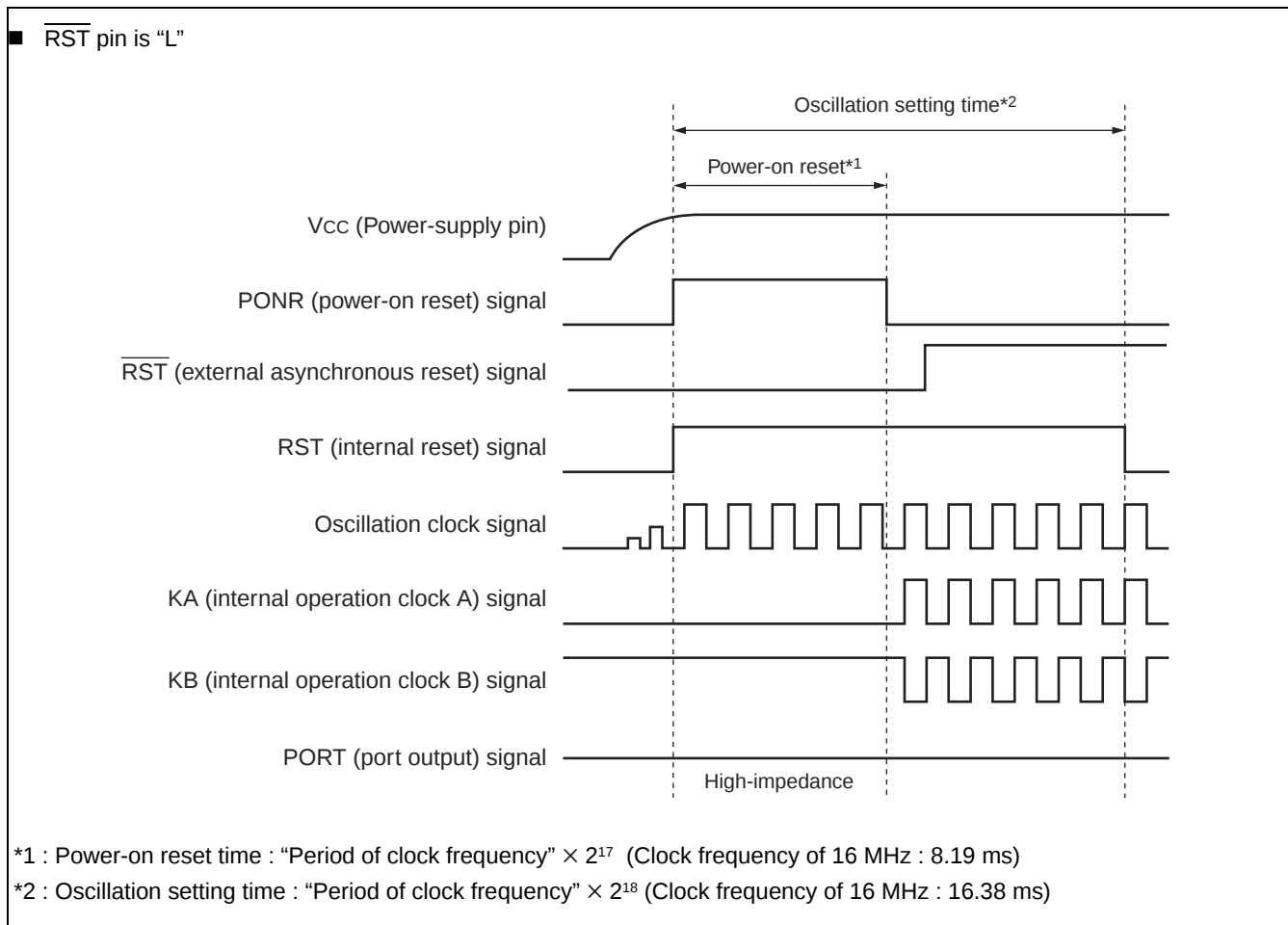
During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

- If $\overline{\text{RST}}$ pin is "H", the outputs become indeterminate.
 - If $\overline{\text{RST}}$ pin is "L", the outputs become high-impedance.
- Pay attention to the port output timing shown as follow.

■ $\overline{\text{RST}}$ pin is "H"


*1 : Power-on reset time : "Period of clock frequency" $\times 2^{17}$ (Clock frequency of 16 MHz : 8.19 ms)

*2 : Oscillation setting time : "Period of clock frequency" $\times 2^{18}$ (Clock frequency of 16 MHz : 16.38 ms)



(13) Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(14) Directions of "DIV A, Ri" and "DIVW A, RWi" instructions

In the Signed multiplication and division instructions ("DIV A, Ri" and "DIVW A, RWi"), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in "00H".

If the values of the corresponding bank registers (DTB, ADB, USB, SSB) are set to other than "00H", the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

(15) Using REALOS

The use of EI²OS is not possible with the REALOS real time operating system.

(16) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

Address	Register	Abbreviation	Access	Resource name	Initial value
24 _H	Serial mode register 1	SMR1	R/W	UART1	0 0 0 0 0 0 0 0 _B
25 _H	Serial control register 1	SCR1	R/W		0 0 0 0 0 1 0 0 _B
26 _H	Serial input data register 1/ Serial output data register 1	SIDR1/SODR1	R/W		XXXXXXXX _B
27 _H	Serial status register 1	SSR1	R/W		0 0 0 0 1 _ 0 0 _B
28 _H	UART1 prescaler control register	CDCR	R/W		0 _ _ _ 1 1 1 1 _B
29 _H	Serial Edge select register	SES1	R/W		_ _ _ _ _ 0 _B
2A _H	Prohibited				
2B _H	Serial I/O prescaler	SCDCR	R/W	Extended I/O Serial Interface	0 _ _ _ 1 1 1 1 _B
2C _H	Serial mode control register	SMCS	R/W		_ _ _ _ 0 0 0 0 _B
2D _H	Serial mode control register	SMCS	R/W		0 0 0 0 0 0 1 0 _B
2E _H	Serial data register	SDR	R/W		XXXXXXXX _B
2F _H	Serial Edge select register	SES2	R/W		_ _ _ _ _ 0 _B
30 _H	External interrupt enable register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0 _B
31 _H	External interrupt request register	EIRR	R/W		XXXXXXXX _B
32 _H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0 _B
33 _H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0 _B
34 _H	A/D control status register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0 _B
35 _H	A/D control status register 1	ADCS1	R/W		0 0 0 0 0 0 0 0 _B
36 _H	A/D data register 0	ADCR0	R		XXXXXXXX _B
37 _H	A/D data register 1	ADCR1	R/W		0 0 0 0 1 _ XX _B
38 _H	PPG0 operation mode control register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 0 _ _ 1 _B
39 _H	PPG1 operation mode control register	PPGC1	R/W		0 _ 0 0 0 0 0 1 _B
3A _H	PPG0/1 clock selection register	PPG01	R/W		0 0 0 0 0 0 _ _ _B
3B _H	Prohibited				
3C _H	PPG2 operation mode control register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 0 _ _ 1 _B
3D _H	PPG3 operation mode control register	PPGC3	R/W		0 _ 0 0 0 0 0 1 _B
3E _H	PPG2/3 Clock Selection Register	PPG23	R/W		0 0 0 0 0 0 _ _ _B
3F _H	Prohibited				
40 _H	PPG4 operation mode control register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 0 _ _ 1 _B
41 _H	PPG5 operation mode control register	PPGC5	R/W		0 _ 0 0 0 0 0 1 _B
42 _H	PPG4/5 clock selection register	PPG45	R/W		0 0 0 0 0 0 _ _ _B
43 _H	Prohibited				
44 _H	PPG6 operation mode control register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 0 _ _ 1 _B
45 _H	PPG7 operation mode control register	PPGC7	R/W		0 _ 0 0 0 0 0 1 _B
46 _H	PPG6/7 clock selection register	PPG67	R/W		0 0 0 0 0 0 _ _ _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
A2 _H to A4 _H	Prohibited				
A5 _H	Automatic ready function select register	ARSR	W	External Memory Access	0 0 1 1 _ _ 0 0 _B
A6 _H	External address output control register	HACR	W		0 0 0 0 0 0 0 0 _B
A7 _H	Bus control signal selection register	ECSR	W		0 0 0 0 0 0 0 _ _B
A8 _H	Watchdog Timer control register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1 _B
A9 _H	Time Base Timer Control register	TBTC	R/W	Time Base Timer	1 - - 0 0 1 0 0 _B
AA _H	Watch timer control register	WTC	R/W	Watch Timer	1 X 0 0 0 0 0 0 _B
AB _H to AD _H	Prohibited				
AE _H	Flash memory control status register (Flash only, otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0 _B
AF _H	Prohibited				
B0 _H	Interrupt control register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1 _B
B1 _H	Interrupt control register 01	ICR01	R/W		0 0 0 0 0 1 1 1 _B
B2 _H	Interrupt control register 02	ICR02	R/W		0 0 0 0 0 1 1 1 _B
B3 _H	Interrupt control register 03	ICR03	R/W		0 0 0 0 0 1 1 1 _B
B4 _H	Interrupt control register 04	ICR04	R/W		0 0 0 0 0 1 1 1 _B
B5 _H	Interrupt control register 05	ICR05	R/W		0 0 0 0 0 1 1 1 _B
B6 _H	Interrupt control register 06	ICR06	R/W		0 0 0 0 0 1 1 1 _B
B7 _H	Interrupt control register 07	ICR07	R/W		0 0 0 0 0 1 1 1 _B
B8 _H	Interrupt control register 08	ICR08	R/W		0 0 0 0 0 1 1 1 _B
B9 _H	Interrupt control register 09	ICR09	R/W		0 0 0 0 0 1 1 1 _B
BA _H	Interrupt control register 10	ICR10	R/W		0 0 0 0 0 1 1 1 _B
BB _H	Interrupt control register 11	ICR11	R/W		0 0 0 0 0 1 1 1 _B
BC _H	Interrupt control register 12	ICR12	R/W		0 0 0 0 0 1 1 1 _B
BD _H	Interrupt control register 13	ICR13	R/W		0 0 0 0 0 1 1 1 _B
BE _H	Interrupt control register 14	ICR14	R/W		0 0 0 0 0 1 1 1 _B
BF _H	Interrupt control register 15	ICR15	R/W		0 0 0 0 0 1 1 1 _B
C0 _H to FF _H	External				

Address	Register	Abbreviation	Access	Resource name	Initial value
1FF0 _H	Program address detection register 0	PADR0	R/W	Address Match Detection Function	XXXXXXXX _B
1FF1 _H	Program address detection register 0	PADR0	R/W		XXXXXXXX _B
1FF2 _H	Program address detection register 0	PADR0	R/W		XXXXXXXX _B
1FF3 _H	Program address detection register 1	PADR1	R/W		XXXXXXXX _B
1FF4 _H	Program address detection register 1	PADR1	R/W		XXXXXXXX _B
1FF5 _H	Program address detection register 1	PADR1	R/W		XXXXXXXX _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
3900 _H	Reload L	PRLLO	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX _B
3901 _H	Reload H	PRLH0	R/W		XXXXXXXX _B
3902 _H	Reload L	PRLLO	R/W		XXXXXXXX _B
3903 _H	Reload H	PRLH1	R/W		XXXXXXXX _B
3904 _H	Reload L	PRLLO	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX _B
3905 _H	Reload H	PRLH2	R/W		XXXXXXXX _B
3906 _H	Reload L	PRLLO	R/W		XXXXXXXX _B
3907 _H	Reload H	PRLH3	R/W		XXXXXXXX _B
3908 _H	Reload L	PRLLO	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX _B
3909 _H	Reload H	PRLH4	R/W		XXXXXXXX _B
390A _H	Reload L	PRLLO	R/W		XXXXXXXX _B
390B _H	Reload H	PRLH5	R/W		XXXXXXXX _B
390C _H	Reload L	PRLLO	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX _B
390D _H	Reload H	PRLH6	R/W		XXXXXXXX _B
390E _H	Reload L	PRLLO	R/W		XXXXXXXX _B
390F _H	Reload H	PRLH7	R/W		XXXXXXXX _B
3910 _H to 3917 _H	Reserved				
3918 _H	Input Capture Register 0	IPCP0	R	Input Capture 0/1	XXXXXXXX _B
3919 _H	Input Capture Register 0	IPCP0	R		XXXXXXXX _B
391A _H	Input Capture Register 1	IPCP1	R		XXXXXXXX _B
391B _H	Input Capture Register 1	IPCP1	R		XXXXXXXX _B
391C _H	Input Capture Register 2	IPCP2	R	Input Capture 2/3	XXXXXXXX _B
391D _H	Input Capture Register 2	IPCP2	R		XXXXXXXX _B
391E _H	Input Capture Register 3	IPCP3	R		XXXXXXXX _B
391F _H	Input Capture Register 3	IPCP3	R		XXXXXXXX _B
3920 _H	Input Capture Register 4	IPCP4	R	Input Capture 4/5	XXXXXXXX _B
3921 _H	Input Capture Register 4	IPCP4	R		XXXXXXXX _B
3922 _H	Input Capture Register 5	IPCP5	R		XXXXXXXX _B
3923 _H	Input Capture Register 5	IPCP5	R		XXXXXXXX _B
3924 _H	Input Capture Register 6	IPCP6	R	Input Capture 6/7	XXXXXXXX _B
3925 _H	Input Capture Register 6	IPCP6	R		XXXXXXXX _B
3926 _H	Input Capture Register 7	IPCP7	R		XXXXXXXX _B
3927 _H	Input Capture Register 7	IPCP7	R		XXXXXXXX _B

(Continued)

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Units	Remarks
		Min	Max		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *1
	$AVRH, AVRL$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH/AVRL, AVRH \geq AVRL$ *1
Input voltage	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Output voltage	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Maximum clamp current	I_{CLAMP}	- 2.0	+ 2.0	mA	*6
Total maximum clamp current	$\Sigma I_{CLAMP} $	—	20	mA	*6
"L" level max output current	I_{OL}	—	15	mA	*3
"L" level avg. output current	I_{OLAV}	—	4	mA	*4
"L" level max overall output current	ΣI_{OL}	—	100	mA	
"L" level avg. overall output current	ΣI_{OLAV}	—	50	mA	*5
"H" level max output current	I_{OH}	—	-15	mA	*3
"H" level avg. output current	I_{OHAV}	—	-4	mA	*4
"H" level max overall output current	ΣI_{OH}	—	-100	mA	
"H" level avg. overall output current	ΣI_{OHAV}	—	-50	mA	*5
Power consumption	P_D	—	500	mW	Flash device
		—	400	mW	MASK ROM
Operating temperature	T_A	-40	+105	°C	
Storage temperature	T_{STG}	-55	+150	°C	

*1 : AV_{CC} , $AVRH$, $AVRL$ should not exceed V_{CC} . Also, $AVRH$, $AVRL$ should not exceed AV_{CC} , and $AVRL$ does not exceed $AVRH$.

*2 : V_I and V_O should not exceed $V_{CC} + 0.3\text{ V}$. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supercedes the V_I rating.

*3 : The maximum output current is a peak value for a corresponding pin.

*4 : Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5 : Total average current is an average current value observed for a 100 ms period for all corresponding pins.

*6 :

- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The + B signal should always be applied with a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the + B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a + B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- Care must be taken not to leave the + B input pin open.

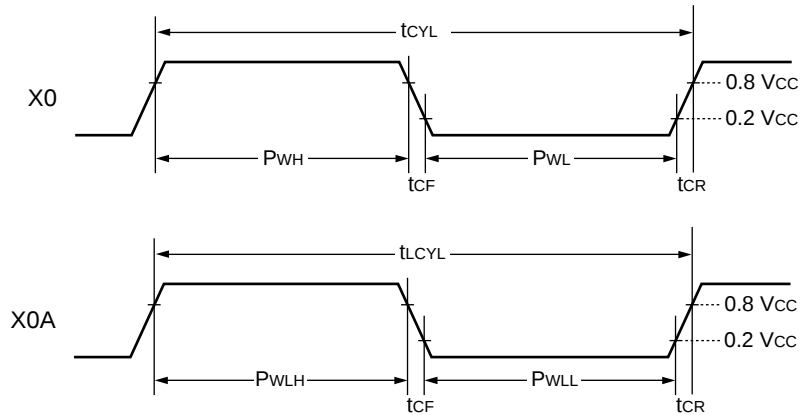
(Continued)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

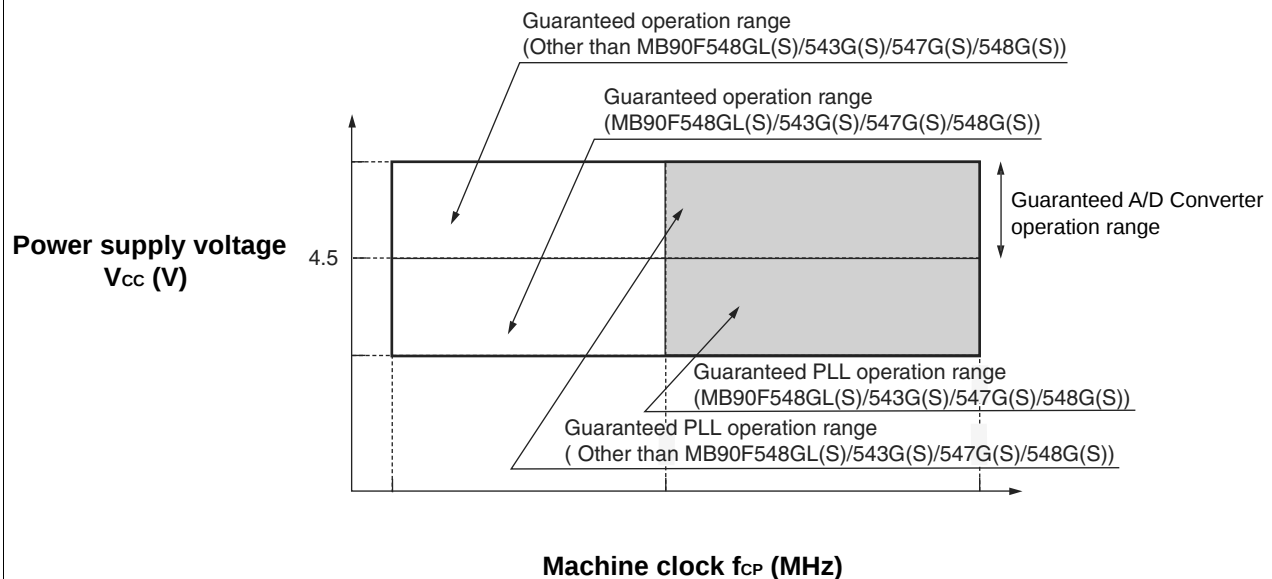
(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	No multiplier When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			62.5	—	125	ns	PLL multiplied by 1 When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			125	—	250	ns	PLL multiplied by 2 When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			187.5	—	333	ns	PLL multiplied by 3 When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			250	—	333	ns	PLL multiplied by 4 When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			200	—	333	ns	When using an oscillator circuit $V_{CC} < 4.5\text{ V}$ (MB90F548GL(S)/543G(S)/ 547G(S)/548G(S))
			62.5	—	333	ns	No multiplier When using an external clock
			62.5	—	125	ns	PLL multiplied by 1 When using an external clock
			125	—	250	ns	PLL multiplied by 2 When using an external clock
			187.5	—	333	ns	PLL multiplied by 3 When using an external clock
			250	—	333	ns	PLL multiplied by 4 When using an external clock
	t_{LCYL}	X0A, X1A	—	30.5	—	μs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WLH}, P_{WLL}	X0A	—	15.2	—	μs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using an external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	When using main clock
	f_{LCP}	—	—	8.192	—	kHz	When using sub-clock
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	When using main clock
	t_{LCP}	—	—	122.1	—	μs	When using sub-clock

■ Clock Timing



■ Guaranteed PLL operation range

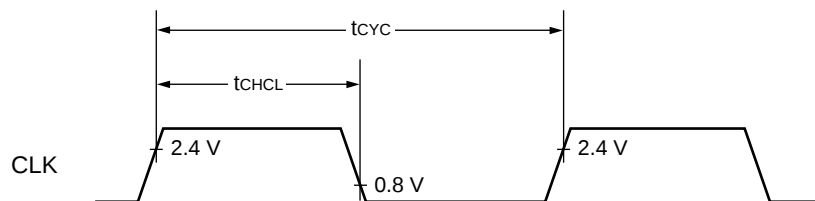


11.4.2 Clock Output Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	$V_{CC} = 5\text{ V} \pm 10\%$	62.5	—	ns	
CLK $\uparrow$ → CLK $\downarrow$	t_{CHCL}			20	—	ns	



11.4.3 Reset and Hardware Standby Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

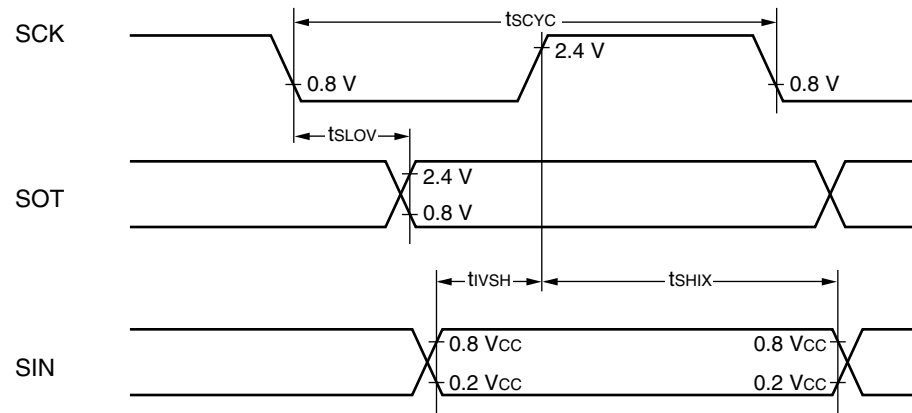
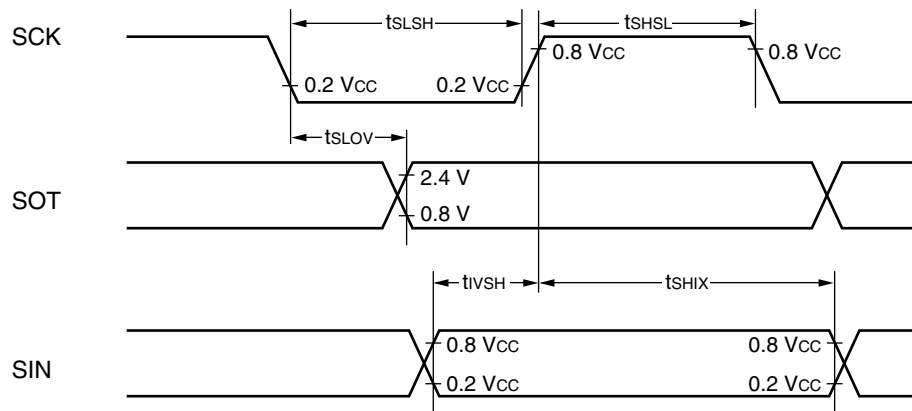
(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value		Units	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	4 t_{CP}	—	ns	Under normal operation
			Oscillation time of oscillator + 4 t_{CP}	—	ms	In stop mode
			100	—	μs	In pseudo timer mode (MB90543G (S) /547G (S) /548G (S))
			4 t_{CP}	—	ns	In pseudo timer mode (Other than MB90543G (S) /547G (S) /548G (S))
			2 t_{LCP}	—	μs	In sub-clock mode, sub-sleep mode, timer mode
Hardware standby input time	t_{HSTL}	HST	4 t_{CP}	—	ns	Under normal operation

Note : “ t_{cp} ” represents one cycle time of the machine clock.

Oscillation time of oscillator is time that amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ns.

Any reset can not fully initialize the Flash Memory if it is performing the automatic algorithm.

Internal Shift Clock Mode

External Shift Clock Mode


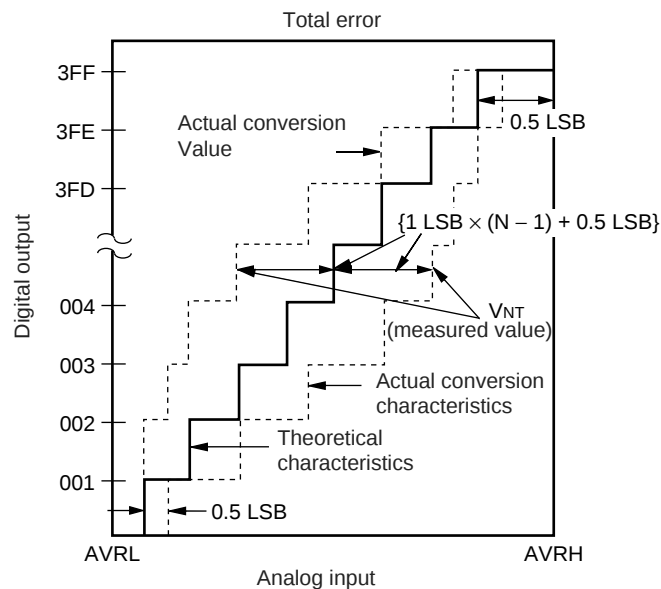
11.5.2 A/D Converter Glossary

Resolution : Analog changes that are identifiable with the A/D converter

Linearity error : The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ↔ "11 1111 1111") from actual conversion characteristics

Differential linearity error : The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error : The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1 \text{ LSB} = (\text{Theoretical value}) \frac{AVRH - AVRL}{1024} [\text{V}]$$

$$V_{OT} (\text{Theoretical value}) = AVRL + 0.5 \text{ LSB} [\text{V}]$$

$$V_{FST} (\text{Theoretical value}) = AVRH - 1.5 \text{ LSB} [\text{V}]$$

$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} [\text{LSB}]$$

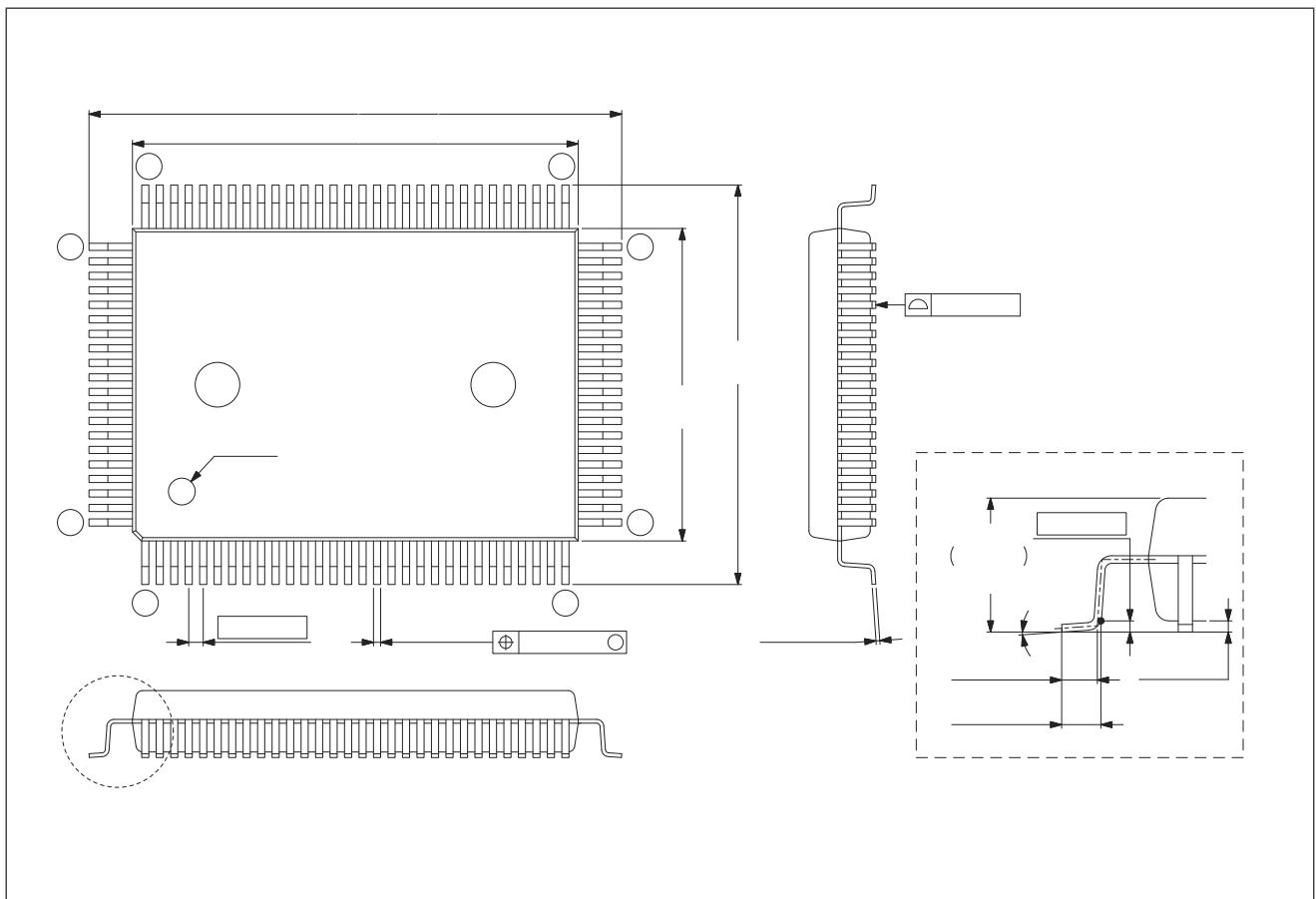
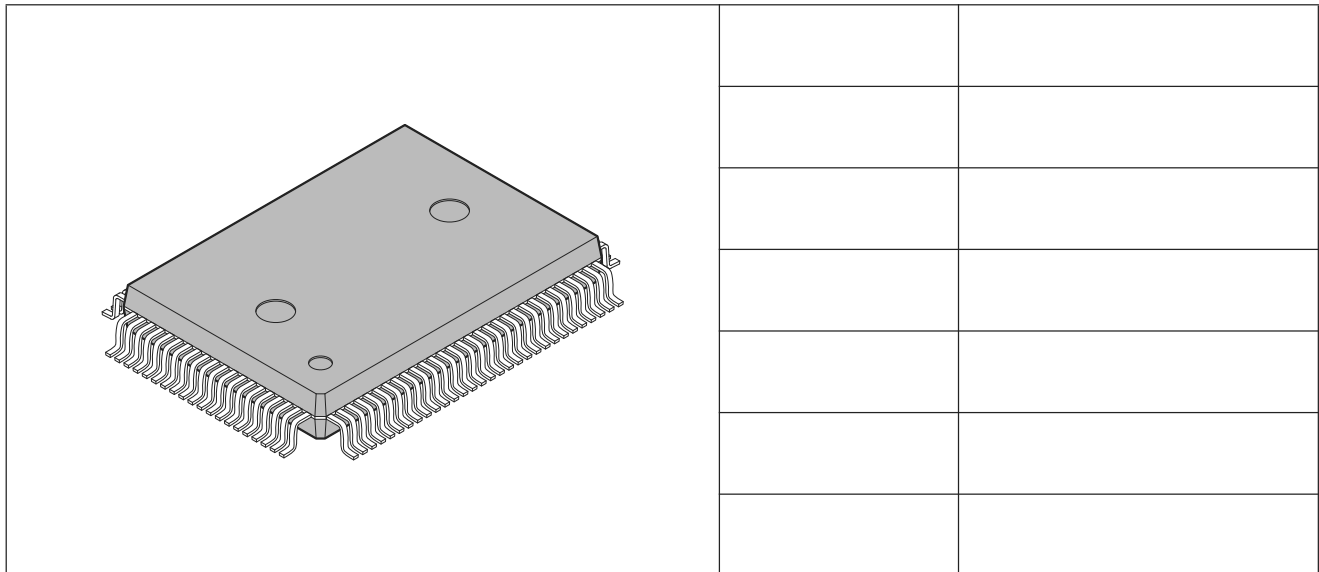
V_{NT} : Voltage at a transition of digital output from $(N - 1)$ to N

(Continued)

11.6 Flash Memory Program/Erase Characteristics

Parameter	Condition	Value			Units	Remarks	
		Min	Typ	Max			
Sector erase time	T _A = + 25 °C V _{CC} = 5.0 V	—	1	15	s	Excludes 00H programming prior erasure	
Chip erase time		—	5	—	s	MB90F543G (S) /F548G (S) /F548GL (S)	Excludes 00H programming prior erasure
			7	—	s	MB90F549G (S) /F546G (S)	
Word (16 bit width) programming time		—	16	3,600	μs	Excludes system-level overhead	
Erase/Program cycle	—	10,000	—	—	cycle		

14. Package Dimensions



(Continued)

(Continued)

