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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

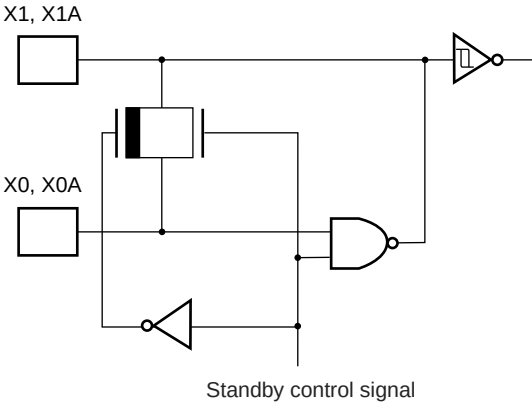
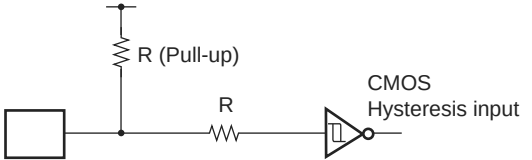
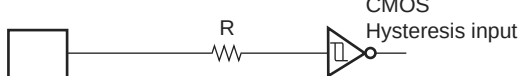
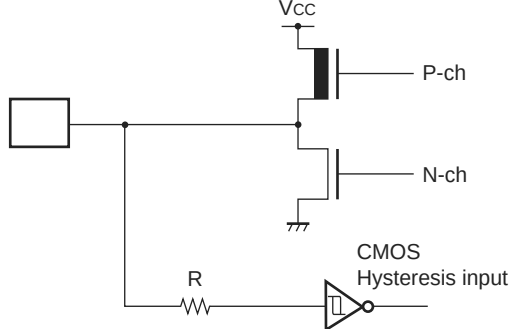
Details

Product Status	Active
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspf-gs-9020

Pin No.		Pin name	Circuit type	Function
LQFP ²	QFP ¹			
11	13	P33	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode, external bus 8-bit mode or when WRH pin output is disabled.
		$\overline{\text{WRH}}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the WRH output pin is enabled.
12	14	P34	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.
13	15	P35	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.
14	16	P36	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.
		RDY		Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.
15	17	P37	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the CLK output is disabled.
		CLK		CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled.
16	18	P40	G	General I/O port. This function is enabled when UART0 disables the serial data output.
		SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.
17	19	P41	G	General I/O port. This function is enabled when UART0 disables serial clock output.
		SCK0		Serial clock I/O pin for UART0. This function is enabled when UART0 enables the serial clock output.
18	20	P42	G	General I/O port. This function is always enabled.
		SIN0		Serial data input pin for UART0. Set the corresponding Port Direction Register to input if this function is used.
19	21	P43	G	General I/O port. This function is always enabled.
		SIN1		Serial data input pin for UART1. Set the corresponding Port Direction Register to input if this function is used.

(Continued)

4. I/O Circuit Type

Circuit type	Diagram	Remarks
A	 Standby control signal	■ High-speed oscillation feedback resistor : 1 MΩ approx. ■ Low-speed oscillation feedback resistor: 10 MΩ approx.
B	 R (Pull-up) CMOS Hysteresis input	■ CMOS Hysteresis input ■ Pull-up resistor : 50 kΩ approx.
C	 CMOS Hysteresis input	■ CMOS Hysteresis input
D	 Vcc P-ch N-ch CMOS Hysteresis input R	■ CMOS level output ■ CMOS Hysteresis input

(Continued)

(6) Pull-up/down resistors

The MB90540G/545G Series does not support internal pull-up/down resistors (except Port0 – Port3 : pull-up resistors) . Use external components where needed.

(7) Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via the shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuits do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation.

(8) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC} , AV_{RH} , AV_{RL}) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}) .

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AV_{RH} or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable) .

(9) Connection of Unused Pins of A/D Converter

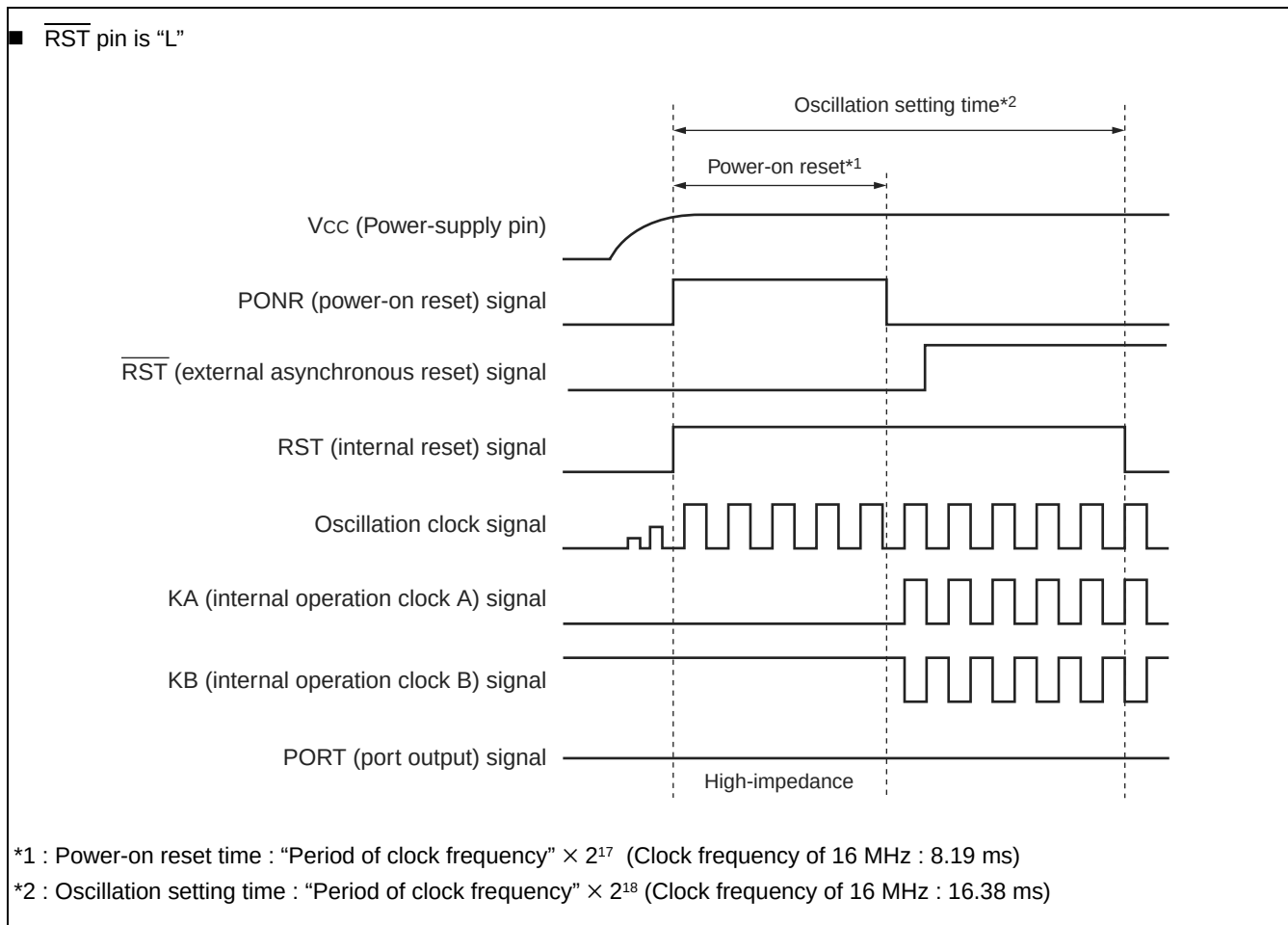
Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AV_{RH} = V_{SS}$.

(10) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

(11) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μ s or more (0.2 V to 2.7 V) .



(13) Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(14) Directions of "DIV A, Ri" and "DIVW A, RWi" instructions

In the Signed multiplication and division instructions ("DIV A, Ri" and "DIVW A, RWi"), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in "00H".

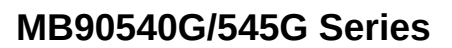
If the values of the corresponding bank registers (DTB, ADB, USB, SSB) are set to other than "00H", the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

(15) Using REALOS

The use of EI²OS is not possible with the REALOS real time operating system.

(16) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.



Document Number: 002- 07696 Rev. *A

Address	Register	Abbreviation	Access	Resource name	Initial value
24 _H	Serial mode register 1	SMR1	R/W	UART1	0 0 0 0 0 0 0 0 _B
25 _H	Serial control register 1	SCR1	R/W		0 0 0 0 0 1 0 0 _B
26 _H	Serial input data register 1/ Serial output data register 1	SIDR1/SODR1	R/W		XXXXXXXX _B
27 _H	Serial status register 1	SSR1	R/W		0 0 0 0 1 _ 0 0 _B
28 _H	UART1 prescaler control register	CDCR	R/W		0 _ _ 1 1 1 1 _B
29 _H	Serial Edge select register	SES1	R/W		_ _ _ _ _ 0 _B
2A _H	Prohibited				
2B _H	Serial I/O prescaler	SCDCR	R/W	Extended I/O Serial Interface	0 _ _ 1 1 1 1 _B
2C _H	Serial mode control register	SMCS	R/W		_ _ _ 0 0 0 0 _B
2D _H	Serial mode control register	SMCS	R/W		0 0 0 0 0 1 0 _B
2E _H	Serial data register	SDR	R/W		XXXXXXXX _B
2F _H	Serial Edge select register	SES2	R/W		_ _ _ _ _ 0 _B
30 _H	External interrupt enable register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0 _B
31 _H	External interrupt request register	EIRR	R/W		XXXXXXXX _B
32 _H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0 _B
33 _H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0 _B
34 _H	A/D control status register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0 _B
35 _H	A/D control status register 1	ADCS1	R/W		0 0 0 0 0 0 0 0 _B
36 _H	A/D data register 0	ADCR0	R		XXXXXXXX _B
37 _H	A/D data register 1	ADCR1	R/W		0 0 0 0 1 _ XX _B
38 _H	PPG0 operation mode control register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 _ _ 1 _B
39 _H	PPG1 operation mode control register	PPGC1	R/W		0 _ 0 0 0 0 1 _B
3A _H	PPG0/1 clock selection register	PPG01	R/W		0 0 0 0 0 _ _ _B
3B _H	Prohibited				
3C _H	PPG2 operation mode control register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 _ _ 1 _B
3D _H	PPG3 operation mode control register	PPGC3	R/W		0 _ 0 0 0 0 1 _B
3E _H	PPG2/3 Clock Selection Register	PPG23	R/W		0 0 0 0 0 _ _ _B
3F _H	Prohibited				
40 _H	PPG4 operation mode control register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 _ _ 1 _B
41 _H	PPG5 operation mode control register	PPGC5	R/W		0 _ 0 0 0 0 1 _B
42 _H	PPG4/5 clock selection register	PPG45	R/W		0 0 0 0 0 _ _ _B
43 _H	Prohibited				
44 _H	PPG6 operation mode control register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 _ _ 1 _B
45 _H	PPG7 operation mode control register	PPGC7	R/W		0 _ 0 0 0 0 1 _B
46 _H	PPG6/7 clock selection register	PPG67	R/W		0 0 0 0 0 _ _ _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
A2 _H to A4 _H	Prohibited				
A5 _H	Automatic ready function select register	ARSR	W	External Memory Access	0 0 1 1 _ _ 0 0 _B
A6 _H	External address output control register	HACR	W		0 0 0 0 0 0 0 0 _B
A7 _H	Bus control signal selection register	ECSR	W		0 0 0 0 0 0 0 _ _B
A8 _H	Watchdog Timer control register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1 _B
A9 _H	Time Base Timer Control register	TBTC	R/W	Time Base Timer	1 - - 0 0 1 0 0 _B
AA _H	Watch timer control register	WTC	R/W	Watch Timer	1 X 0 0 0 0 0 0 _B
AB _H to AD _H	Prohibited				
AE _H	Flash memory control status register (Flash only, otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0 _B
AF _H	Prohibited				
B0 _H	Interrupt control register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1 _B
B1 _H	Interrupt control register 01	ICR01	R/W		0 0 0 0 0 1 1 1 _B
B2 _H	Interrupt control register 02	ICR02	R/W		0 0 0 0 0 1 1 1 _B
B3 _H	Interrupt control register 03	ICR03	R/W		0 0 0 0 0 1 1 1 _B
B4 _H	Interrupt control register 04	ICR04	R/W		0 0 0 0 0 1 1 1 _B
B5 _H	Interrupt control register 05	ICR05	R/W		0 0 0 0 0 1 1 1 _B
B6 _H	Interrupt control register 06	ICR06	R/W		0 0 0 0 0 1 1 1 _B
B7 _H	Interrupt control register 07	ICR07	R/W		0 0 0 0 0 1 1 1 _B
B8 _H	Interrupt control register 08	ICR08	R/W		0 0 0 0 0 1 1 1 _B
B9 _H	Interrupt control register 09	ICR09	R/W		0 0 0 0 0 1 1 1 _B
BA _H	Interrupt control register 10	ICR10	R/W		0 0 0 0 0 1 1 1 _B
BB _H	Interrupt control register 11	ICR11	R/W		0 0 0 0 0 1 1 1 _B
BC _H	Interrupt control register 12	ICR12	R/W		0 0 0 0 0 1 1 1 _B
BD _H	Interrupt control register 13	ICR13	R/W		0 0 0 0 0 1 1 1 _B
BE _H	Interrupt control register 14	ICR14	R/W		0 0 0 0 0 1 1 1 _B
BF _H	Interrupt control register 15	ICR15	R/W		0 0 0 0 0 1 1 1 _B
C0 _H to FF _H	External				

Address	Register	Abbreviation	Access	Resource name	Initial value
1FF0 _H	Program address detection register 0	PADR0	R/W	Address Match Detection Function	XXXXXXXX _B
1FF1 _H	Program address detection register 0	PADR0	R/W		XXXXXXXX _B
1FF2 _H	Program address detection register 0	PADR0	R/W		XXXXXXXX _B
1FF3 _H	Program address detection register 1	PADR1	R/W		XXXXXXXX _B
1FF4 _H	Program address detection register 1	PADR1	R/W		XXXXXXXX _B
1FF5 _H	Program address detection register 1	PADR1	R/W		XXXXXXXX _B

(Continued)

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003B00 _H	003D00 _H	Control status register	CSR	R/W, R	00---000 0---0-1 _B
003B01 _H	003D01 _H				
003B02 _H	003D02 _H	Last event indicator register	LEIR	R/W	----- 000-0000 _B
003B03 _H	003D03 _H				
003B04 _H	003D04 _H	Receive/transmit error counter register	RTEC	R	00000000 00000000 _B
003B05 _H	003D05 _H				
003B06 _H	003D06 _H	Bit timing register	BTR	R/W	-1111111 11111111 _B
003B07 _H	003D07 _H				
003B08 _H	003D08 _H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXX _B
003B09 _H	003D09 _H				
003B0A _H	003D0A _H	Transmit RTR register	TRTRR	R/W	00000000 00000000 _B
003B0B _H	003D0B _H				
003B0C _H	003D0C _H	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXX _B
003B0D _H	003D0D _H				
003B0E _H	003D0E _H	Transmit request enable register	TIER	R/W	00000000 00000000 _B
003B0F _H	003D0F _H				
003B10 _H	003D10 _H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXX _B
003B11 _H	003D11 _H				XXXXXXXX XXXXXXXX _B
003B12 _H	003D12 _H				
003B13 _H	003D13 _H				
003B14 _H	003D14 _H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXX _B
003B15 _H	003D15 _H				XXXXXX--- XXXXXXXX _B
003B16 _H	003D16 _H				
003B17 _H	003D17 _H				
003B18 _H	003D18 _H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXX _B
003B19 _H	003D19 _H				XXXXXX--- XXXXXXXX _B
003B1A _H	003D1A _H				
003B1B _H	003D1B _H				

List of Message Buffers (ID Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A00 _H to 003A1F _H	003C00 _H to 003C1F _H	General-purpose RAM	—	R/W	XXXXXXXX _B to XXXXXXXX _B
003A20 _H	003C20 _H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXX _B
003A21 _H	003C21 _H				XXXXXX--- XXXXXXXX _B
003A22 _H	003C22 _H				
003A23 _H	003C23 _H				

(Continued)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A3C _H	003C3C _H	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX _B
003A3D _H	003C3D _H				
003A3E _H	003C3E _H				XXXXX--- XXXXXXXX _B
003A3F _H	003C3F _H				
003A40 _H	003C40 _H	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX _B
003A41 _H	003C41 _H				
003A42 _H	003C42 _H				XXXXX--- XXXXXXXX _B
003A43 _H	003C43 _H				
003A44 _H	003C44 _H	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX _B
003A45 _H	003C45 _H				
003A46 _H	003C46 _H				XXXXX--- XXXXXXXX _B
003A47 _H	003C47 _H				
003A48 _H	003C48 _H	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX _B
003A49 _H	003C49 _H				
003A4A _H	003C4A _H				XXXXX--- XXXXXXXX _B
003A4B _H	003C4B _H				
003A4C _H	003C4C _H	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX _B
003A4D _H	003C4D _H				
003A4E _H	003C4E _H				XXXXX--- XXXXXXXX _B
003A4F _H	003C4F _H				
003A50 _H	003C50 _H	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX _B
003A51 _H	003C51 _H				
003A52 _H	003C52 _H				XXXXX--- XXXXXXXX _B
003A53 _H	003C53 _H				
003A54 _H	003C54 _H	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX _B
003A55 _H	003C55 _H				
003A56 _H	003C56 _H				XXXXX--- XXXXXXXX _B
003A57 _H	003C57 _H				
003A58 _H	003C58 _H	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX _B
003A59 _H	003C59 _H				
003A5A _H	003C5A _H				XXXXX--- XXXXXXXX _B
003A5B _H	003C5B _H				
003A5C _H	003C5C _H	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX _B
003A5D _H	003C5D _H				
003A5E _H	003C5E _H				XXXXX--- XXXXXXXX _B
003A5F _H	003C5F _H				

List of Message Buffers (DLC Registers and Data Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A60 _H	003C60 _H	DLC register 0	DLCR0	R/W	----XXXX _B
003A61 _H	003C61 _H				
003A62 _H	003C62 _H	DLC register 1	DLCR1	R/W	----XXXX _B
003A63 _H	003C63 _H				
003A64 _H	003C64 _H	DLC register 2	DLCR2	R/W	----XXXX _B
003A65 _H	003C65 _H				
003A66 _H	003C66 _H	DLC register 3	DLCR3	R/W	----XXXX _B
003A67 _H	003C67 _H				
003A68 _H	003C68 _H	DLC register 4	DLCR4	R/W	----XXXX _B
003A69 _H	003C69 _H				
003A6A _H	003C6A _H	DLC register 5	DLCR5	R/W	----XXXX _B
003A6B _H	003C6B _H				
003A6C _H	003C6C _H	DLC register 6	DLCR6	R/W	----XXXX _B
003A6D _H	003C6D _H				
003A6E _H	003C6E _H	DLC register 7	DLCR7	R/W	----XXXX _B
003A6F _H	003C6F _H				
003A70 _H	003C70 _H	DLC register 8	DLCR8	R/W	----XXXX
003A71 _H	003C71 _H				
003A72 _H	003C72 _H	DLC register 9	DLCR9	R/W	----XXXX _B
003A73 _H	003C73 _H				
003A74 _H	003C74 _H	DLC register 10	DLCR10	R/W	----XXXX _B
003A75 _H	003C75 _H				
003A76 _H	003C76 _H	DLC register 11	DLCR11	R/W	----XXXX _B
003A77 _H	003C77 _H				
003A78 _H	003C78 _H	DLC register 12	DLCR12	R/W	----XXXX _B
003A79 _H	003C79 _H				
003A7A _H	003C7A _H	DLC register 13	DLCR13	R/W	----XXXX _B
003A7B _H	003C7B _H				
003A7C _H	003C7C _H	DLC register 14	DLCR14	R/W	----XXXX _B
003A7D _H	003C7D _H				
003A7E _H	003C7E _H	DLC register 15	DLCR15	R/W	----XXXX _B
003A7F _H	003C7F _H				
003A80 _H to 003A87 _H	003C80 _H to 003C87 _H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B

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11.2 Recommended Conditions

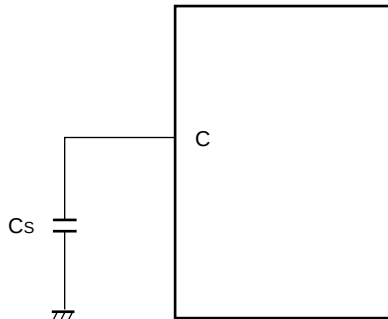
($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value			Units	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.5	5.0	5.5	V	Under normal operation : Other than MB90F548GL(S)/543G(S)/547G(S)/548G(S)
						Under normal operation when A/D converter is used : MB90F548GL(S)/543G(S)/547G(S)/548G(S)
		3.5	5.0	5.5	V	Under normal operation when A/D converter is not used : MB90F548GL(S)/543G(S)/547G(S)/548G(S)
		3.0	—	5.5	V	Maintain RAM data in stop mode
Smooth capacitor	C_S	0.022	0.1	1.0	μF	*
Operating temperature	T_A	−40	—	+105	°C	

*: Use a ceramic capacitor or a capacitor of better 4. AC characteristics. The bypass capacitor should be greater than this capacitor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ C Pin Connection Diagram



11.3 DC Characteristics

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Input H voltage	V_{IHS}	CMOS hysteresis input pin	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IH}	TTL input pin	—	2.0	—	—	V	
	V_{IHM}	MD input pin	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	
Input L voltage	V_{ILS}	CMOS hysteresis input pin	—	$V_{CC} - 0.3$	—	$0.2 V_{CC}$	V	
	V_{IL}	TTL input pin	—	—	—	0.8	V	
	V_{ILM}	MD input pin	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	
Output H voltage	V_{OH}	All output pins	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -4.0 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	V_{OL}	All output pins	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 4.0 \text{ mA}$	—	—	0.4	V	
Input leak current	I_{IL}	—	$V_{CC} = 5.5 \text{ V}$, $V_{SS} < V_I < V_{CC}$	-5	—	5	μA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, RST	—	25	50	100	$k\Omega$	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	$k\Omega$	Except Flash devices

(Continued)

(Continued)

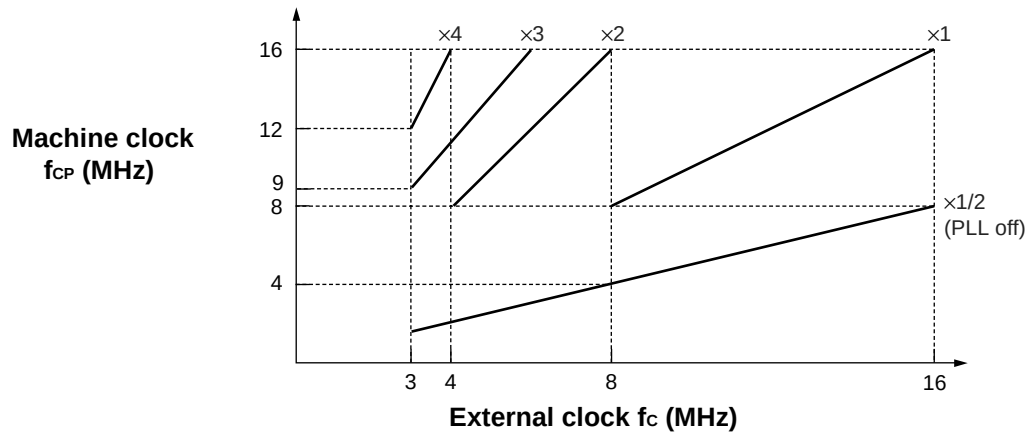
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

Parameter	Sym- bol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Power supply current*	I _{CC}	V _{CC}	Internal frequency : 16 MHz, At normal operating	—	40	55	mA	
			Internal frequency : 16 MHz, At Flash programming/erasing	—	50	70	mA	Flash device
	I _{CCS}		Internal frequency : 16 MHz, At sleep mode	—	12	20	mA	
	I _{CTS}		V _{CC} = 5.0 V ± 10%, Internal frequency : 2 MHz, At pseudo timer mode	—	300	600	μA	
				—	600	1100	μA	MB90F548GL (S) only
				—	200	400	μA	MB90543G(S)/547G(S)/548(S) only
	I _{CCL}		Internal frequency : 8 kHz, At sub operation, T _A = 25 °C	—	400	750	μA	MB90F548GL only
				—	50	100	μA	MASK ROM
				—	150	300	μA	Flash device
	I _{CCLS}		Internal frequency : 8 kHz, At sub sleep, T _A = 25 °C	—	15	40	μA	
I _{CCT}	Internal frequency : 8 kHz, At timer mode, T _A = 25 °C	—	7	25	μA			
I _{CCH1}	At stop, T _A = 25 °C	—	5	20	μA			
I _{CCH2}	At hardware standby mode, T _A = 25 °C	—	50	100	μA			
Input capacity	C _{IN}	Other than AV _{CC} , AV _{SS} , AVRH, AVRL, C, V _{CC} , V _{SS}	—	—	5	15	pF	

* : The power supply current testing conditions are when using the external clock.

■ External clock frequency and Machine clock frequency



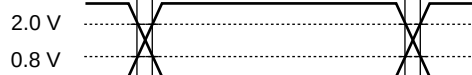
AC characteristics are set to the measured reference voltage values below.

■ Input signal waveform

Hysteresis Input Pin



TTL Input Pin



■ Output signal waveform

Output Pin

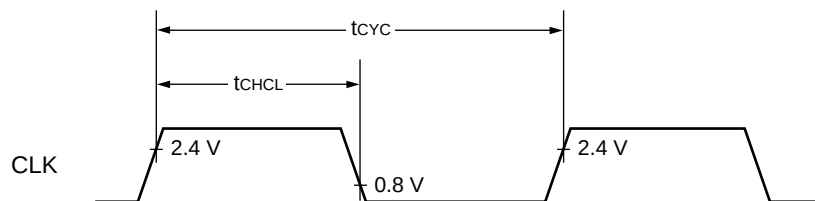


11.4.2 Clock Output Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	$V_{CC} = 5\text{ V} \pm 10\%$	62.5	—	ns	
CLK $\uparrow$ → CLK $\downarrow$	t_{CHCL}			20	—	ns	



11.4.3 Reset and Hardware Standby Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value		Units	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	4 t_{CP}	—	ns	Under normal operation
			Oscillation time of oscillator + 4 t_{CP}	—	ms	In stop mode
			100	—	μs	In pseudo timer mode (MB90543G (S) /547G (S) /548G (S))
			4 t_{CP}	—	ns	In pseudo timer mode (Other than MB90543G (S) /547G (S) /548G (S))
			2 t_{LCP}	—	μs	In sub-clock mode, sub-sleep mode, timer mode
Hardware standby input time	t_{HSTL}	HST	4 t_{CP}	—	ns	Under normal operation

Note : “ t_{cp} ” represents one cycle time of the machine clock.

Oscillation time of oscillator is time that amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ns.

Any reset can not fully initialize the Flash Memory if it is performing the automatic algorithm.

11.4.4 Power On Reset

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

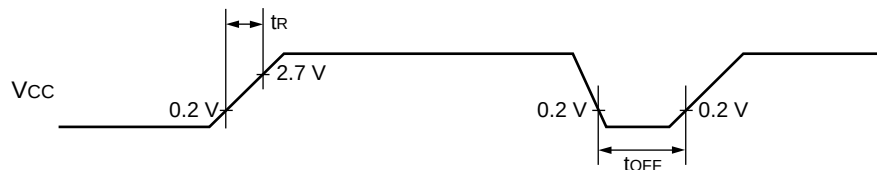
(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	*
Power off time	t_{OFF}	V_{CC}	—	50	—	ms	Waiting time until power-on

* : V_{CC} must be kept lower than 0.2 V before power-on.

Notes : ■ The above values are used for creating a power-on reset.

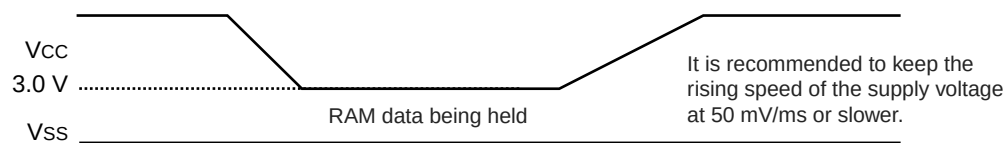
■ Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset.

To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.

In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.

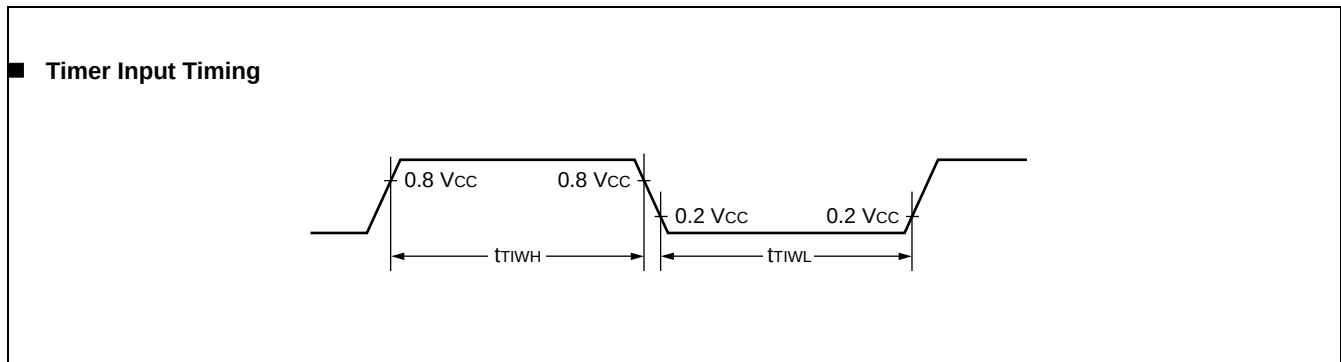


11.4.10 Timer Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	$4\ t_{CP}$	—	ns	
	t_{TIWL}	INO to IN7					

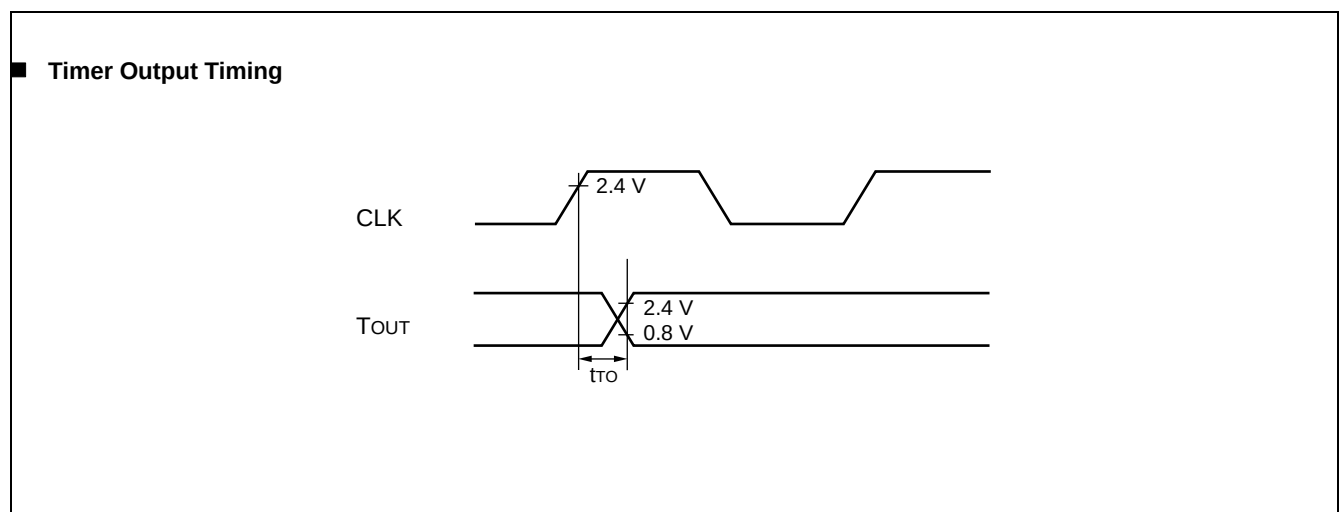


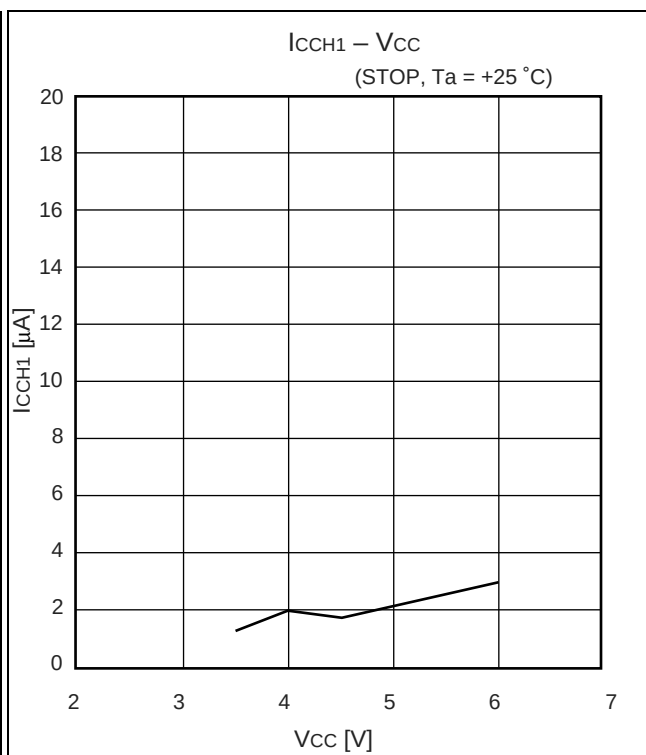
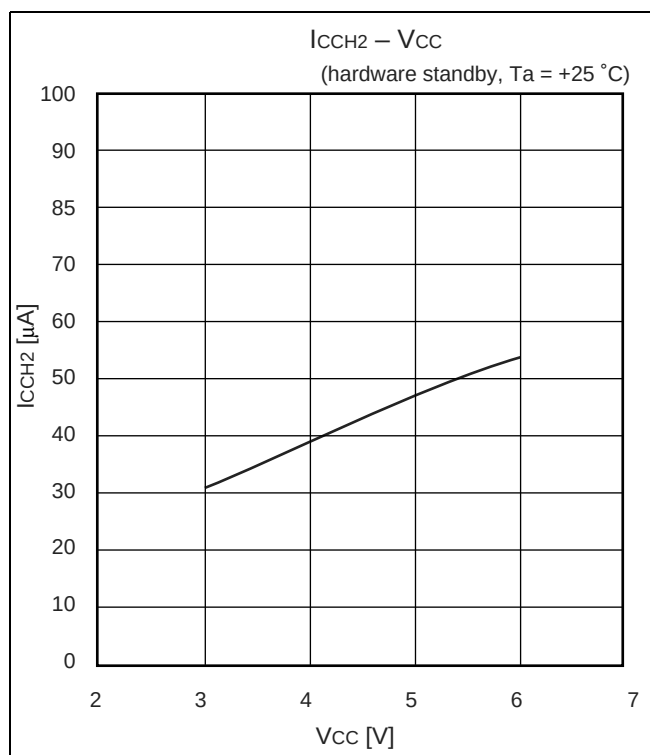
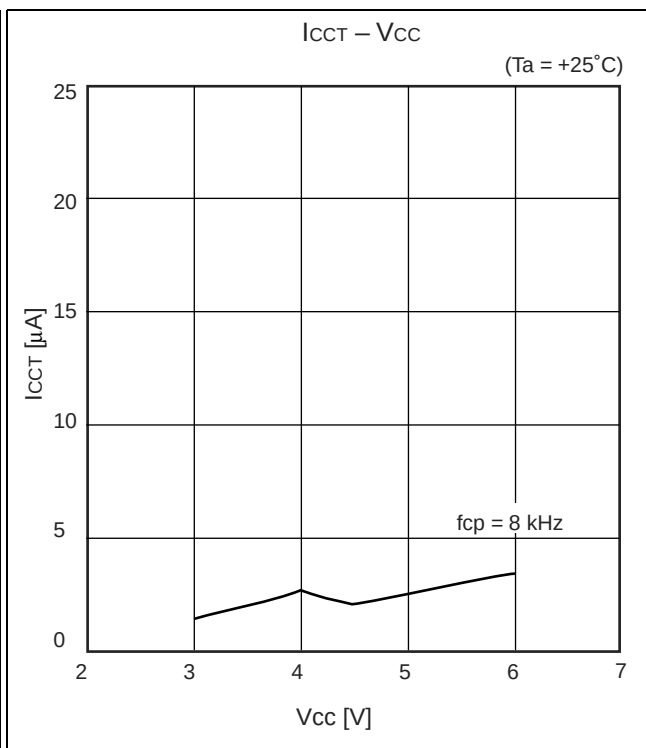
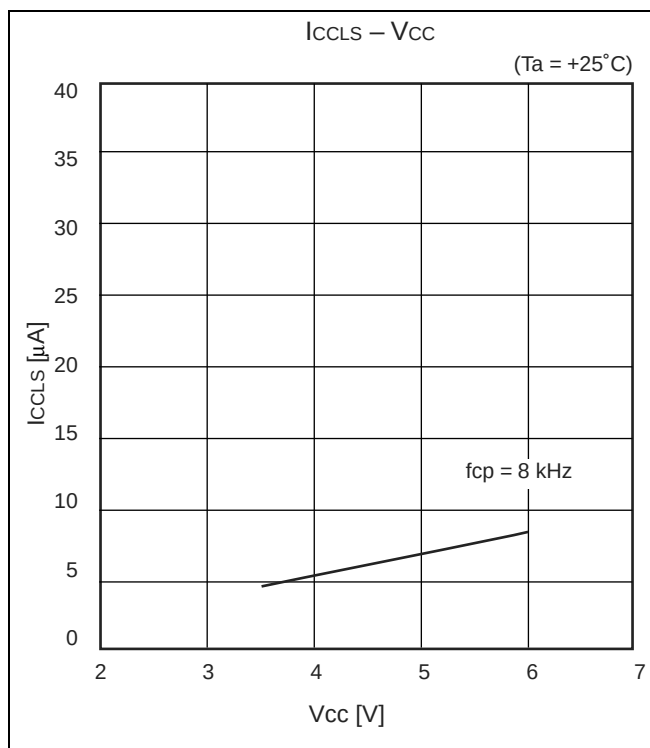
11.4.11 Timer Output Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
CLK $\uparrow$ → T _{OUT} change time	t_{TO}	TOT0, TOT1, PPG0 to PPG3	—	30	—	ns	





■ Power supply current (MB90F549G)

