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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspf-gs-9021

Starting by an external trigger input.
Conversion time : 26.3 μs

- FULL-CAN interfaces
  MB90540G series : 2 channels
  MB90545G series : 1 channel
  Conforming to Version 2.0 Part A and Part B
  Flexible message buffering (mailbox and FIFO buffering can be mixed)
- External bus interface : Maximum address space 16 Mbytes
- Package: QFP-100, LQFP-100

Contents

Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
11	13	P33	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode, external bus 8-bit mode or when WRH pin output is disabled.
		$\overline{\text{WRH}}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{\text{WRH}}$ output pin is enabled.
12	14	P34	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.
13	15	P35	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.
14	16	P36	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.
		RDY		Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.
15	17	P37	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the CLK output is disabled.
		CLK		CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled.
16	18	P40	G	General I/O port. This function is enabled when UART0 disables the serial data output.
		SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.
17	19	P41	G	General I/O port. This function is enabled when UART0 disables serial clock output.
		SCK0		Serial clock I/O pin for UART0. This function is enabled when UART0 enables the serial clock output.
18	20	P42	G	General I/O port. This function is always enabled.
		SIN0		Serial data input pin for UART0. Set the corresponding Port Direction Register to input if this function is used.
19	21	P43	G	General I/O port. This function is always enabled.
		SIN1		Serial data input pin for UART1. Set the corresponding Port Direction Register to input if this function is used.

(Continued)

Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
20	22	P44	G	General I/O port. This function is enabled when UART1 disables the clock output.
		SCK1		Serial clock pulse I/O pin for UART1. This function is enabled when UART1 enables the serial clock output.
22	24	P45	G	General I/O port. This function is enabled when UART1 disables the serial data output.
		SOT1		Serial data output pin for UART1. This function is enabled when UART1 enables the serial data output.
23	25	P46	G	General I/O port. This function is enabled when the Extended I/O serial interface disables the serial data output.
		SOT2		Serial data output pin for the Extended I/O serial interface. This function is enabled when the Extended I/O serial interface enables the serial data output.
24	26	P47	G	General I/O port. This function is enabled when the Extended I/O serial interface disables the clock output.
		SCK2		Serial clock pulse I/O pin for the Extended I/O serial interface . This function is enabled when the Extended I/O serial interface enables the Serial clock output.
26	28	P50	D	General I/O port. This function is always enabled.
		SIN2		Serial data input pin for the Extended I/O serial interface . Set the corresponding Port Direction Register to input if this function is used.
27 to 30	29 to 32	P51 to P54	D	General I/O port. This function is always enabled.
		INT4 to INT7		External interrupt request input pins for INT4 to INT7. Set the corresponding Port Direction Register to input if this function is used.
31	33	P55	D	General I/O port. This function is always enabled.
		ADTG		Trigger input pin for the A/D converter. Set the corresponding Port Direction Register to input if this function is used.
36 to 39	38 to 41	P60 to P63	E	General I/O port. This function is enabled when the analog input enable register specifies a port.
		AN0 to AN3		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.
41 to 44	43 to 46	P64 to P67	E	General I/O port. The function is enabled when the analog input enable register specifies a port.
		AN4 to AN7		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.
45	47	P56	D	General I/O port. This function is always enabled.
		TIN0		Event input pin for the 16-bit reload timers 0. Set the corresponding Port Direction Register to input if this function is used.

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
24H	Serial mode register 1	SMR1	R/W	UART1	0 0 0 0 0 0 0 0B
25H	Serial control register 1	SCR1	R/W		0 0 0 0 0 1 0 0B
26H	Serial input data register 1/ Serial output data register 1	SIDR1/SODR1	R/W		XXXXXXXXB
27H	Serial status register 1	SSR1	R/W		0 0 0 0 1_0 0B
28H	UART1 prescaler control register	CDCR	R/W		0_ _ _1 1 1 1B
29H	Serial Edge select register	SES1	R/W		_ _ _ _ _ _ _0B
2AH	Prohibited				
2BH	Serial I/O prescaler	SCDCR	R/W	Extended I/O Serial Interface	0_ _ _1 1 1 1B
2CH	Serial mode control register	SMCS	R/W		_ _ _ _0 0 0 0B
2DH	Serial mode control register	SMCS	R/W		0 0 0 0 0 0 1 0B
2EH	Serial data register	SDR	R/W		XXXXXXXXB
2FH	Serial Edge select register	SES2	R/W		_ _ _ _ _ _ _0B
30H	External interrupt enable register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0B
31H	External interrupt request register	EIRR	R/W		XXXXXXXXB
32H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0B
33H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0B
34H	A/D control status register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0B
35H	A/D control status register 1	ADCS1	R/W		0 0 0 0 0 0 0 0B
36H	A/D data register 0	ADCR0	R		XXXXXXXXB
37H	A/D data register 1	ADCR1	R/W		0 0 0 0 1 _ XXB
38H	PPG0 operation mode control register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 0 _ _ 1B
39H	PPG1 operation mode control register	PPGC1	R/W		0 _ 0 0 0 0 0 1B
3AH	PPG0/1 clock selection register	PPG01	R/W		0 0 0 0 0 0 _ _B
3BH	Prohibited				
3CH	PPG2 operation mode control register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 0 _ _1B
3DH	PPG3 operation mode control register	PPGC3	R/W		0 _ 0 0 0 0 0 1B
3EH	PPG2/3 Clock Selection Register	PPG23	R/W		0 0 0 0 0 0 _ _B
3FH	Prohibited				
40H	PPG4 operation mode control register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 0 _ _ 1B
41H	PPG5 operation mode control register	PPGC5	R/W		0 _ 0 0 0 0 0 1B
42H	PPG4/5 clock selection register	PPG45	R/W		0 0 0 0 0 0 _ _B
43H	Prohibited				
44H	PPG6 operation mode control register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 0 _ _ 1B
45H	PPG7 operation mode control register	PPGC7	R/W		0 _ 0 0 0 0 0 1B
46H	PPG6/7 clock selection register	PPG67	R/W		0 0 0 0 0 0 _ _B

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9. CAN Controller

The MB90540G series contains two CAN controllers (CAN0 and CAN1) , the MB90545G series contains only one (CAN0) . The Evaluation Chip MB90V540G also has two CAN controllers.

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 1 Mbps (when input clock is at 16 MHz)

List of Control Registers

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070_H	000080_H	Message buffer valid register	BVALR	R/W	$00000000\ 00000000_B$
000071_H	000081_H				
000072_H	000082_H	Transmit request register	TREQR	R/W	$00000000\ 00000000_B$
000073_H	000083_H				
000074_H	000084_H	Transmit cancel register	TCANR	W	$00000000\ 00000000_B$
000075_H	000085_H				
000076_H	000086_H	Transmit complete register	TCR	R/W	$00000000\ 00000000_B$
000077_H	000087_H				
000078_H	000088_H	Receive complete register	RCR	R/W	$00000000\ 00000000_B$
000079_H	000089_H				
$00007A_H$	$00008A_H$	Remote request receiving register	RRTRR	R/W	$00000000\ 00000000_B$
$00007B_H$	$00008B_H$				
$00007C_H$	$00008C_H$	Receive overrun register	ROVRR	R/W	$00000000\ 00000000_B$
$00007D_H$	$00008D_H$				
$00007E_H$	$00008E_H$	Receive interrupt enable register	RIER	R/W	$00000000\ 00000000_B$
$00007F_H$	$00008F_H$				

(Continued)

List of Message Buffers (DLC Registers and Data Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A60H	003C60H	DLC register 0	DLCR0	R/W	----XXXXB
003A61H	003C61H				
003A62H	003C62H	DLC register 1	DLCR1	R/W	----XXXXB
003A63H	003C63H				
003A64H	003C64H	DLC register 2	DLCR2	R/W	----XXXXB
003A65H	003C65H				
003A66H	003C66H	DLC register 3	DLCR3	R/W	----XXXXB
003A67H	003C67H				
003A68H	003C68H	DLC register 4	DLCR4	R/W	----XXXXB
003A69H	003C69H				
003A6AH	003C6AH	DLC register 5	DLCR5	R/W	----XXXXB
003A6BH	003C6BH				
003A6CH	003C6CH	DLC register 6	DLCR6	R/W	----XXXXB
003A6DH	003C6DH				
003A6EH	003C6EH	DLC register 7	DLCR7	R/W	----XXXXB
003A6FH	003C6FH				
003A70H	003C70H	DLC register 8	DLCR8	R/W	----XXXX
003A71H	003C71H				
003A72H	003C72H	DLC register 9	DLCR9	R/W	----XXXXB
003A73H	003C73H				
003A74H	003C74H	DLC register 10	DLCR10	R/W	----XXXXB
003A75H	003C75H				
003A76H	003C76H	DLC register 11	DLCR11	R/W	----XXXXB
003A77H	003C77H				
003A78H	003C78H	DLC register 12	DLCR12	R/W	----XXXXB
003A79H	003C79H				
003A7AH	003C7AH	DLC register 13	DLCR13	R/W	----XXXXB
003A7BH	003C7BH				
003A7CH	003C7CH	DLC register 14	DLCR14	R/W	----XXXXB
003A7DH	003C7DH				
003A7EH	003C7EH	DLC register 15	DLCR15	R/W	----XXXXB
003A7FH	003C7FH				
003A80H to 003A87H	003C80H to 003C87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB

(Continued)

(Continued)

*1 : The interrupt request flag is cleared by the EI²OS interrupt clear signal.

*2 : The interrupt request flag is cleared by the EI²OS interrupt clear signal. A stop request is available.

Notes :

- N/A : The interrupt request flag is not cleared by the EI²OS interrupt clear signal.
- For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.
- At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by a hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.
- If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0.0$ V)

Parameter	Symbol	Value		Units	Remarks
		Min	Max		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *1
	AVRH, AVRL	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq$ AVRH/AVRL, AVRH $\geq$ AVRL *1
Input voltage	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Output voltage	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Maximum clamp current	I_{CLAMP}	−2.0	+2.0	mA	*6
Total maximum clamp current	$\Sigma\lvert I_{CLAMP} \rvert$	−	20	mA	*6
“L” level max output current	I_{OL}	−	15	mA	*3
“L” level avg. output current	I_{OLAV}	−	4	mA	*4
“L” level max overall output current	ΣI_{OL}	−	100	mA	
“L” level avg. overall output current	ΣI_{OLAV}	−	50	mA	*5
“H” level max output current	I_{OH}	−	−15	mA	*3
“H” level avg. output current	I_{OHAV}	−	−4	mA	*4
“H” level max overall output current	ΣI_{OH}	−	−100	mA	
“H” level avg. overall output current	ΣI_{OHAV}	−	−50	mA	*5
Power consumption	P_D	−	500	mW	Flash device
		−	400	mW	MASK ROM
Operating temperature	T_A	−40	+105	°C	
Storage temperature	T_{STG}	−55	+150	°C	

*1 : AV_{CC}, AVRH, AVRL should not exceed V_{CC}. Also, AVRH, AVRL should not exceed AV_{CC}, and AVRL does not exceed AVRH.

*2 : V_I and V_O should not exceed $V_{CC} + 0.3$ V. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supercedes the V_I rating.

*3 : The maximum output current is a peak value for a corresponding pin.

*4 : Average output current is an average current value observed for a 100 ms period for a corresponding pin.

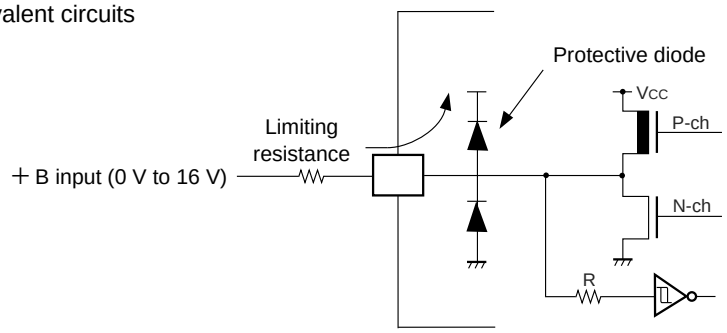
*5 : Total average current is an average current value observed for a 100 ms period for all corresponding pins.

*6 :

- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The + B signal should always be applied with a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the + B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a + B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- Care must be taken not to leave the + B input pin open.

- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept + B signal input.
- Sample recommended circuits :

■ Input/Output Equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

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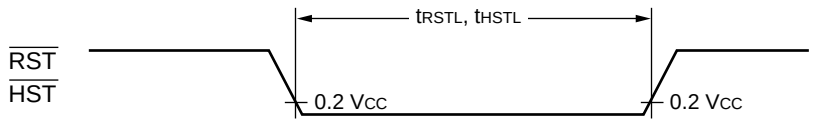
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

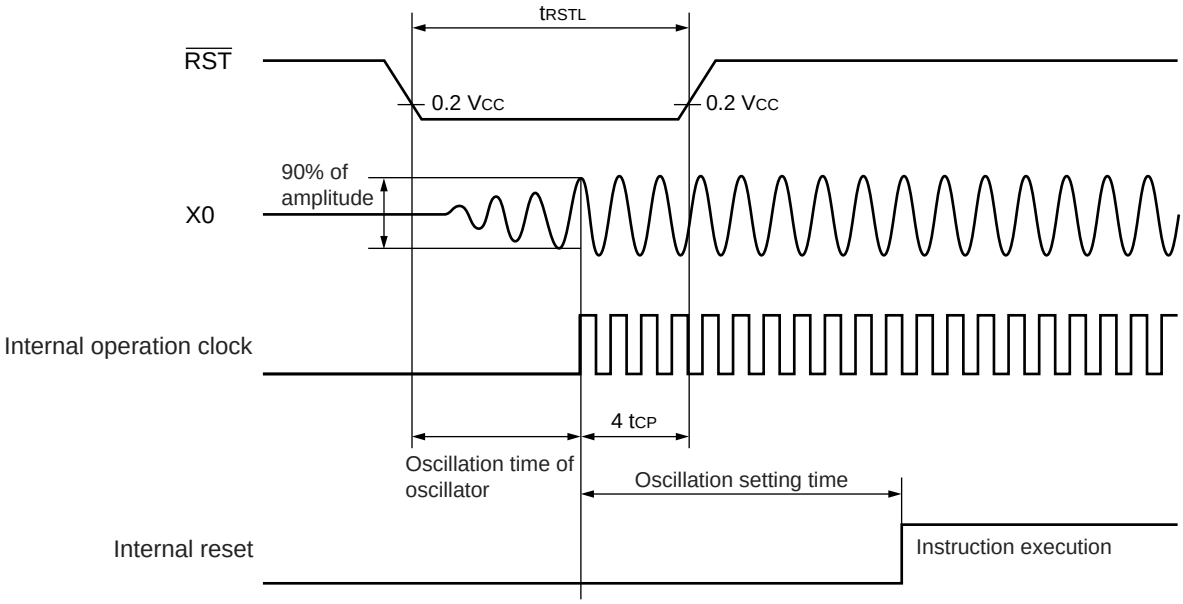
(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	No multiplier When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			62.5	—	125	ns	PLL multiplied by 1 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			125	—	250	ns	PLL multiplied by 2 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			187.5	—	333	ns	PLL multiplied by 3 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			250	—	333	ns	PLL multiplied by 4 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			200	—	333	ns	When using an oscillator circuit V_{CC} < 4.5 V(MB90F548GL(S)/543G(S)/547G(S)/548G(S))
			62.5	—	333	ns	No multiplier When using an external clock
			62.5	—	125	ns	PLL multiplied by 1 When using an external clock
			125	—	250	ns	PLL multiplied by 2 When using an external clock
			187.5	—	333	ns	PLL multiplied by 3 When using an external clock
			250	—	333	ns	PLL multiplied by 4 When using an external clock
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WLH}, P_{WLL}	X0A	—	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using an external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	When using main clock
	f_{LCP}	—	—	8.192	—	kHz	When using sub-clock
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	When using main clock
	t_{LCP}	—	—	122.1	—	µs	When using sub-clock

■ In under normal operation, pseudo timer mode, sub-clock mode, sub-sleep mode, timer mode



■ In stop mode



11.4.7 Ready Input Timing

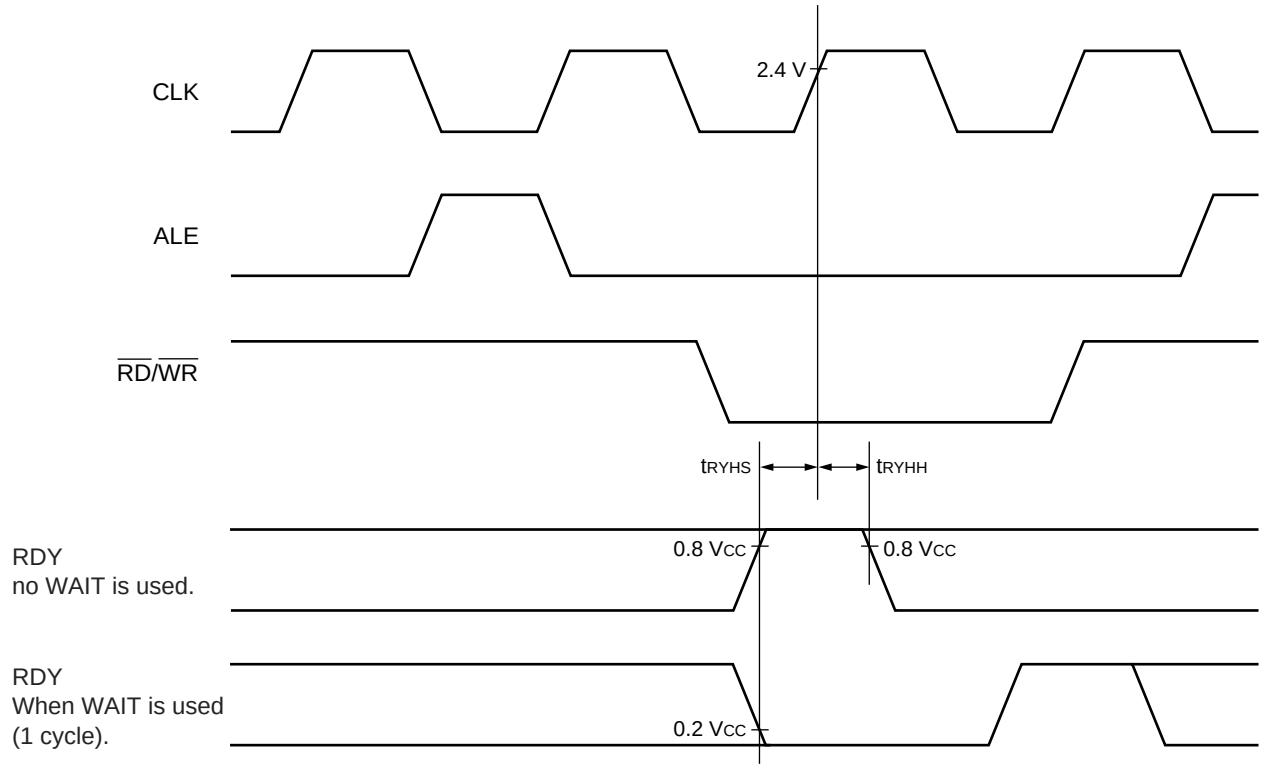
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.

■ **Ready Input Timing**



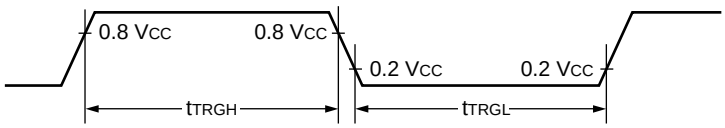
11.4.12 Trigger Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT7, ADTG	—	5 t_{CP}	—	ns	Under nomal operation
				1	—	µs	In stop mode

■ **Trigger Input Timing**



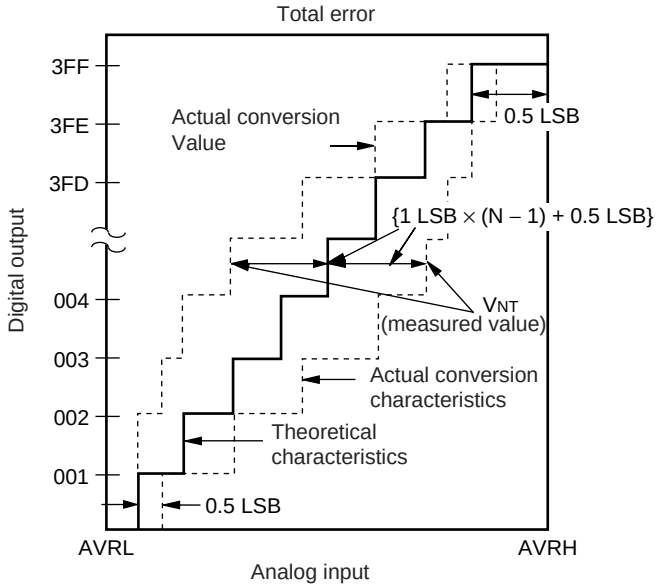
11.5.2 A/D Converter Glossary

Resolution : Analog changes that are identifiable with the A/D converter

Linearity error : The deviation of the straight line connecting the zero transition point (“00 0000 0000” ⟷ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ⟷ “11 1111 1111”) from actual conversion characteristics

Differential linearity error : The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error : The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1\,\text{LSB} = (\text{Theoretical value})\,\frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

$$V_{OT}\ (\text{Theoretical value}) = \text{AVRL} + 0.5\ \text{LSB}\ [\text{V}]$$

$$V_{FST}\ (\text{Theoretical value}) = \text{AVRH} - 1.5\ \text{LSB}\ [\text{V}]$$

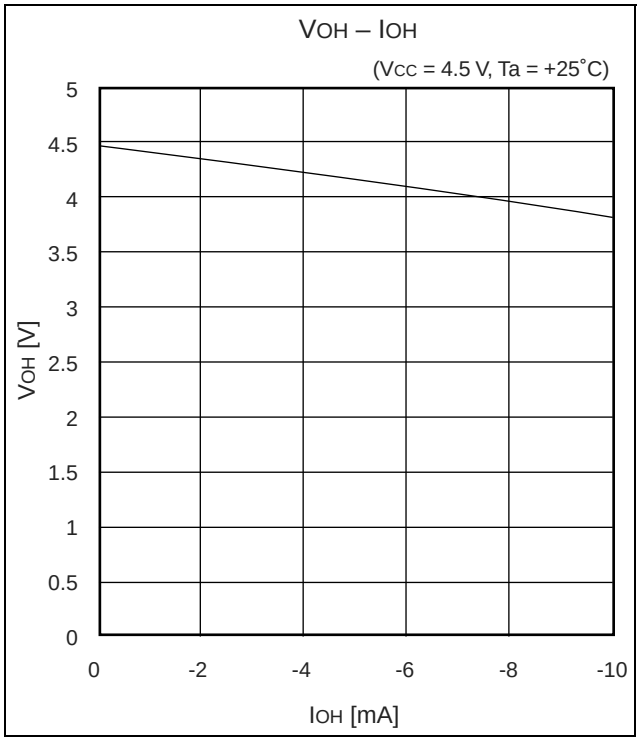
$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (\text{N} - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

V_{NT} : Voltage at a transition of digital output from (N − 1) to N

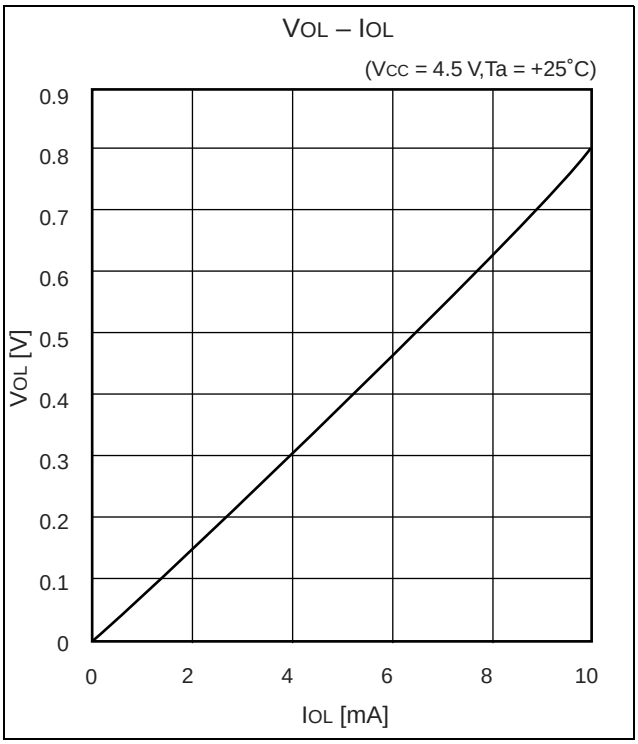
(Continued)

12. Example Characteristics

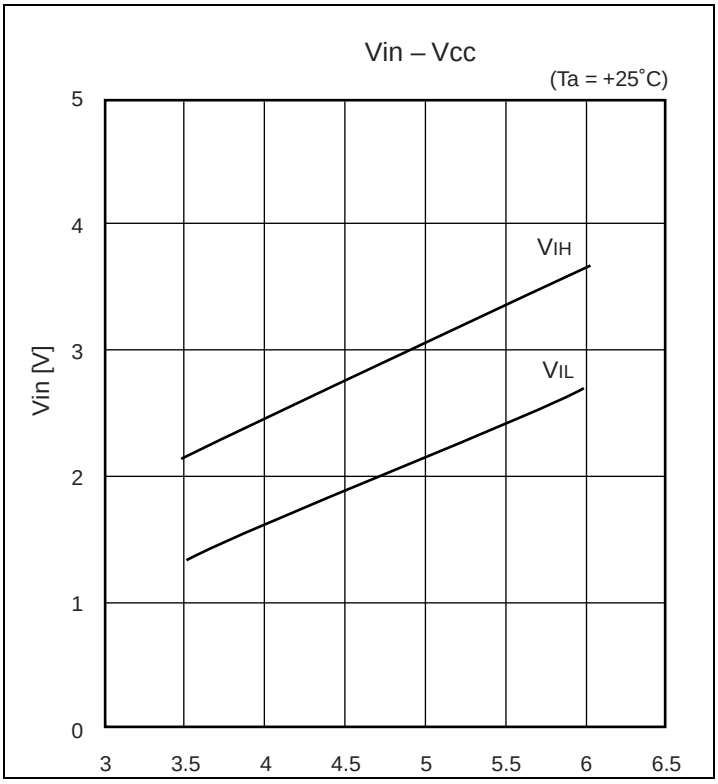
■ “H” level output voltage



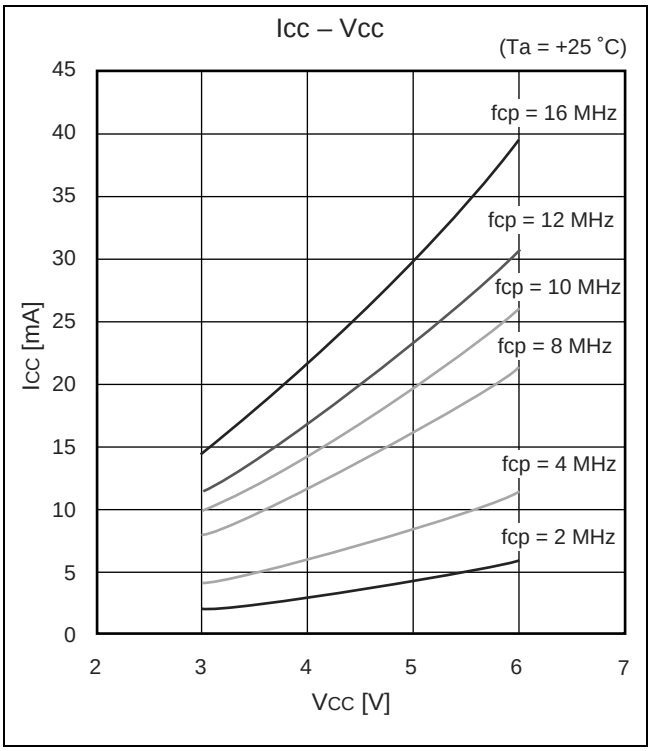
■ “L” level output voltage

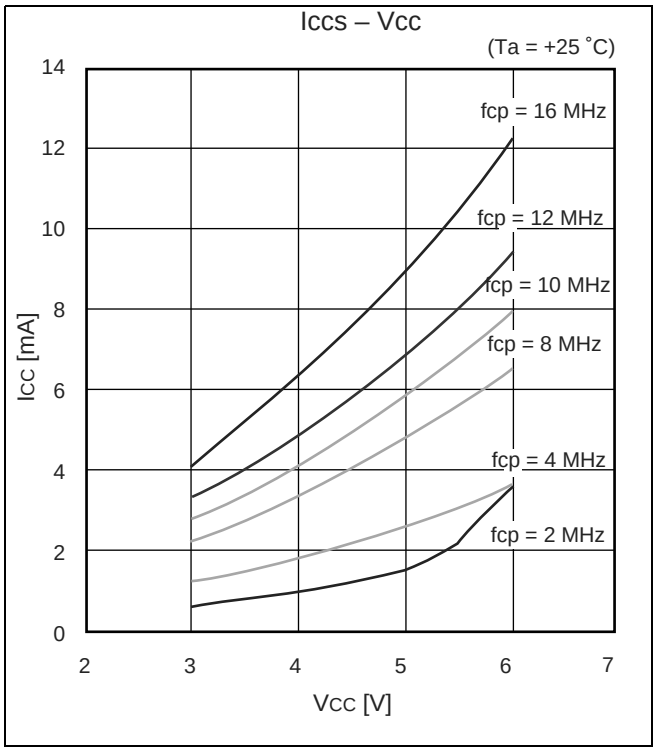


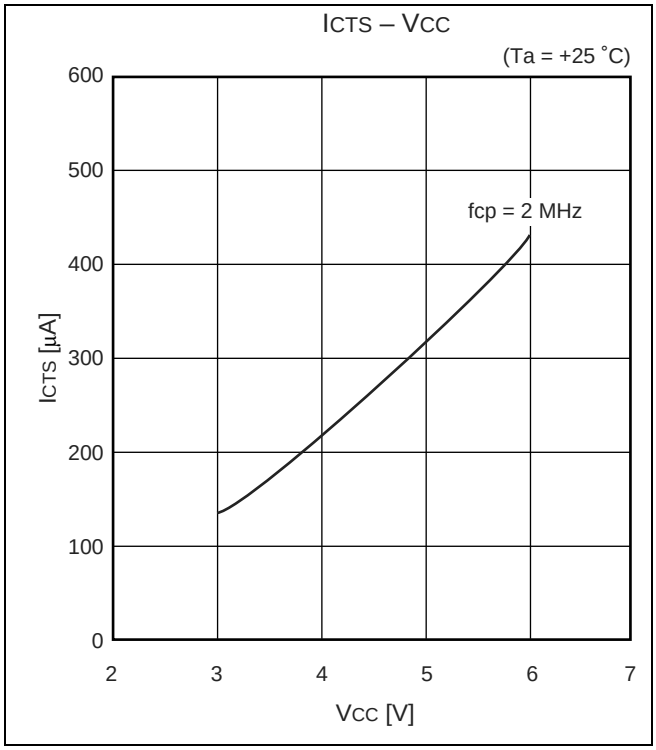
■ “H” level input voltage/ “L” level input voltage (Hysterisis inpiut)

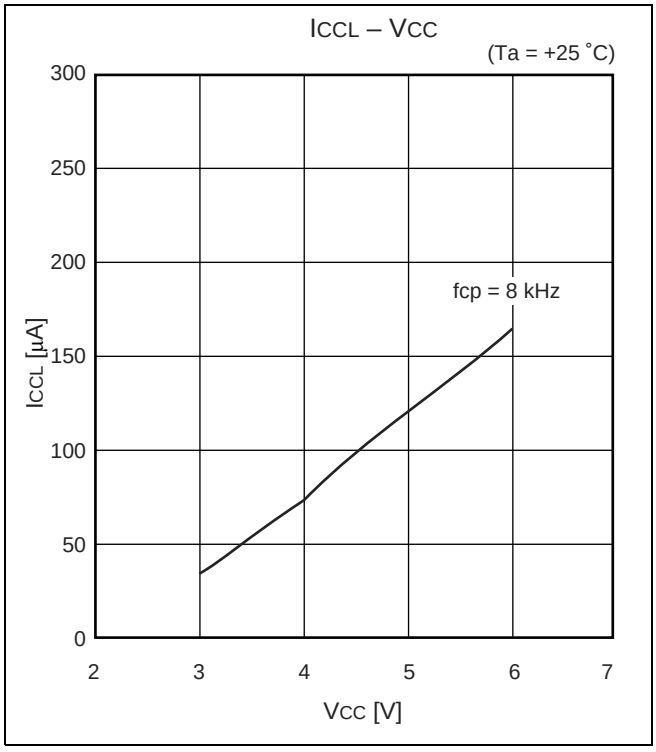


■ Power supply current (MB90F549G)

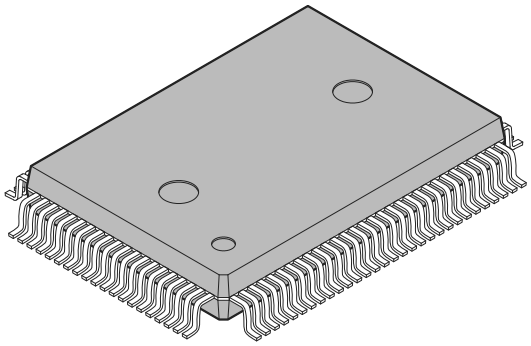


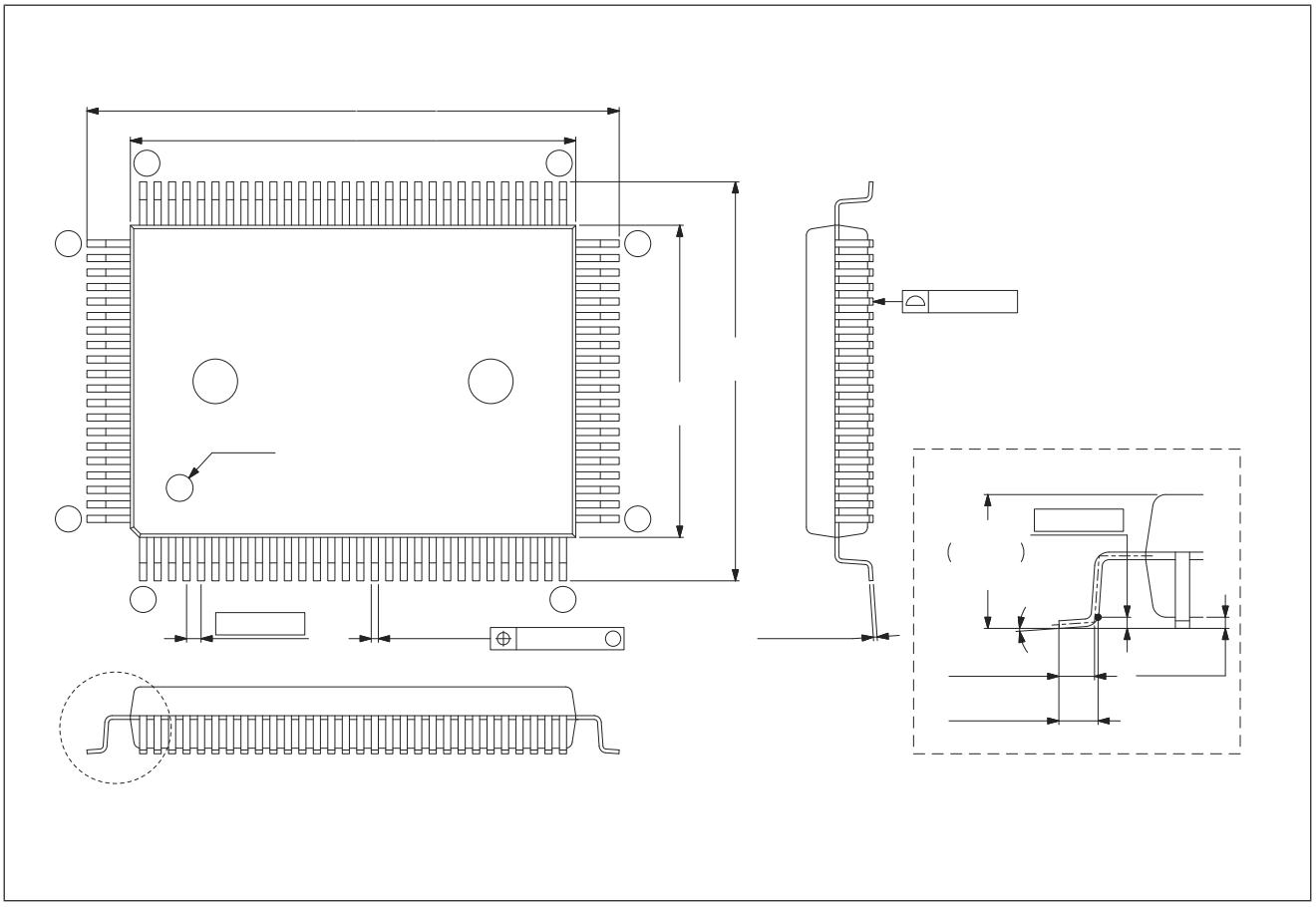






14. Package Dimensions



(Continued)

15. Major Changes

Spansion Publication Number: DS07-13703-7E

Section	Change Results
■ PRODUCT LINEUP	Changed the name in peripheral resource. 16-bit I/O Timer → 16-bit Free-run Timer
■ I/O CIRCUIT TYPE	Changed the name of input typ. Hysteresis → CMOS Hysteresis HYS → CMOS Hysteresis
■ BLOCK DIAGRAM	Changed the arrow direction of SOT1 signal at UART1(SCI). "← →" (input/output) → "←" (output)
■ I/O MAP	Changed the text of "Note".
■ INTERRUPT MAP	Changed the name of peripheral resource of the pin number: #19. I/O Timer → 16-bit Free-run Timer
■ ELECTRICAL CHARACTERISTICS 2. Recommended Conditions	Changed the remarks of "parameter: Power supply voltage".
3. DC Characteristics	Changed the maximum value of symbol : VILM of parameter: Input voltage. V_{CC} + 0.3 → V_{SS} + 0.3
	Added the following remarks for parameter : Pull-down resistance. Except Flash device
4. AC Characteristics (1) Clock Timing	Added the value when using an external clock in Oscillation frequency and Clock cycle time on (1) Clock Timing for parameter.
	Added the item of A/D converter operation range in figure of "■ Guaranteed PLL operation range"
(3) Reset and Hardware Standby Input Timing	Changed the following item. (3) Reset and Hardware Standby Input Timing Remarks: In sub-clock mode, sub-sleep mode, timer mode $2t_{CP}$ → $2t_{LCP}$
(4) Power On Reset	Changed as follows; Due to repetitive operation → Waiting time until power-on
5. A/D Converter	Changed the unit of Zero transition voltage and Full scale transition voltage. mV → V
■ ORDERING INFORMATION	Added the MB90F548GLPMC in Part Numbers.

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: MB90F543G(S)/546G(S)/548G(S)/549G(S)/549G(S)/V540G/MB90543G(S)/547G(S)/548G(S)/F548GL(S) CMOS F2MC-16LX MB90540G/545G Series 16-bit Proprietary Microcontroller
Document Number: 002-07696

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	11/13/2008	Migrated to Cypress and assigned document number 002-07696. No change to document contents or format.
*A	5537115	AKIH	11/30/2016	Updated to Cypress template

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