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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspf-gs-9021
i di ciidae ONL	





Starting by an external trigger input. Conversion time: 26.3 µs

■ FULL-CAN interfaces

MB90540G series : 2 channels MB90545G series : 1 channel

Conforming to Version 2.0 Part A and Part B

Flexible message buffering (mailbox and FIFO buffering can be mixed)

■ External bus interface : Maximum address space 16 Mbytes

■ Package: QFP-100, LQFP-100





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Pin	No.	B'	0::	Function				
LQFP*2	QFP*1	- Pin name	Circuit type	Function				
		P33		General I/O port with programmable pullup. This function is enabled in the single-chip mode, external bus 8-bit mode or when WRH pin output is disabled.				
11	13	WRH	I	Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the WRH output pin is enabled.				
12	14	P34		General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.				
12	14	HRQ		Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.				
12	45	P35		General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.				
13	15	HAK		Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.				
4.4	40	P36		General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.				
14	16	RDY		Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.				
15	47	P37	- н	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the CLK output is disabled.				
15	17	CLK		CLK output pin. This function is enabled when both the external bus and CL outputs are enabled.				
16	18	P40	- G	General I/O port. This function is enabled when UART0 disables the serial data output.				
סו	10	SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.				
17	10	P41	- G	General I/O port. This function is enabled when UART0 disables serial clock output.				
17	19 SCK0			Serial clock I/O pin for UART0. This function is enabled when UART0 enables the serial clock output.				
		P42		General I/O port. This function is always enabled.				
18	20 SINO		G	Serial data input pin for UART0. Set the corresponding Port Direction Register to input if this function is used.				
		P43		General I/O port. This function is always enabled.				
19	21	SIN1	G	Serial data input pin for UART1. Set the corresponding Port Direction Register to input if this function is used.				



Pin No.		Din nome	Cincuit turns	Firmation				
LQFP*2	QFP*1	Pin name	Circuit type	Function				
20	22	P44	– G	General I/O port. This function is enabled when UART1 disables the clock output.				
20	22	SCK1		Serial clock pulse I/O pin for UART1. This function is enabled when UART1 enables the serial clock output.				
22	24	P45	_ G	General I/O port. This function is enabled when UART1 disables the serial data output.				
22	24	SOT1		Serial data output pin for UART1. This function is enabled when UART1 enables the serial data output.				
.00	05	P46		General I/O port. This function is enabled when the Extended I/O serial interface disables the serial data output.				
23	25	SOT2	– G	Serial data output pin for the Extended I/O serial interface. This function is enabled when the Extended I/O serial interface enables the serial data output.				
		P47		General I/O port. This function is enabled when the Extended I/O serial interface disables the clock output.				
24	24 26	SCK2	G	Serial clock pulse I/O pin for the Extended I/O serial interface. This function is enabled when the Extended I/O serial interface enables the Serial clock output.				
		P50		General I/O port. This function is always enabled.				
26	28	SIN2	D	Serial data input pin for the Extended I/O serial interface . Set the corresponding Port Direction Register to input if this function is used.				
		P51 to P54		General I/O port. This function is always enabled.				
27 to 30	29 to 32	INT4 to INT7	D	External interrupt request input pins for INT4 to INT7. Set the corresponding Port Direction Register to input if this function is used.				
		P55		General I/O port. This function is always enabled.				
31	33	ADTG	D	Trigger input pin for the A/D converter. Set the corresponding Port Direction Register to input if this function is used.				
36 to 39	38 to 41	P60 to P63	— E	General I/O port. This function is enabled when the analog input enable register specifies a port.				
36 10 39	36 10 41	AN0 to AN3		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.				
44 to 44	42 to 46	P64 to P67	– E	General I/O port. The function is enabled when the analog input enable register specifies a port.				
41 to 44	43 to 46	AN4 to AN7		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.				
		P56		General I/O port. This function is always enabled.				
45	47	TINO	D	Event input pin for the 16-bit reload timers 0. Set the corresponding Port Direction Register to input if this function is used.				



Address	Register	Abbreviation	Access	Resource name	Initial value
24н	Serial mode register 1	SMR1	R/W		0 0 0 0 0 0 0 0в
25н	Serial control register 1	SCR1	R/W		0 0 0 0 0 1 0 0в
26н	Serial input data register 1/ Serial output data register 1	SIDR1/SODR1	R/W	UART1	XXXXXXXXB
27н	Serial status register 1	SSR1	R/W		0 0 0 0 1_0 0в
28н	UART1 prescaler control register	CDCR	R/W		01 1 1 1в
29н	Serial Edge select register	SES1	R/W		Ов
2Ан	Prohibited	·		•	
2Вн	Serial I/O prescaler	SCDCR	R/W		01 1 1 1в
2Сн	Serial mode control register	SMCS	R/W		0 0 0 0в
2Dн	Serial mode control register	SMCS	R/W	Extended I/O Serial Interface	0 0 0 0 0 0 1 0в
2Ен	Serial data register	SDR	R/W		XXXXXXXXB
2F _H	Serial Edge select register	SES2	R/W		Ов
30н	External interrupt enable register	ENIR	R/W		0 0 0 0 0 0 0 0в
31н	External interrupt request register	EIRR	R/W	Forte me al late mount	XXXXXXXXB
32н	External interrupt level register	ELVR	R/W	External Interrupt	0 0 0 0 0 0 0 0в
33н	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0в
34н	A/D control status register 0	ADCS0	R/W		0 0 0 0 0 0 0 0в
35н	A/D control status register 1	ADCS1	R/W	A/D Commenter	0 0 0 0 0 0 0 0в
36н	A/D data register 0	ADCR0	R	A/D Converter	XXXXXXXXB
37н	A/D data register 1	ADCR1	R/W		0 0 0 0 1 _ XX _B
38н	PPG0 operation mode control register	PPGC0	R/W	16-bit Programmable	0_0001в
39н	PPG1 operation mode control register	PPGC1	R/W	Pulse	0_00001в
ЗАн	PPG0/1 clock selection register	PPG01	R/W	Generator 0/1	0 0 0 0 0 0в
3Вн	Prohibited				
3Сн	PPG2 operation mode control register	PPGC2	R/W	16-bit Programmable	0_0001в
3Dн	PPG3 operation mode control register	PPGC3	R/W	Pulse	0_00001в
3Ен	PPG2/3 Clock Selection Register	PPG23	R/W	Generator 2/3	000000в
3Fн	Prohibited				
40н	PPG4 operation mode control register	PPGC4	R/W	16-bit Programmable	0_0001в
41н	PPG5 operation mode control register	PPGC5	R/W	1 0100	0_00001в
42н	PPG4/5 clock selection register	PPG45	R/W	Generator 4/5	0 0 0 0 0 0в
43н	Prohibited	•		•	•
44 _H	PPG6 operation mode control register	PPGC6	R/W	16-bit Programmable	0_0001в
45н	PPG7 operation mode control register	PPGC7	R/W	Pulse	0_00001в
46н	PPG6/7 clock selection register	PPG67	R/W	Generator 6/7	0 0 0 0 0 0в



9. CAN Controller

The MB90540G series contains two CAN controllers (CAN0 and CAN1) , the MB90545G series contains only one (CAN0) . The Evaluation Chip MB90V540G also has two CAN controllers.

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
 - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
 - □ 29-bit ID and 8-byte data
 - □ Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
 - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 1 Mbps (when input clock is at 16 MHz)

List of Control Registers

Address		Dogistor	Abbreviation	Access	Initial Value	
CAN0	CAN1	Register	Appreviation	Access	initial value	
000070н	000080н	Managa buffar valid register	BVALR	R/W	0000000 00000000	
000071н	000081н	Message buffer valid register	DVALK	R/VV	0000000 0000000B	
000072н	000082н	Transmit required register	TREOR	R/W	00000000 00000000в	
000073н	000083н	Transmit request register	IREQR	R/VV	0000000 0000000В	
000074н	000084н	Transmit cancel register	TCANR	W	00000000 00000000в	
000075н	000085н	Transmit cancel register	TCANK	VV	0000000 0000000B	
000076н	000086н	Transmit complete register	TCR	R/W	00000000 00000000В	
000077н	000087н	Transmit complete register	TCR	R/VV		
000078н	000088н	Descive complete register	RCR	R/W	0000000 00000000	
000079н	000089н	Receive complete register	RCR	R/VV	00000000 00000000В	
00007Ан	00008Ан	Remote request receiving register	RRTRR	R/W	0000000 00000000-	
00007Вн	00008Вн	Remote request receiving register	KKIKK	K/VV	00000000 00000000В	
00007Сн	00008Сн	Pagaiya ayarrun ragiatar	ROVRR	R/W	00000000 00000000	
00007Dн	00008Dн	Receive overrun register	KOVKK	IK/ VV	0000000 0000000B	
00007Ен	00008Ен	Pageive interrupt applie register	RIER	R/W	00000000 00000000	
00007Fн	00008Fн	Receive interrupt enable register	RIER	K/VV	0000000 0000000B	

(Continued)

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List of Message Buffers (DLC Registers and Data Registers)

Address							
CAN0	CAN1	Register	Abbreviation	Access	Initial Value		
003А60н	003С60н	DI C register 0	DLCR0	DAM	XXXX _B		
003А61н	003С61н	DLC register 0	DLCRU	R/W	XXXAB		
003А62н	003С62н	DI Consistent	DI CD4	DAM	VVVV		
003А63н	003С63н	DLC register 1	DLCR1	R/W	XXXX _B		
003А64н	003С64н	DI C register 2	DI CDO	DAM	VVVV		
003А65н	003С65н	DLC register 2	DLCR2	R/W	XXXX _B		
003А66н	003С66н	DI C register 2	DI CD2	R/W	VVV-		
003А67н	003С67н	DLC register 3	DLCR3	R/VV	XXXX _B		
003А68н	003С68н	DI C register 4	DI CD4	DAM	VVV-		
003А69н	003С69н	DLC register 4	DLCR4	R/W	XXXX _B		
003А6Ан	003С6Ан	DI C register 5	DI CDE	DAM	VVVV		
003А6Вн	003С6Вн	DLC register 5	DLCR5	R/W	XXXX _B		
003А6Сн	003С6Сн	DLC register 6	DI CDC	R/W	XXXX _B		
003А6Dн	003С6Дн	DLC register 6	DLCR6	R/VV	AAAB		
003А6Ен	003С6Ен	DLC register 7	DLCR7	R/W	XXXX _B		
003А6Fн	003С6Fн	DLC register 7	DLCRI	R/VV	AAAB		
003А70н	003С70н	DI C register 9	DLCR8	R/W	xxxx		
003А71н	003С71н	DLC register 8	DLCRo	R/VV			
003А72н	003С72н	DLC register 9	DLCR9	R/W	XXXX _B		
003А73н	003С73н	DLC register 9	DLCK9	IN/VV			
003А74н	003С74н	DLC register 10	DLCR10	R/W	XXXXB		
003А75н	003С75н	DLC register 10	DLCKTO	IN/VV			
003А76н	003С76н	DLC register 11	DLCR11	R/W	YYYY ₂		
003А77н	003С77н	DEC register 11	DLCKII	IN/VV	XXXX _B		
003А78н	003С78н	DLC register 12	DLCR12	R/W			
003А79н	003С79н	DEG Tegister 12	DEGITIZ	TX/ VV	XXXX _B		
003А7Ан	003С7Ан	DLC register 13	DLCR13	R/W	XXXX _B		
003А7Вн	003С7Вн	— DEO register 13	DLOKIS	13/ 77			
003А7Сн	003С7Сн	DLC register 14	DLCR14	R/W	XXXX _B		
003А7Dн	003С7Дн	DEO register 14	DLON 14	13/ 77			
003А7Ен	003С7Ен	DLC register 15	DLCR15	R/W	XXXX _B		
003А7Fн	003С7Fн	— DEC register 13	DLONTO	IN/ VV	VVVVR		
003А80н	003С80н				XXXXXXXXB		
to 003A87н	to 003С87н	Data register 0 (8 bytes)	DTR0	R/W	to XXXXXXXXB		



- *1 : The interrupt request flag is cleared by the El²OS interrupt clear signal.
- *2 : The interrupt request flag is cleared by the El2OS interrupt clear signal. A stop request is available.

Notes:

- N/A: The interrupt request flag is not cleared by the El²OS interrupt clear signal.
- For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the El²OS interrupt clear signal.
- At the end of El²OS, the El²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the El²OS and in the meantime another interrupt flag is set by a hardware event, the later event is lost because the flag is cleared by the El²OS clear signal caused by the first event. So it is recommended not to use the El²OS for this interrupt number.
- If El²OS is enabled, El²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same El²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the El²OS, the other interrupt should be disabled.

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11. Electrical Characteristics

11.1 Absolute Maximum Ratings

(Vss = AVss = 0.0 V)

Parameter	Cumbal	V	alue	Units	Remarks	
Parameter	Symbol	Min	Max	Units	Remarks	
	Vcc	Vss - 0.3	Vss + 6.0	V		
Power supply voltage	AVcc	Vss - 0.3	Vss + 6.0	V	Vcc = AVcc *1	
Tower supply voltage	AVRH, AVRL	V _{SS} — 0.3	Vss + 6.0	V	AVcc≥ AVRH/AVRL, AVRH≥ AVRL *1	
Input voltage	Vı	$V_{SS} - 0.3$	Vss + 6.0	V	*2	
Output voltage	Vo	$V_{SS} - 0.3$	Vss + 6.0	V	*2	
Maximum clamp current	ICLAMP	- 2.0	+ 2.0	mA	*6	
Total maximum clamp current	Σ ICLAMP	_	20	mA	*6	
"L" level max output current	Іоь	_	15	mA	*3	
"L" level avg. output current	lolav	_	4	mA	*4	
"L" level max overall output current	ΣΙοι	_	100	mA		
"L" level avg. overall output current	Σ lolav	_	50	mA	*5	
"H" level max output current	Іон	_	-15	mA	*3	
"H" level avg. output current	Іонач	_	- 4	mA	*4	
"H" level max overall output current	ΣІон	_	-100	mA		
"H" level avg. overall output current	ΣΙομαν	_	-50	mA	*5	
Dawar canaumation	Pp	_	500	mW	Flash device	
Power consumption	PD	_	400	mW	MASK ROM	
Operating temperature	TA	-40	+105	°C		
Storage temperature	Тѕтс	- 55	+150	°C		

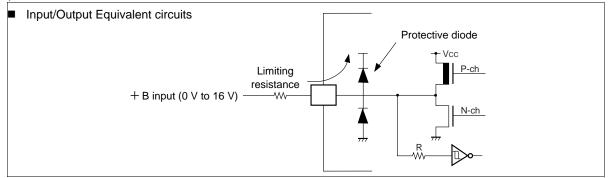
- *1 : AVcc, AVRH, AVRL should not exceed Vcc. Also, AVRH, AVRL should not exceed AVcc, and AVRL does not exceed AVRH.
- *2 : V_I and V_O should not exceed V_{CC} + 0.3 V. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supercedes the V_I rating.
- *3: The maximum output current is a peak value for a corresponding pin.
- *4 : Average output current is an average current value observed for a 100 ms period for a corresponding pin.
- *5 : Total average current is an average current value observed for a 100 ms period for all corresponding pins.

*6

- Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0
- Use within recommended operating conditions.
- □ Use at DC voltage (current).
- □ The + B signal should always be applied with a limiting resistance placed between the + B signal and the microcontroller.
- □ The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- □ Note that when the microcontroller drive current is low, such as in the power saving modes, the + B input potential may pass through the protective diode and increase the potential at the Vcc pin, and this may affect other devices.
- □ Note that if a + B signal is input when the microcontroller current is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- □ Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- □ Care must be taken not to leave the + B input pin open.



- □ Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept + B signal input.
- □ Sample recommended circuits :



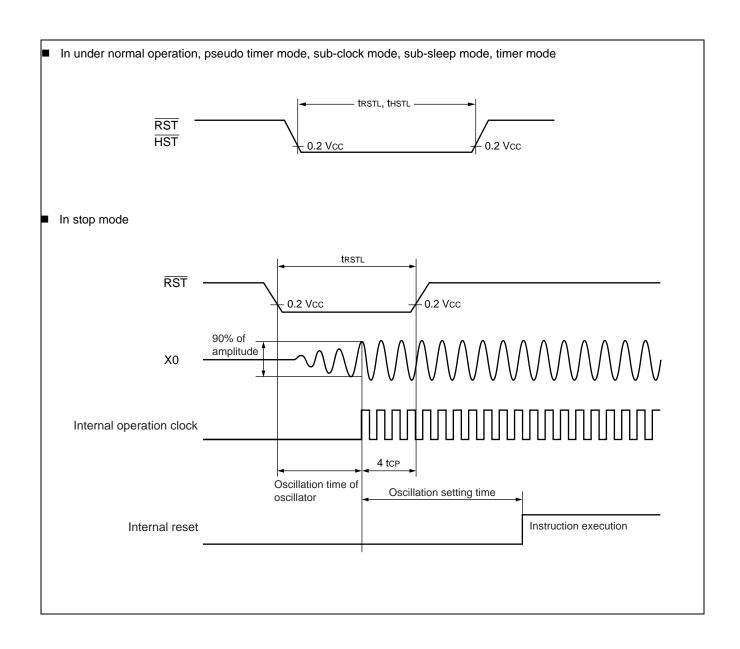
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.



 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } +105 \text{ °C}) \\ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } +105 \text{ °C}) \\ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } +105 \text{ °C}) \\ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } +105 \text{ °C}) \\ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } +105 \text{ °C}) \\ (Other than MB90543G(S)/F548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } +105 \text{ °C}) \\ (Other than MB90543G(S)/F548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } +105 \text{ °C}) \\ (Other than MB90543G(S)/F548G(S)/F5$

Dama wa atau			Value			1114		
Parameter	Symbol	Pin name	Min	Тур	Max	Units	Remarks	
			62.5	_	333	ns	No multiplier When using an oscillator circuit Vcc = 5.0 V ± 10%	
			62.5	_	125	ns	PLL multiplied by 1 When using an oscillator circuit Vcc = 5.0 V ± 10%	
			125	_	250	ns	PLL multiplied by 2 When using an oscillator circuit Vcc = 5.0 V ± 10%	
			187.5	_	333	ns	PLL multiplied by 3 When using an oscillator circuit Vcc = 5.0 V ± 10%	
Clock cycle time	tcyL	X0, X1	250	_	333	ns	PLL multiplied by 4 When using an oscillator circuit Vcc = 5.0 V ± 10%	
Clock cycle time			200	_	333	ns	When using an oscillator circuit Vcc < 4.5 V(MB90F548GL(S)/543G(S)/ 547G(S)/548G(S))	
			62.5	_	333	ns	No multiplier When using an external clock	
			62.5	_	125	ns	PLL multiplied by 1 When using an external clock	
			125	_	250	ns	PLL multiplied by 2 When using an external clock	
			187.5	_	333	ns	PLL multiplied by 3 When using an external clock	
			250	_	333	ns	PLL multiplied by 4 When using an external clock	
	t LCYL	X0A, X1A	_	30.5	_	μs		
Input clock pulse width	Pwh, PwL	X0	10	_	_	ns	Duty ratio is about 30% to 70% .	
mpat clock palse wiath	Pwlh, Pwll	X0A	_	15.2	_	μs	Duty fatio is about 50 / 0 to 70 / 0.	
Input clock rise and fall time	tcr, tcr	X0	_	_	5	ns	When using an external clock	
Machina clask fraguancy	fcp	_	1.5	_	16	MHz	When using main clock	
Machine clock frequency	fLCP	_	_	8.192	_	kHz	When using sub-clock	
Machina clack avala tima	tcp	_	62.5	_	666	ns	When using main clock	
Machine clock cycle time	t LCP	_	_	122.1	_	μs	When using sub-clock	





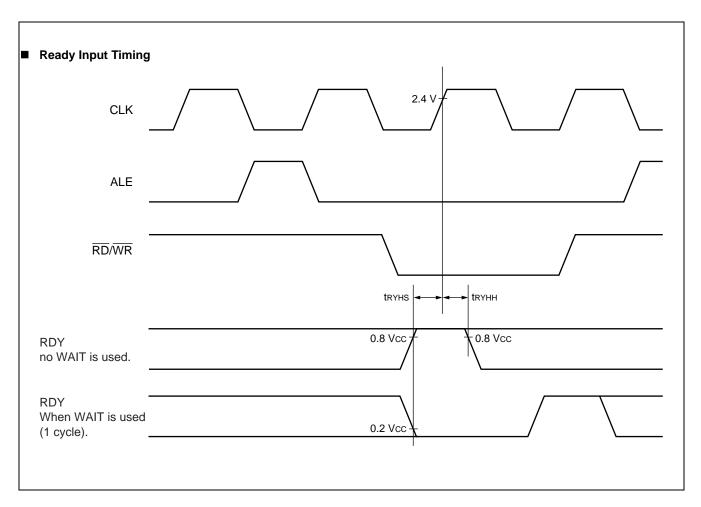


11.4.7 Ready Input Timing

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } + 105 \text{ °C}) \\ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } + 105 \text{ °C}) \\ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } + 105 \text{ °C}) \\ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } + 105 \text{ °C}) \\ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } + 105 \text{ °C}) \\ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } + 105 \text{ °C}) \\ (Other than MB90543G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } + 105 \text{ °C}) \\ (Other than MB90543G(S)/F548G(S$

Parameter	Symbol Pin name		Condition	Val	ue	Units	Remarks
Faranietei	Symbol	Fill Hallie	Condition	Min	Max	Units	Remarks
RDY setup time	tryhs	RDY	_	45	_	ns	
RDY hold time	tкүнн	RDY		0	_	ns	

Note: If the RDY setup time is insufficient, use the auto-ready function.

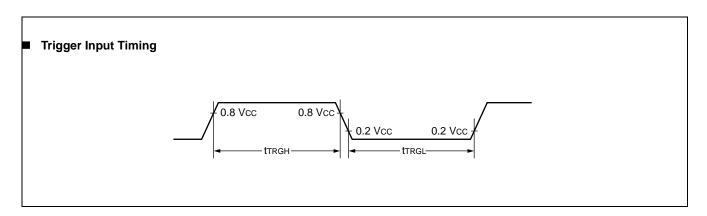




11.4.12 Trigger Input Timing

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } + 105 \text{ °C}) \\ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } + 105 \text{ °C}) \\ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } + 105 \text{ °C}) \\ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } + 105 \text{ °C}) \\ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } + 105 \text{ °C}) \\ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } + 105 \text{ °C}) \\ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = \text{AV}_{SS} = 0.0 \text{ V}, T_{A} = -40 \text{ °C to } + 105 \text{ °C}) \\ (Other than MB90543G(S)/548G(S)/F548G(S)/$

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks			
raiailletei	Symbol	Fili lialile	Condition	Min Max		Units	Remarks			
Input pulse width	t TRGH	INT0 to INT7,		5 tcp	_	ns	Under nomal operation			
input puise wiatri	t TRGL	ADTG	_	_	_	_	1	_	μs	In stop mode





11.5.2 A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point ("00 0000 0000" ←→ "00 0000

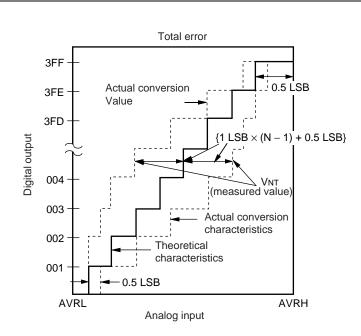
0001") with the full-scale transition point ("11 1111 1110" \longleftrightarrow "11 1111 1111") from actual conversion

characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which

includes zero-transition error/full-scale transition error and linearity error.



1 LSB = (Theoretical value)
$$\frac{AVRH - AVRL}{1024}$$
 [V]

Vot (Theoretical value) = AVRL + 0.5 LSB [V]

 V_{FST} (Theoretical value) = AVRH - 1.5 LSB [V]

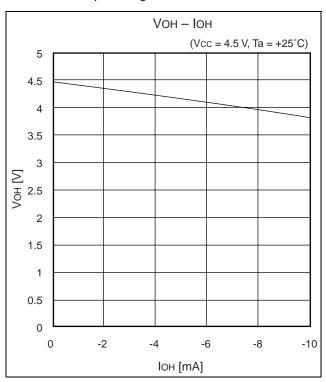
Total error for digital output N =
$$\frac{V_{NT} - \{1 \text{ LSB} \times (N-1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}}$$
 [LSB]

 V_{NT} : Voltage at a transition of digital output from (N-1) to N

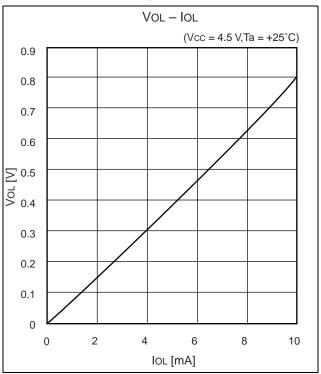


12. Example Characteristics

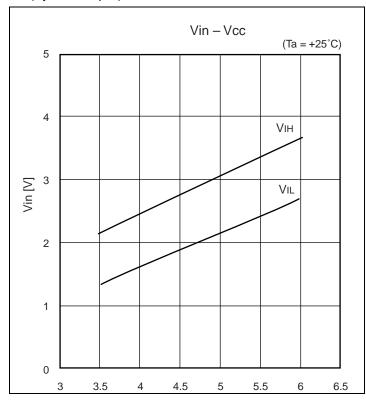
■ "H" level output voltage



■ "L" level output voltage

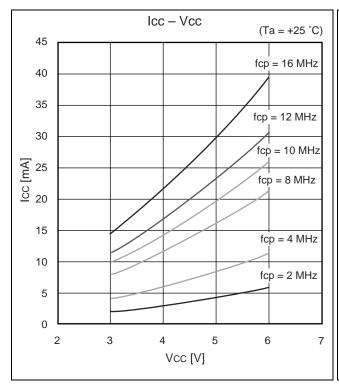


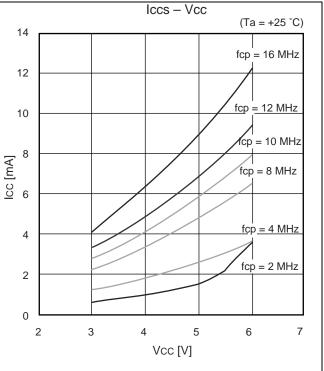
"H" level input voltage/ "L" level input voltage (Hysterisis inpiut)

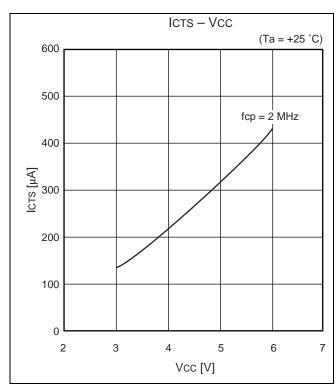


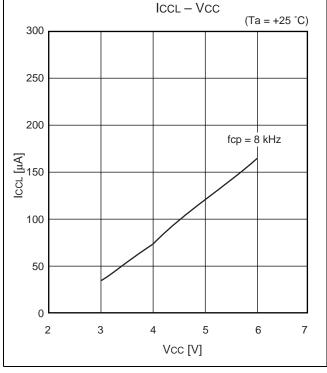


■ Power supply current (MB90F549G)



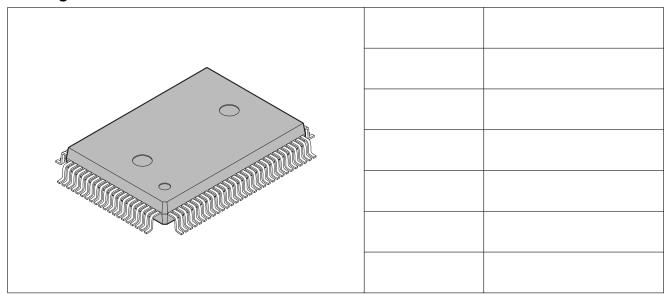


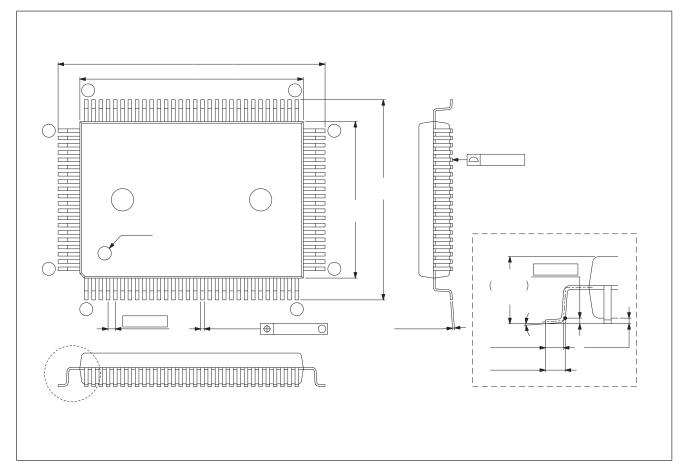






14. Package Dimensions







15. Major Changes

Spansion Publication Number: DS07-13703-7E

Section	Change Results
■ PRODUCT LINEUP	Changed the name in peripheral resource. 16-bit I/O Timer → 16-bit Free-run Timer
■ I/O CIRCUIT TYPE	Changed the name of input typ. Hysteresis → CMOS Hysteresis HYS → CMOS Hysteresis
■ BLOCK DIAGRAM	Changed the arrow direction of SOT1 signal at UART1(SCI). " \leftarrow \rightarrow " (input/output) \rightarrow " \leftarrow " (output)
■ I/O MAP	Changed the text of "Note".
■ INTERRUPT MAP	Changed the name of peripheral resource of the pin number: #19. I/O Timer → 16-bit Free-run Timer
■ ELECTRICAL CHARACTERISTICS 2. Recommended Conditions	Changed the remarks of "parameter: Power supply voltage".
3. DC Characteristics	Changed the maximum value of symbol : VILM of parameter: Input voltage. Vcc + 0.3 \rightarrow Vss + 0.3
	Added the following remarks for parameter : Pull-down resistance. Except Flash device
AC Characteristics Clock Timing	Added the value when using an external clock in Oscillation frequency and Clock cycle time on (1) Clock Timing for parameter.
	Added the item of A/D converter operation range in figure of "■ Guaranteed PLL operation range"
(3) Reset and Hardware Standby Input Timing	Changed the following item. (3) Reset and Hardware Standby Input Timing Remarks: In sub-clock mode, sub-sleep mode, timer mode 2tcp → 2tlcp
(4) Power On Reset	Changed as follows; Due to repetitive operation → Waiting time until power-on
5. A/D Converter	Changed the unit of Zero transition voltage and Full scale transition voltage. $mV \rightarrow V$
■ ORDERING INFORMATION	Added the MB90F548GLPMC in Part Numbers.

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: MB90F543G(S)/546G(S)/548G(S)/549G(S)/549G(S)/V540G/MB90543G(S)/547G(S)/548G(S)/F548GL(S) CMOS F2MC-16LX MB90540G/545G Series 16-bit Proprietary Microcontroller Document Number: 002-07696					
Revision	ECN	Orig. of Change	Submission Date	Description of Change	
**	_	AKIH	11/13/2008	Migrated to Cypress and assigned document number 002-07696. No change to document contents or format.	
*A	5537115	AKIH	11/30/2016	Updated to Cypress template	

Document Number: 002- 07696 Rev. *A Page 69 of 70



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