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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

| Product Status             | Active   |
|----------------------------|--|
| Core Processor             | F <sup>2</sup> MC-16LX   |
| Core Size                  | 16-Bit   |
| Speed                      | 16MHz  |
| Connectivity               | CANbus, EBI/EMI, SCI, Serial I/O, UART/USART                                 |
| Peripherals                | POR, WDT   |
| Number of I/O              | 81   |
| Program Memory Size        | 128KB (128K x 8)   |
| Program Memory Type        | FLASH  |
| EEPROM Size                | <u>.</u>   |
| RAM Size                   | 6K x 8   |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V  |
| Data Converters            | A/D 8x8/10b  |
| Oscillator Type            | External   |
| Operating Temperature      | -40°C ~ 105°C (TA)   |
| Mounting Type              | Surface Mount  |
| Package / Case             | 100-BQFP   |
| Supplier Device Package    | 100-QFP (14x20)  |
| Purchase URL               | https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspf-gse1 |

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| MB90F543G (S) /F548G (S)<br>MB90F549G (S) /F546G (S)<br>MB90F548GL(S)   | MB90543G (S)<br>MB90547G (S)<br>MB90548G (S)<br>MB90549G (S)   | MB90V540G  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|
| Operation clock frequency : fsys/21,  | fsys/2 <sup>3</sup> , fsys/2 <sup>5</sup> (fsys = System clock   | frequency)   |  |  |  |  |  |  |  |
| Supports External Event Count func  | tion   |  |  |  |  |  |  |  |  |
| Signals an interrupt when overflow  |  |  |  |  |  |  |  |  |  |
| Supports Timer Clear when a match   | with Output Compare (Channel 0)  |  |  |  |  |  |  |  |  |
| Operation clock freq. : fsys/2 <sup>2</sup> , fsys/2 <sup>4</sup> , fsys/2 <sup>6</sup> , fsys/2 <sup>8</sup> (fsys = System clock freq.) |  |  |  |  |  |  |  |  |  |
| Signals an interrupt when a match w   | rith 16-bit Free-run Timer   |  |  |  |  |  |  |  |  |
| Four 16-bit compare registers   |  |  |  |  |  |  |  |  |  |
| A pair of compare registers can be u  | sed to generate an output signal   |  |  |  |  |  |  |  |  |
| Rising edge, falling edge or rising &   | falling edge sensitive   |  |  |  |  |  |  |  |  |
| Four 16-bit Capture registers   |  |  |  |  |  |  |  |  |  |
| Signals an interrupt upon external e  | vent   |  |  |  |  |  |  |  |  |
| Supports 8-bit and 16-bit operation r   | nodes  |  |  |  |  |  |  |  |  |
| Eight 8-bit reload counters   |  |  |  |  |  |  |  |  |  |
| Eight 8-bit reload registers for L puls   | e width  |  |  |  |  |  |  |  |  |
| Eight 8-bit reload registers for H puls   | se width   |  |  |  |  |  |  |  |  |
|   |  | unter or as 8-bit prescaler plus 8-bit   |  |  |  |  |  |  |  |
| reload counter  | -  |  |  |  |  |  |  |  |  |
| 4 output pins   |  |  |  |  |  |  |  |  |  |
| Operation clock freq. : fsys, fsys/2 <sup>1</sup> ,   | fsys/2², fsys/2³, fsys/2⁴ or 128 μs@fc   | sc = 4 MHz   |  |  |  |  |  |  |  |
| (fsys = System clock frequency, for   | sc = Oscillation clock frequency)  |  |  |  |  |  |  |  |  |
| Conforms to CAN Specification Vers  | ion 2.0 Part A and B   |  |  |  |  |  |  |  |  |
| Automatic re-transmission in case of  | ferror   |  |  |  |  |  |  |  |  |
| Automatic transmission responding   | to Remote Frame  |  |  |  |  |  |  |  |  |
| Prioritized 16 massage buffers for da   | ata and ID's supports multipe massag   | ges  |  |  |  |  |  |  |  |
| Flexible configuration of acceptance  | filtering :  |  |  |  |  |  |  |  |  |
| Full bit compare/Full bit mask/Two p  | artial bit masks   |  |  |  |  |  |  |  |  |
| Supports up to 1 Mbps   |  |  |  |  |  |  |  |  |  |
| Sub-clock for low power operation   |  |  |  |  |  |  |  |  |  |
| Can be programmed edge sensitive  | or level sensitive   |  |  |  |  |  |  |  |  |
| External access using the selectable  | e 8-bit or 16-bit bus is enabled   |  |  |  |  |  |  |  |  |
| (external bus mode.)  |  |  |  |  |  |  |  |  |  |
| Virtually all external pins can be use  | d as general purpose I/O   |  |  |  |  |  |  |  |  |
| All push-pull outputs and schmitt trig  | ger inputs   |  |  |  |  |  |  |  |  |
| Bit-wise programmable as input/outp   | out or peripheral signal   |  |  |  |  |  |  |  |  |
| Sub-clock for 32 kHz Sub clock low  | power operation  |  |  |  |  |  |  |  |  |
| Supports automatic programming, E   | mbeded Algorithm   |  |  |  |  |  |  |  |  |
| Write/Erase/Erase-Suspend/Erase-F   | Resume commands  |  |  |  |  |  |  |  |  |
|   |  |  |  |  |  |  |  |  |  |
|   |  |  |  |  |  |  |  |  |  |
|   |  |  |  |  |  |  |  |  |  |
|   |  |  |  |  |  |  |  |  |  |
| Boot block configuration<br>Erase can be performed on each block  |  |  |  |  |  |  |  |  |  |
| Liase can be penornied on each bid  |  |  |  |  |  |  |  |  |  |
|   | MB90F549G (S) /F546G (S)<br>MB90F548GL(S)<br>Operation clock frequency : fsys/2 <sup>1</sup> ,<br>Supports External Event Count funct<br>Signals an interrupt when overflow<br>Supports Timer Clear when a match<br>Operation clock freq. : fsys/2 <sup>2</sup> , fsys/2<br>Signals an interrupt when a match w<br>Four 16-bit compare registers<br>A pair of compare registers can be u<br>Rising edge, falling edge or rising &<br>Four 16-bit Capture registers<br>Signals an interrupt upon external even<br>Supports 8-bit and 16-bit operation r<br>Eight 8-bit reload counters<br>Eight 8-bit reload registers for L puls<br>Eight 8-bit reload registers for L puls<br>Eight 8-bit reload counters can be<br>reload counter<br>4 output pins<br>Operation clock freq. : fsys, fsys/2 <sup>1</sup> , f<br>(fsys = System clock frequency, fos<br>Conforms to CAN Specification Vers<br>Automatic re-transmission in case of<br>Automatic transmission responding f<br>Prioritized 16 massage buffers for da<br>Flexible configuration of acceptance<br>Full bit compare/Full bit mask/Two p<br>Supports up to 1 Mbps<br>Sub-clock for low power operation<br>Can be programmed edge sensitive<br>External access using the selectable<br>(external bus mode.)<br>Virtually all external pins can be use<br>All push-pull outputs and schmitt trig<br>Bit-wise programmable as input/outp<br>Sub-clock for 32 kHz Sub clock low<br>Supports automatic programming, E<br>Write/Erase/Erase-Suspend/Erase-F<br>A flag indicating completion of the al<br>Number of erase cycles : 10,000 tim<br>Data retention time : 10 years<br>Boot block configuration | MB90F349G (S) //F340G (S)<br>MB90548G (S)         MB90548G (S)<br>MB90548G (S)           Operation clock frequency : fsys/2 <sup>1</sup> , fsys/2 <sup>3</sup> , fsys/2 <sup>5</sup> (fsys = System clock<br>Supports External Event Count function<br>Signals an interrupt when overflow           Supports Timer Clear when a match with Output Compare (Channel 0)<br>Operation clock freq. : fsys/2 <sup>2</sup> , fsys/2 <sup>6</sup> , fsys/2 <sup>6</sup> (fsys = System clock<br>Signals an interrupt when a match with 16-bit Free-run Timer<br>Four 16-bit compare registers           A pair of compare registers         A pair of compare registers           Signals an interrupt upon external event         Supports 8-bit and 16-bit operation modes           Eight 8-bit reload counters         Eight 8-bit reload registers for L pulse width           Supports 10 clock freq. : fsys, fsys/2 <sup>1</sup> , fsys/2 <sup>2</sup> , fsys/2 <sup>3</sup> , fsys/2 <sup>4</sup> or 128 µs@fc<br>(fsys = System clock frequency, fosc = Oscillation clock frequency)           Conforms to CAN Specification Version 2.0 Part A and B           Automatic re-transmission in case of error           Automatic re-transmission is case of error           Automatic ransmission responding to Remote Frame           Prioritized 16 massage buffers for data and ID's supports multipe massa           Flexible configuration of acceptance filtering :           Full bit compare/Full bit mask/Two partial bit masks           Supports up to 1 Mbps           Sub-clock for 32 kHz Sub clock low power operation           Can be programmed edge sensitive or level sensitive           External access using the sele |  |  |  |  |  |  |  |

\*1 : If the one clock system is used, equip X0A and X1A with clocks from the tool side.



| No.   | Din namo  |  | Function   |  |  |  |  |
|-------|---|--|--|--|--|--|--|
| QFP*1 | Finnanie  | Circuit type   | Function   |  |  |  |  |
|       | P33   |  | General I/O port with programmable pullup. This f <u>unction is enabled in the single-chip mode, external bus 8-bit mode or when WRH pin output is disabled.</u>   |  |  |  |  |
| 13    | WRH   | Ĩ  | Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the WRH output pin is enabled.   |  |  |  |  |
| 14    | P34   |  | General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.   |  |  |  |  |
| 14    | HRQ   |  | Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.  |  |  |  |  |
| 15    | P35   |  | General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.   |  |  |  |  |
| 15    | HAK   |  | Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.   |  |  |  |  |
| 16    | P36   |  | General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.   |  |  |  |  |
| RDY   |   |  | Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.   |  |  |  |  |
| 17    | P37   | Ц  | General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the CLK output is disabled.  |  |  |  |  |
| 17    | CLK   |  | CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled.   |  |  |  |  |
| 10    | P40   | 6  | General I/O port. This function is enabled when UART0 disables the serial data output.   |  |  |  |  |
| 10    | SOT0  | G  | Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.  |  |  |  |  |
| 10    | P41   | G  | General I/O port. This function is enabled when UART0 disables serial clock output.  |  |  |  |  |
| 19    | SCK0  |  | Serial clock I/O pin for UART0. This function is enabled when UART0 enables the serial clock output.   |  |  |  |  |
|       | P42   |  | General I/O port. This function is always enabled.   |  |  |  |  |
| 20    | SINO  | G  | Serial data input pin for UART0. Set the corresponding Port<br>Direction Register to input if this function is used.   |  |  |  |  |
|       | P43   |  | General I/O port. This function is always enabled.   |  |  |  |  |
| 21    | SIN1  | G  | Serial data input pin for UART1. Set the corresponding Port<br>Direction Register to input if this function is used.   |  |  |  |  |
|       | QFP"1         13         14         15         16         17         18         19         20 | Pin name           QFP"1         P33           13         P33           13         WRH           14         P34           14         P35           15         HAR           16         P36           17         P37           17         CLK           18         P40           19         P41           20         P42           21         P43 | Pin name         Circuit type           QFP'1         P33         []           13         P33         []           13         WRH         []           13         WRH         []           14         P34         []           14         P34         []           14         P34         []           15         P35         []           15         P35         []           16         P36         []           RDY         []         []           16         RDY         []           17         P37         []           18         P40         []           19         P40         []           19         P41         []           20         P41         []           21         P43         [] |  |  |  |  |

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### (6) Pull-up/down resistors

The MB90540G/545G Series does not support internal pull-up/down resistors (except Port0 – Port3 : pull-up resistors) . Use external components where needed.

#### (7) Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via the shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuits do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation.

### (8) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AVcc, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (Vcc).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AVcc (turning on/off the analog and digital power supplies simultaneously is acceptable).

### (9) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to  $AV_{CC} = V_{CC}$ ,  $AV_{SS} = AVRH = V_{SS}$ .

### (10) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

#### (11) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50  $\mu$ s or more (0.2 V to 2.7 V).

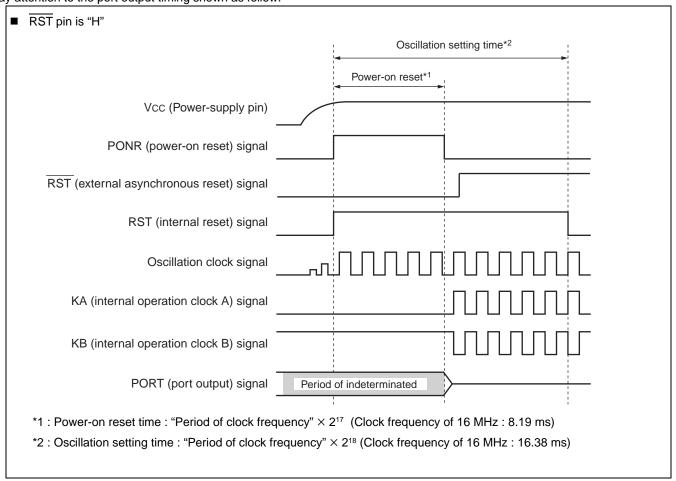


### (12) Indeterminate outputs from ports 0 and 1 (MB90V540G only)

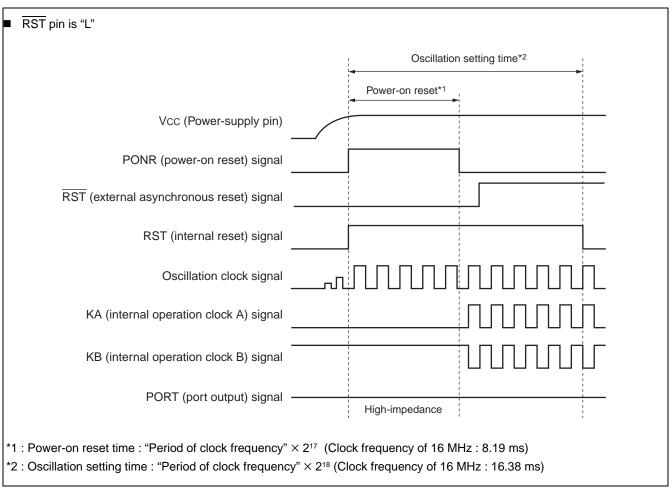
During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

■ If RST pin is "H", the outputs become indeterminate.

■ If RST pin is "L", the outputs become high-impedance. Pay attention to the port output timing shown as follow.







### (13) Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

#### (14) Directions of "DIV A, Ri" and "DIVW A, RWi" instructions

In the Signed multiplication and division instructions ("DIV A, Ri" and "DIVW A, RWi"), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in "00H".

If the values of the corresponding bank registers (DTB, ADB, USB, SSB) are set to other than "00H", the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

### (15) Using REALOS

The use of El<sup>2</sup>OS is not possible with the REALOS real time operating system.

#### (16) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.



| Address         | Register   | Abbreviation | Access | Resource name                          | Initial value                |
|-----------------|--|--------------|--------|--|------------------------------|
| 47н to 4Вн      | Prohibited   |              | •      |  |                              |
| 4Сн             | Input capture control status register 0/1            | ICS01        | R/W    | Input Capture 0/1                      | 00000000                     |
| 4DH             | Input capture control status register 2/3            | ICS23        | R/W    | Input Capture 2/3                      | 00000000                     |
| 4Eн             | Input capture control status register 4/5            | ICS45        | R/W    | Input Capture 4/5                      | 00000000                     |
| 4F <sub>H</sub> | Input capture control status register 6/7            | ICS67        | R/W    | Input Capture 6/7                      | 00000000                     |
| 50н             | Timer control status register 0                      | TMCSR0       | R/W    |  | 00000000                     |
| 51н             | Timer control status register 0                      | TMCSR0       | R/W    |  | 0000в                        |
| 52н             | Timer register 0/reload register 0                   | TMR0/TMRLR0  | R/W    | 16-bit Reload Timer 0                  | XXXXXXXAB                    |
| 53н             | Timer register 0/reload register 0                   | TMR0/TMRLR0  | R/W    | -                                      | XXXXXXXXB                    |
| 54н             | Timer control status register 1                      | TMCSR1       | R/W    |  | 00000000                     |
| 55н             | Timer control status register 1                      | TMCSR1       | R/W    | 16-bit Reload Timer 1                  | 0000в                        |
| 56н             | Timer register 1/reload register 1                   | TMR1/TMRLR1  | R/W    | To-bit Reload Timer T                  | XXXXXXXAB                    |
| 57н             | Timer register 1/reload register 1                   | TMR1/TMRLR1  | R/W    |  | XXXXXXXAB                    |
| 58н             | Output compare control status register 0             | OCS0         | R/W    | Output Compose 0/1                     | 000000в                      |
| 59н             | Output compare control status register 1             | OCS1         | R/W    | Output Compare 0/1                     | 00000в                       |
| 5Ан             | Output compare control status register 2             | OCS2         | R/W    | 0.1                                    | 000000в                      |
| 5Вн             | Output compare control status register 3             | OCS3         | R/W    | Output Compare 2/3                     | 00000 <sub>B</sub>           |
| 5Cн to 6Bн      | Prohibited   |              |        |  | •                            |
| 6Сн             | Timer Data register                                  | TCDT         | R/W    |  | 00000000                     |
| 6Dн             | Timer Data register                                  | TCDT         | R/W    | I/O Timer                              | 00000000                     |
| 6Ен             | Timer Control register                               | TCCS         | R/W    | -                                      | 00000000                     |
| 6Fн             | ROM mirror function selection register               | ROMM         | R/W    | ROM Mirror                             | 1в                           |
| 70н to 7Fн      | Reserved for CAN 0 Interface.                        |              |        |  | •                            |
| 80н to 8Fн      | Reserved for CAN 1 Interface.                        |              |        |  |                              |
| 90н to 9Dн      | Prohibited   |              |        |  |                              |
| 9Ен             | Program address detection<br>control status register | PACSR        | R/W    | Address Match<br>Detection<br>Function | 000000000                    |
| 9Fн             | Delayed interrupt/release register                   | DIRR         | R/W    | Delayed Interrupt                      | 0в                           |
| АОн             | Low-power mode control register                      | LPMCR        | R/W    | Low Power<br>Controller                | 0 0 0 1 1 0 0 0 <sub>B</sub> |
| А1н             | Clock selection register                             | CKSCR        | R/W    | Low Power<br>Controller                | 1111100 <sub>B</sub>         |

# MB90540G/545G Series



(Continued)

| Address        | Register                      | Abbreviation | Access | Resource name      | Initial value |
|----------------|-------------------------------|--------------|--------|--------------------|---------------|
| 3928н          | Output Compare Register 0     | OCCP0        | R/W    |                    | XXXXXXXXB     |
| 3929н          | Output Compare Register 0     | OCCP0        | R/W    | Output Compare 0/1 | XXXXXXXXB     |
| 392Ан          | Output Compare Register 1     | OCCP1        | R/W    | Output Compare 0/1 | XXXXXXXXB     |
| 392Вн          | Output Compare Register 1     | OCCP1        | R/W    |                    | XXXXXXXXB     |
| 392Сн          | Output Compare Register 2     | OCCP2        | R/W    |                    | XXXXXXXXB     |
| 392Dн          | Output Compare Register 2     | OCCP2        | R/W    | Output Compore 2/2 | XXXXXXXXB     |
| 392Ен          | Output Compare Register 3     | OCCP3        | R/W    | Output Compare 2/3 | XXXXXXXXB     |
| 392Fн          | Output Compare Register 3     | OCCP3        | R/W    |                    | XXXXXXXXB     |
| 3930н to 39FFн | Reserved                      |              |        | ·                  |               |
| 3A00H to 3AFFH | Reserved for CAN 0 Interface. |              |        |                    |               |
| 3B00н to 3BFFн | Reserved for CAN 0 Interface. |              |        |                    |               |
| 3C00н to 3CFFн | Reserved for CAN 1 Interface. |              |        |                    |               |
| 3D00н to 3DFFн | Reserved for CAN 1 Interface. |              |        |                    |               |
| 3E00н to 3FFFн | Reserved                      |              |        |                    |               |

- Read/write notation
  - R/W : Reading and writing permitted
  - R : Read-only
  - W : Write-only

### Initial value notation

- 0 : Initial value is "0".
- 1 : Initial value is "1".
- X : Initial value is undefined.
- \_ : Initial value is unused.

Note: Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading "X".



### List of Message Buffers (DLC Registers and Data Registers)

| Ad              | Idress              | <b>B</b> 14               |              |        |                   |  |  |
|-----------------|---------------------|---------------------------|--------------|--------|-------------------|--|--|
| CAN0            | CAN1                | Register                  | Abbreviation | Access | Initial Value     |  |  |
| 003A60н         | 003C60н             |                           | DI CDO       | DAA    |                   |  |  |
| 003A61н         | 003C61н             | – DLC register 0          | DLCR0        | R/W    | XXXXB             |  |  |
| 003А62н         | 003C62н             |                           | DI CD4       | DAA    |                   |  |  |
| 003A63н         | 003C63н             | DLC register 1            | DLCR1        | R/W    | XXXXB             |  |  |
| 003A64н         | 003C64 <sub>H</sub> |                           | DI CD2       | DAA    |                   |  |  |
| 003А65н         | 003C65н             | DLC register 2            | DLCR2        | R/W    | XXXX <sub>B</sub> |  |  |
| 003А66н         | 003C66н             |                           |              | DAM    | ~~~~              |  |  |
| <b>003А67</b> н | 003C67н             | DLC register 3            | DLCR3        | R/W    | XXXXB             |  |  |
| 003A68н         | 003C68н             |                           |              | DAM    | ~~~~              |  |  |
| 003A69н         | 003C69н             | DLC register 4            | DLCR4        | R/W    | XXXX <sub>B</sub> |  |  |
| 003А6Ан         | 003С6Ан             | DL C register 5           |              | DAM    | ~~~~              |  |  |
| 003А6Вн         | 003С6Вн             | DLC register 5            | DLCR5        | R/W    | XXXXB             |  |  |
| 003А6Сн         | 003С6Сн             |                           |              | R/W    | XXXXB             |  |  |
| 003A6Dн         | 003C6DH             | DLC register 6            | DLCR6        | R/VV   |                   |  |  |
| 003А6Ен         | 003C6Eн             | DI C register 7           | DLCR7        | R/W    | XXXX <sub>B</sub> |  |  |
| 003A6Fн         | 003C6Fн             | DLC register 7            | DLCR7        | R/VV   |                   |  |  |
| 003А70н         | 003С70н             | DI C register 9           | DLCR8        | R/W    | XXXX              |  |  |
| 003A71н         | 003C71н             | DLC register 8            | DLCRO        | R/VV   |                   |  |  |
| 003А72н         | 003С72н             | DI C register 0           | DLCR9        | R/W    | XXXXB             |  |  |
| 003А73н         | 003С73н             | DLC register 9            | DLCR9        | r///   |                   |  |  |
| 003A74н         | 003C74н             | DLC register 10           | DLCR10       | R/W    | XXXXB             |  |  |
| 003A75н         | 003C75н             |                           | DECKTO       | N/ W   |                   |  |  |
| 003А76н         | 003C76н             | DLC register 11           | DLCR11       | R/W    | XXXXB             |  |  |
| 003A77н         | 003C77н             |                           | DECKTI       | N/ W   |                   |  |  |
| 003A78н         | 003C78н             | DLC register 12           | DLCR12       | R/W    | XXXX <sub>B</sub> |  |  |
| 003A79н         | 003C79н             | DLC register 12           | DEGITIZ      | 1.7.00 |                   |  |  |
| 003А7Ан         | 003С7Ан             | DLC register 13           | DLCR13       | R/W    | XXXXB             |  |  |
| 003A7Bн         | 003C7Bн             |                           | DECKIS       | N/ W   |                   |  |  |
| 003A7Cн         | 003C7Cн             | DI C register 14          | DLCR14       | R/W    | XXXXB             |  |  |
| 003A7DH         | 003C7Dн             | DLC register 14           | DLON 14      |        |                   |  |  |
| 003A7Eн         | 003C7Eн             | – DLC register 15         | DLCR15       | R/W    | XXXXB             |  |  |
| 003A7Fн         | 003C7Fн             |                           | DLORIG       | 1.7.00 | ////              |  |  |
| 003А80н         | 003С80н             |                           |              |        | XXXXXXXB          |  |  |
| to<br>003А87н   | to<br>003C87н       | Data register 0 (8 bytes) | DTR0         | R/W    | to<br>XXXXXXXXB   |  |  |

\_\_\_\_\_



 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V \text{ to } 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ °C to } +105 \text{ °C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V\_{CC} = 5.0 V ± 10\%, V\_{SS} = AV\_{SS} = 0.0 V, T\_A = -40 \text{ °C to } +105 \text{ °C})

| Deveneter         | Sym-  | n-<br>Pin name | Condition  |     | Value |      | Units | Demente                             |
|-------------------|---|----------------|--|-----|-------|------|-------|-------------------------------------|
| Parameter         | bol   | Pin name       | Condition  | Min | Тур   | Max  | Units | Remarks                             |
|                   | lcc   |                | Internal frequency : 16 MHz, At normal operating                       | _   | 40    | 55   | mA    |                                     |
|                   | ICC   |                | Internal frequency : 16 MHz, At<br>Flash programming/erasing           | -   | 50    | 70   | mA    | Flash device                        |
|                   | Iccs  |                | Internal frequency : 16 MHz, At sleep mode                             | _   | 12    | 20   | mA    |                                     |
|                   |   |                | $V_{cc} = 5.0 \text{ V} \pm 10\%$                                      | -   | 300   | 600  | μΑ    |                                     |
|                   | Icts  |                |  | —   | 600   | 1100 | μΑ    | MB90F548GL (S) only                 |
| Power             | ICIS  |                | Internal frequency : 2 MHz,<br>At pseudo timer mode                    | -   | 200   | 400  | μΑ    | MB90543G(S)/547G(S)/<br>548(S) only |
| supply            |   | Vcc            | Internal frequency : 8 kHz,<br>At sub operation, $T_A = 25 \ ^\circ C$ | —   | 400   | 750  | μΑ    | MB90F548GL only                     |
| current*          | ICCL  |                |  | —   | 50    | 100  | μΑ    | MASK ROM                            |
|                   |   |                |  | —   | 150   | 300  | μΑ    | Flash device                        |
|                   | Iccls   |                | Internal frequency : 8 kHz,<br>At sub sleep, $T_A = 25 \text{ °C}$     | -   | 15    | 40   | μΑ    |                                     |
|                   | Ісст  |                | Internal frequency : 8 kHz,<br>At timer mode, $T_A = 25 \text{ °C}$    | -   | 7     | 25   | μΑ    |                                     |
|                   | Іссн1   |                | At stop, $T_A = 25 \ ^\circ C$   | —   | 5     | 20   | μΑ    |                                     |
|                   | Іссн2   |                | At hardware standby mode, $T_A = 25 \text{ °C}$                        | -   | 50    | 100  | μΑ    |                                     |
| Input<br>capacity | Other than<br>AVcc, AVss,<br>C⊪ AVRH, –<br>AVRL, C,<br>Vcc, Vss |                | _  | 5   | 15    | pF   |       |                                     |

\* : The power supply current testing conditions are when using the external clock.



### **11.4 AC Characteristics**

### 11.4.1 Clock Timing

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V \text{ to } 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V\_{CC} = 5.0 V ± 10\%, V\_{SS} = AV\_{SS} = 0.0 V, T\_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C})

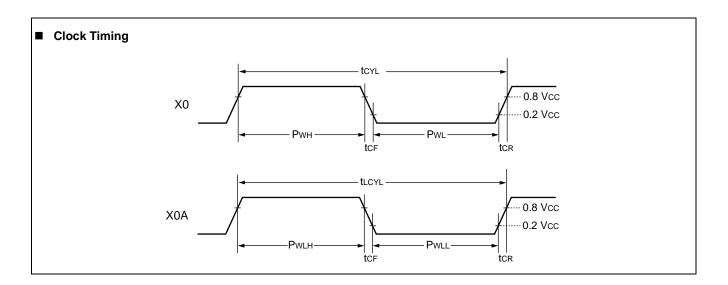
| Parameter             | Symbol | Pin name  |     | Value  |      | Units | Remarks  |   |      |     |  |
|-----------------------|--------|-----------|-----|--------|------|-------|--|---|------|-----|--|
| Falameter             | Symbol | r in name | Min | Тур    | Max  | Units | Remarks  |   |      |     |  |
|                       |        |           | 3   | _      | 16   | MHz   | No multiplier<br>When using an oscillator circuit<br>$V_{cc} = 5.0 \text{ V} \pm 10\%$     |   |      |     |  |
|                       |        |           | 8   | _      | 16   | MHz   | PLL multiplied by 1<br>When using an oscillator circuit<br>$V_{cc} = 5.0 V \pm 10\%$       |   |      |     |  |
|                       |        |           | 4   | _      | 8    | MHz   | PLL multiplied by 2<br>When using an oscillator circuit<br>$V_{cc} = 5.0 V \pm 10\%$       |   |      |     |  |
|                       | fc     |           |     |        |      | 3     | 3  | _ | 5.33 | MHz | PLL multiplied by 3<br>When using an oscillator circuit<br>$V_{cc} = 5.0 V \pm 10\%$ |
| Oscillation frequency |        | X0, X1    | 3   | _      | 4    | MHz   | PLL multiplied by 4<br>When using an oscillator circuit<br>$V_{cc} = 5.0 V \pm 10\%$       |   |      |     |  |
|                       |        |           | 3   | _      | 5    | MHz   | When using an oscillator circuit<br>Vcc < 4.5 V(MB90F548GL(S)/543G(S)/<br>547G(S)/548G(S)) |   |      |     |  |
|                       |        |           | 3   | _      | 16   | MHz   | No multiplier<br>When using an external clock  |   |      |     |  |
|                       |        |           | 8   | _      | 16   | MHz   | PLL multiplied by 1<br>When using an external clock  |   |      |     |  |
|                       |        |           | 4   | _      | 8    | MHz   | PLL multiplied by 2<br>When using an external clock  |   |      |     |  |
|                       |        |           | 3   | _      | 5.33 | MHz   | PLL multiplied by 3<br>When using an external clock  |   |      |     |  |
|                       |        |           | 3   | _      | 4    | MHz   | PLL multiplied by 4<br>When using an external clock  |   |      |     |  |
|                       | fc∟    | X0A, X1A  | —   | 32.768 | -    | kHz   |  |   |      |     |  |

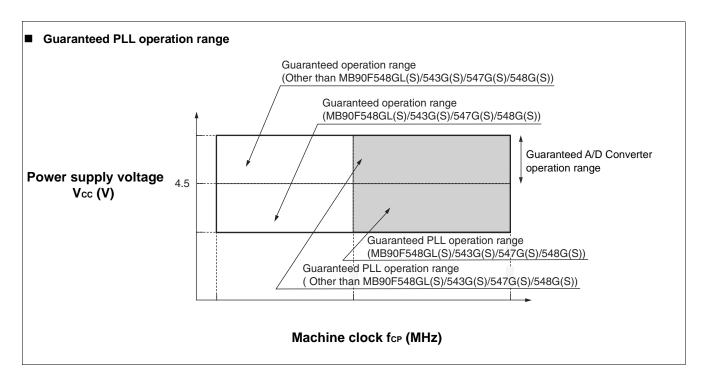


 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V \text{ to } 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ }^{\circ}\text{C} \text{ to } +105 \text{ }^{\circ}\text{C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V\_{CC} = 5.0 V ± 10\%, V\_{SS} = AV\_{SS} = 0.0 V, T\_A = -40 \text{ }^{\circ}\text{C} \text{ to } +105 \text{ }^{\circ}\text{C})

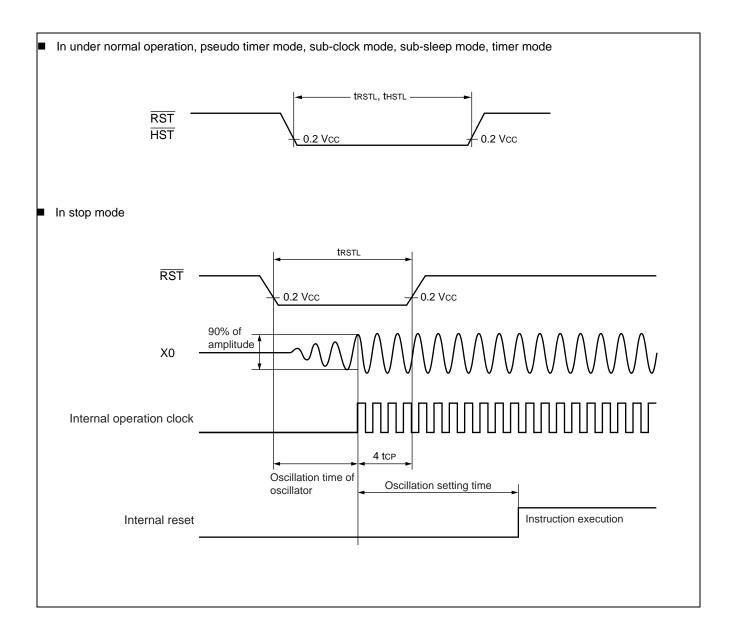
| <b>B</b>                       |               |          |       | Value |     |       | - ·  |
|--------------------------------|---------------|----------|-------|-------|-----|-------|--|
| Parameter                      | Symbol        | Pin name | Min   | Тур   | Max | Units | Remarks  |
|                                |               |          | 62.5  | _     | 333 | ns    | No multiplier<br>When using an oscillator circuit<br>$V_{cc} = 5.0 V \pm 10\%$             |
|                                |               |          | 62.5  | _     | 125 | ns    | PLL multiplied by 1<br>When using an oscillator circuit<br>$V_{cc} = 5.0 V \pm 10\%$       |
|                                |               |          | 125   | _     | 250 | ns    | PLL multiplied by 2<br>When using an oscillator circuit<br>$V_{cc} = 5.0 V \pm 10\%$       |
|                                |               |          | 187.5 | _     | 333 | ns    | PLL multiplied by 3<br>When using an oscillator circuit<br>$V_{cc} = 5.0 V \pm 10\%$       |
| Clock cycle time               | tcy∟          | X0, X1   | 250   | _     | 333 | ns    | PLL multiplied by 4<br>When using an oscillator circuit<br>$V_{cc} = 5.0 V \pm 10\%$       |
| Clock cycle time               |               |          | 200   | _     | 333 | ns    | When using an oscillator circuit<br>Vcc < 4.5 V(MB90F548GL(S)/543G(S)/<br>547G(S)/548G(S)) |
|                                |               |          | 62.5  | _     | 333 | ns    | No multiplier<br>When using an external clock  |
|                                |               |          | 62.5  | _     | 125 | ns    | PLL multiplied by 1<br>When using an external clock  |
|                                |               |          | 125   | _     | 250 | ns    | PLL multiplied by 2<br>When using an external clock  |
|                                |               |          | 187.5 | -     | 333 | ns    | PLL multiplied by 3<br>When using an external clock  |
|                                |               |          | 250   | _     | 333 | ns    | PLL multiplied by 4<br>When using an external clock  |
|                                | <b>t</b> LCYL | X0A, X1A | -     | 30.5  | -   | μs    |  |
| Input clock pulse width        | Pwh, Pwl      | X0       | 10    | —     | —   | ns    | Duty ratio is about $30\%$ to $70\%$ .   |
|                                | Pwlh, Pwll    | X0A      | —     | 15.2  | —   | μs    |  |
| Input clock rise and fall time | tcr, tcr      | X0       | _     | _     | 5   | ns    | When using an external clock   |
| Machine clock frequency        | fcp           | -        | 1.5   | —     | 16  | MHz   | When using main clock  |
|                                | flcp          | -        | —     | 8.192 | —   | kHz   | When using sub-clock   |
| Machine clock cycle time       | tcp           | -        | 62.5  | —     | 666 | ns    | When using main clock  |
| Machine Gook Cycle uille       | <b>t</b> LCP  | -        | -     | 122.1 | -   | μs    | When using sub-clock   |











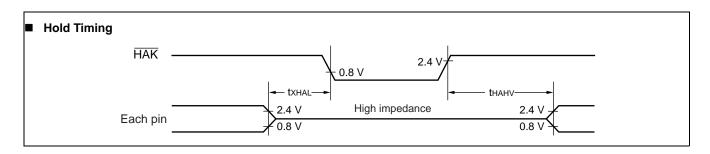


### 11.4.8 Hold Timing

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V \text{ to } 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ }^{\circ}\text{C} \text{ to } + 105 \text{ }^{\circ}\text{C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V\_{CC} = 5.0 V ± 10\%, V\_{SS} = AV\_{SS} = 0.0 V, T\_A = -40 \text{ }^{\circ}\text{C} \text{ to } + 105 \text{ }^{\circ}\text{C})

| Parameter   | Symbol Pin name |         | Condition | Va  | lue   | Units | Remarks |
|---|-----------------|---------|-----------|-----|-------|-------|---------|
| Faranielei  | Symbol          | Finname | Condition | Min | Max   | Units | Remarks |
| Pin floating $\rightarrow \overline{\text{HAK}}\downarrow$ time | <b>t</b> xhal   | HAK     |           | 30  | tcp   | ns    |         |
| $\overline{\text{HAK}}$ time $\rightarrow$ Pin valid time       | tнанv           | HAK     | _         | tcp | 2 tcp | ns    |         |

Note : There is more than 1 cycle from the time HRQ is read to the time the  $\overline{HAK}$  is changed.



### 11.4.9 UART0/1, Serial I/O Timing

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V \text{ to } 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ °C to } + 105 \text{ °C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V\_{CC} = 5.0 V ± 10%, V\_{SS} = AV\_{SS} = 0.0 V, T\_A = -40 \text{ °C to } + 105 \text{ °C})

| Parameter                                | Symbol | Pin name                      | Condition   | Value             |     | Units | Remarks  |
|--|--------|-------------------------------|---|-------------------|-----|-------|----------|
| Farameter                                | Symbol | Fin hame                      | Condition   | Min Max           |     | Units | Rellians |
| Serial clock cycle time                  | tscyc  | SCK0 to SCK2                  |   | 8 tcp             | -   | ns    |          |
| $SCK \downarrow \to SOT$ delay time      | tslov  | SCK0 to SCK2,<br>SOT0 to SOT2 | Internal clock operation                              | - 80              | 80  | ns    |          |
| Valid SIN $\rightarrow$ SCK <sup>↑</sup> | tıvsн  | SCK0 to SCK2,<br>SIN0 to SIN2 | output pins are C∟ = 80<br>pF + 1 TTL.                | 100               | _   | ns    |          |
| $SCK^{\uparrow} \to Valid SIN hold time$ | tsнix  | SCK0 to SCK2,<br>SIN0 to SIN2 |   | 60                | _   | ns    |          |
| Serial clock "H" pulse width             | tshsL  | SCK0 to SCK2                  |   | 4 t <sub>CP</sub> | -   | ns    |          |
| Serial clock "L" pulse width             | tslsh  | SCK0 to SCK2                  |   | 4 tcp             | -   | ns    |          |
| $SCK \downarrow \to SOT$ delay time      | tslov  | SCK0 to SCK2,<br>SOT0 to SOT2 | External clock operation output pins are $C_{L} = 80$ | _                 | 150 | ns    |          |
| Valid SIN $\rightarrow$ SCK <sup>↑</sup> | tıvsн  | SCK0 to SCK2,<br>SIN0 to SIN2 | pF + 1 TTL.   | 60                | _   | ns    |          |
| $SCK^{\uparrow} \to Valid SIN hold time$ | tsнıx  | SCK0 to SCK2,<br>SIN0 to SIN2 |   | 60                | _   | ns    |          |

Notes :

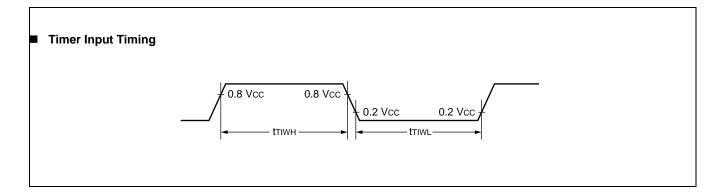
- AC characteristic in CLK synchronized mode.
- $C_{L}$  is load capacity value of pins when testing.
- For tcp (Machine clock cycle time), refer to "(1) Clock Timing".



### 11.4.10 Timer Input Timing

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V \text{ to } 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ }^{\circ}\text{C} \text{ to } +105 \text{ }^{\circ}\text{C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V\_{CC} = 5.0 V ± 10\%, V\_{SS} = AV\_{SS} = 0.0 V, T\_A = -40 \text{ }^{\circ}\text{C} \text{ to } +105 \text{ }^{\circ}\text{C})

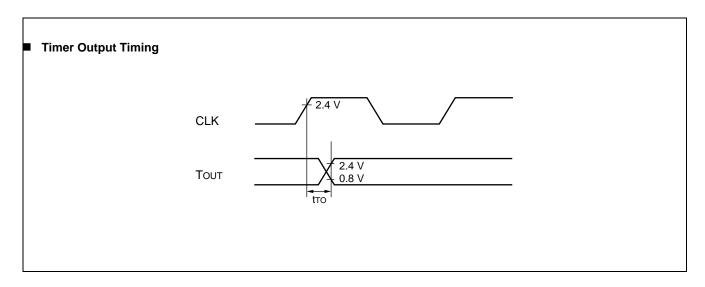
| Parameter         | Symbol Pin name |                 | Condition | Va    | ue  | Units | Remarks   |
|-------------------|-----------------|-----------------|-----------|-------|-----|-------|-----------|
| Falanetei         | Symbol          | OI Pin name Con |           | Min   | Max |       | Relliarks |
| Input pulso width | tтіwн           | TIN0, TIN1      | _         | 4 +== | _   | 20    |           |
| Input pulse width | t⊤ıw∟           | IN0 to IN7      |           | 4 tcp |     | ns    |           |



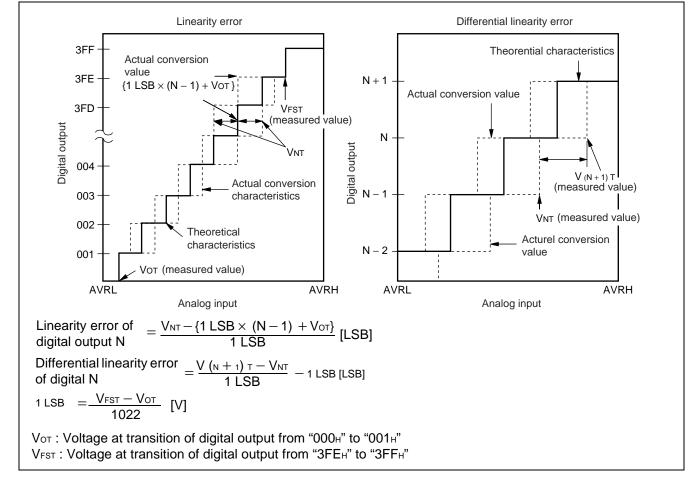
### 11.4.11 Timer Output Timing

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V \text{ to } 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ °C to } + 105 \text{ °C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V\_{CC} = 5.0 V ± 10%, V\_{SS} = AV\_{SS} = 0.0 V, T\_A = -40 \text{ °C to } + 105 \text{ °C})

| Parameter                                | Symbol | Pin name                     | Condition | Value |     | Units | Remarks |
|--|--------|------------------------------|-----------|-------|-----|-------|---------|
| i arameter                               | Symbol | r in name                    | Condition | Min   | Max | Onits | Remarks |
| $CLK^{\uparrow} \to T_{OUT}$ change time | tто    | TOT0 , TOT1,<br>PPG0 to PPG3 | _         | 30    | _   | ns    |         |







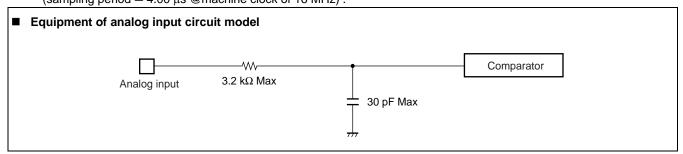
### 11.5.3 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions, :

Output impedance values of the external circuit of 15 kΩ or lower are recommended.

When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.
Note: When the output impedance of the external circuit is too high the sampling period for analog voltages may not be sufficient.

Note : When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period =  $4.00 \ \mu s$  @machine clock of 16 MHz).



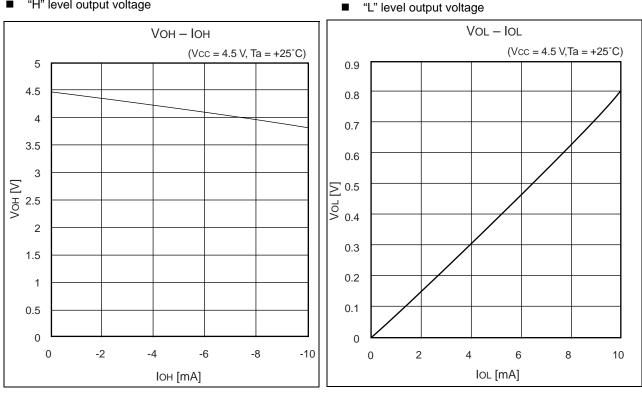
#### 11.5.4 Error

The smaller the |AVRH - AVRL|, the greater the error would become relatively.

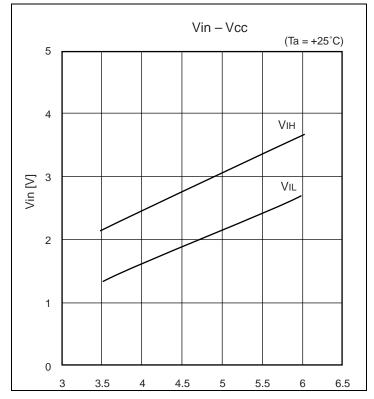


## **12. Example Characteristics**

"H" level output voltage



■ "H" level input voltage/ "L" level input voltage (Hysterisis inpiut)



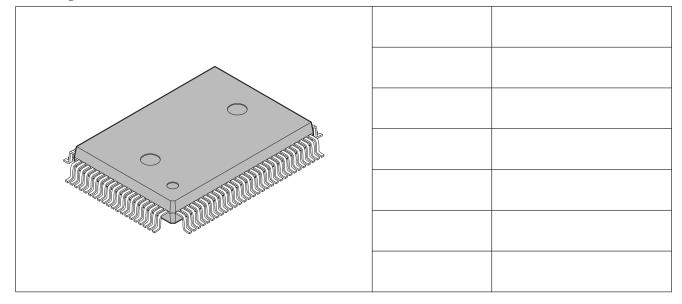


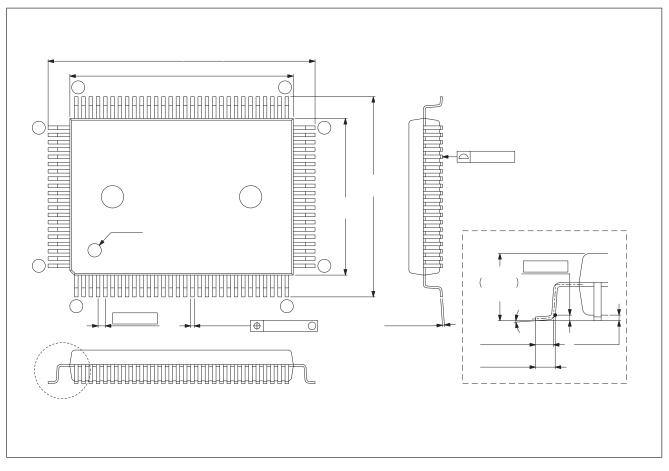
## **13. Ordering Information**

| Part number    | Package              | Remarks |
|----------------|----------------------|---------|
| MB90F543GPF    |                      |         |
| MB90F543GSPF   |                      |         |
| MB90F546GPF    |                      |         |
| MB90F546GSPF   | 100-pin Plastic QFP  |         |
| MB90F548GPF    |                      |         |
| MB90F548GSPF   |                      |         |
| MB90F548GLPF   |                      |         |
| MB90F548GLSPF  |                      |         |
| MB90F549GPF    |                      |         |
| MB90F549GSPF   | (FPT-100P-M06)       |         |
| MB90543GPF     |                      |         |
| MB90543GSPF    |                      |         |
| MB90547GPF     |                      |         |
| MB90547GSPF    |                      |         |
| MB90548GPF     |                      |         |
| MB90548GSPF    |                      |         |
| MB90549GPF     |                      |         |
| MB90549GSPF    |                      |         |
| MB90F543GPMC   |                      |         |
| MB90F543GSPMC  |                      |         |
| MB90F546GPMC   |                      |         |
| MB90F546GSPMC  |                      |         |
| MB90F548GPMC   |                      |         |
| MB90F548GSPMC  |                      |         |
| MB90F548GLPMC  |                      |         |
| MB90F548GLSPMC |                      |         |
| MB90F549GPMC   | 100-pin Plastic LQFP |         |
| MB90F549GSPMC  | (FPT-100P-M20)       |         |
| MB90543GPMC    |                      |         |
| MB90543GSPMC   |                      |         |
| MB90547GPMC    |                      |         |
| MB90547GSPMC   |                      |         |
| MB90548GPMC    |                      |         |
| MB90548GSPMC   |                      |         |
| MB90549GPMC    |                      |         |
| MB90549GSPMC   |                      |         |



# 14. Package Dimensions









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