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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspf-gse1

Features	MB90F543G (S) /F548G (S) MB90F549G (S) /F546G (S) MB90F548GL(S)	MB90543G (S) MB90547G (S) MB90548G (S) MB90549G (S)	MB90V540G
16-bit Reload Timer (2 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = System clock frequency) Supports External Event Count function Signals an interrupt when overflow		
16-bit Free-run Timer	Supports Timer Clear when a match with Output Compare (Channel 0) Operation clock freq. : fsys/2^2, fsys/2^4, fsys/2^6, fsys/2^8 (fsys = System clock freq.)		
16-bit Output Compare (4 channels)	Signals an interrupt when a match with 16-bit Free-run Timer Four 16-bit compare registers A pair of compare registers can be used to generate an output signal		
16-bit Input Capture (8 channels)	Rising edge, falling edge or rising & falling edge sensitive Four 16-bit Capture registers Signals an interrupt upon external event		
8/16-bit Programmable Pulse Generator (4 channels)	Supports 8-bit and 16-bit operation modes Eight 8-bit reload counters Eight 8-bit reload registers for L pulse width Eight 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter 4 output pins Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 µs@fosc = 4 MHz (fsys = System clock frequency, fosc = Oscillation clock frequency)		
CAN Interface MB90540G series : 2 channels MB90545G series : 1 channel	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 massage buffers for data and ID's supports multipe massages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps		
32 kHz Sub-clock	Sub-clock for low power operation		
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive		
External bus interface	External access using the selectable 8-bit or 16-bit bus is enabled (external bus mode.)		
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs and schmitt trigger inputs Bit-wise programmable as input/output or peripheral signal Sub-clock for 32 kHz Sub clock low power operation		
Flash Memory	Supports automatic programming, Embeded Algorithm Write/Erase/Erase-Suspend/Erase-Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block Block protection by externally programmed voltage		

*1 : If the one clock system is used, equip X0A and X1A with clocks from the tool side.

Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
11	13	P33	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode, external bus 8-bit mode or when WRH pin output is disabled.
		$\overline{\text{WRH}}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{\text{WRH}}$ output pin is enabled.
12	14	P34	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.
13	15	P35	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.
14	16	P36	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.
		RDY		Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.
15	17	P37	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the CLK output is disabled.
		CLK		CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled.
16	18	P40	G	General I/O port. This function is enabled when UART0 disables the serial data output.
		SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.
17	19	P41	G	General I/O port. This function is enabled when UART0 disables serial clock output.
		SCK0		Serial clock I/O pin for UART0. This function is enabled when UART0 enables the serial clock output.
18	20	P42	G	General I/O port. This function is always enabled.
		SIN0		Serial data input pin for UART0. Set the corresponding Port Direction Register to input if this function is used.
19	21	P43	G	General I/O port. This function is always enabled.
		SIN1		Serial data input pin for UART1. Set the corresponding Port Direction Register to input if this function is used.

(Continued)

(6) Pull-up/down resistors

The MB90540G/545G Series does not support internal pull-up/down resistors (except Port0 − Port3 : pull-up resistors) . Use external components where needed.

(7) Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via the shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuits do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation.

(8) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}) .

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable) .

(9) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

(10) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

(11) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μs or more (0.2 V to 2.7 V) .

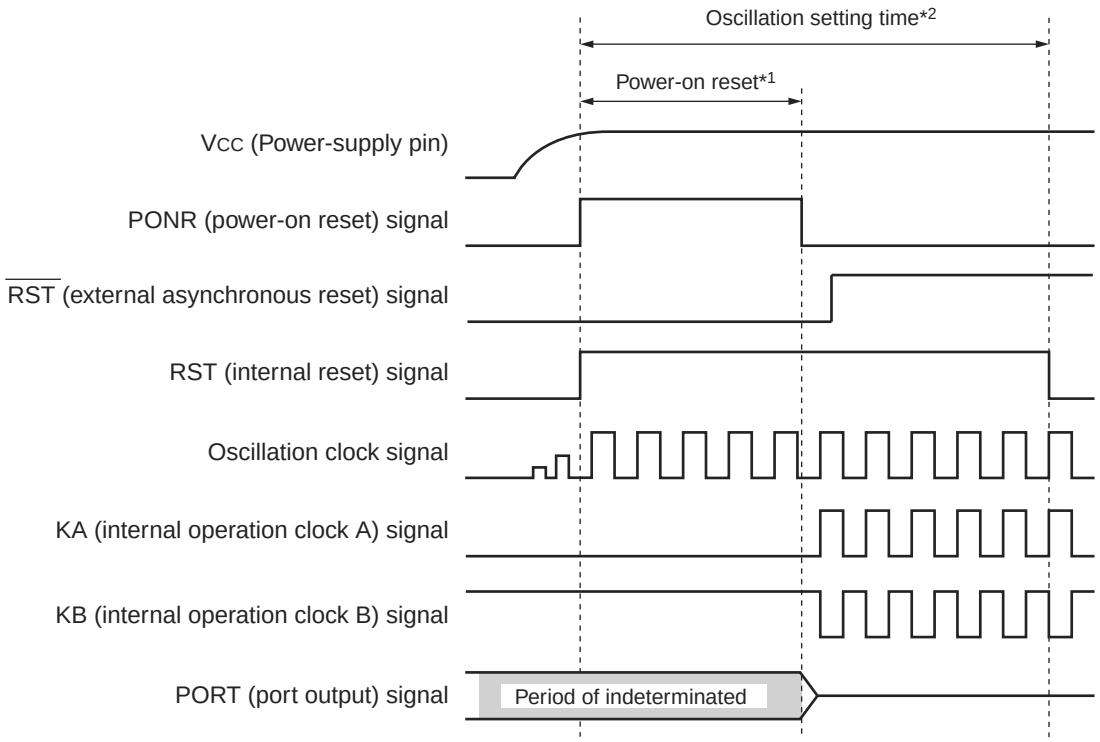
(12) Indeterminate outputs from ports 0 and 1 (MB90V540G only)

During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

- If $\overline{RST}$ pin is “H”, the outputs become indeterminate.
- If $\overline{RST}$ pin is “L”, the outputs become high-impedance.

Pay attention to the port output timing shown as follow.

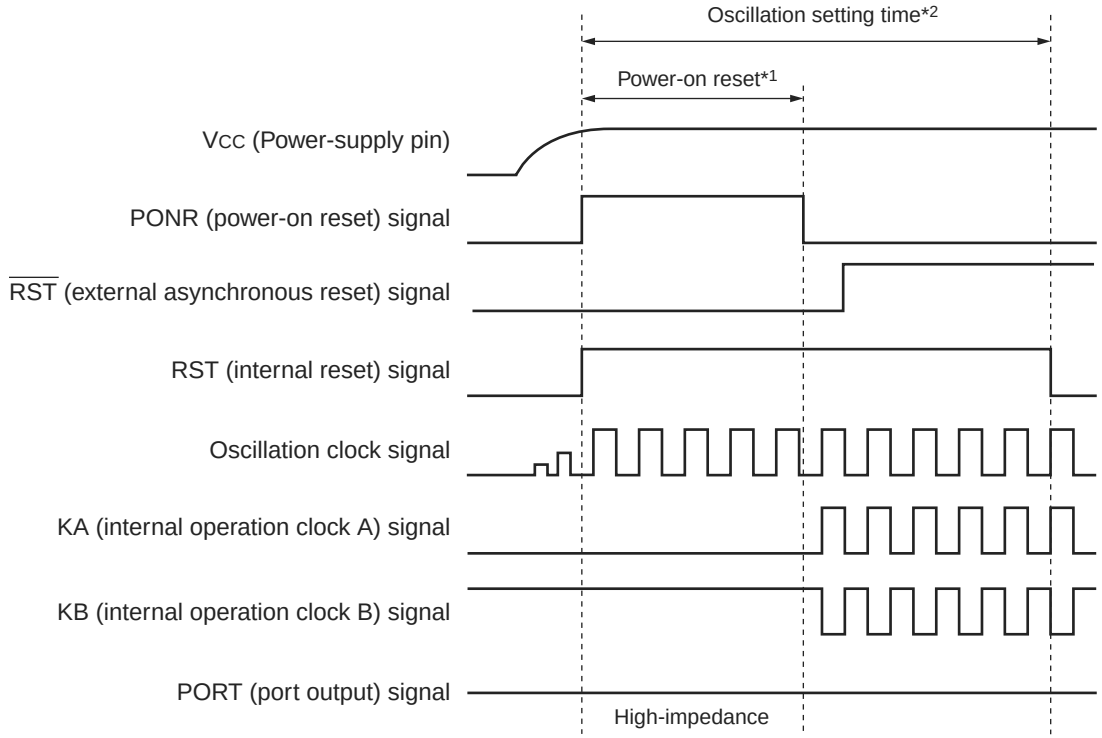
- $\overline{RST}$ pin is “H”



*1 : Power-on reset time : “Period of clock frequency” × 2^{17} (Clock frequency of 16 MHz : 8.19 ms)

*2 : Oscillation setting time : “Period of clock frequency” × 2^{18} (Clock frequency of 16 MHz : 16.38 ms)

■ $\overline{\text{RST}}$ pin is “L”



*1 : Power-on reset time : “Period of clock frequency” × 2^{17} (Clock frequency of 16 MHz : 8.19 ms)

*2 : Oscillation setting time : “Period of clock frequency” × 2^{18} (Clock frequency of 16 MHz : 16.38 ms)

(13) Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(14) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions

In the Signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”) , the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00_H”.

If the values of the corresponding bank registers (DTB, ADB, USB, SSB) are set to other than “00_H”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

(15) Using REALOS

The use of EI²OS is not possible with the REALOS real time operating system.

(16) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

Address	Register	Abbreviation	Access	Resource name	Initial value
47_H to $4B_H$	Prohibited				
$4C_H$	Input capture control status register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0_B
$4D_H$	Input capture control status register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0_B
$4E_H$	Input capture control status register 4/5	ICS45	R/W	Input Capture 4/5	0 0 0 0 0 0 0 0_B
$4F_H$	Input capture control status register 6/7	ICS67	R/W	Input Capture 6/7	0 0 0 0 0 0 0 0_B
50_H	Timer control status register 0	TMCSR0	R/W	16-bit Reload Timer 0	0 0 0 0 0 0 0 0_B
51_H	Timer control status register 0	TMCSR0	R/W		_ _ _ _ 0 0 0 0_B
52_H	Timer register 0/reload register 0	TMR0/TMRLR0	R/W		XXXXXXXX_B
53_H	Timer register 0/reload register 0	TMR0/TMRLR0	R/W		XXXXXXXX_B
54_H	Timer control status register 1	TMCSR1	R/W	16-bit Reload Timer 1	0 0 0 0 0 0 0 0_B
55_H	Timer control status register 1	TMCSR1	R/W		_ _ _ _ 0 0 0 0_B
56_H	Timer register 1/reload register 1	TMR1/TMRLR1	R/W		XXXXXXXX_B
57_H	Timer register 1/reload register 1	TMR1/TMRLR1	R/W		XXXXXXXX_B
58_H	Output compare control status register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 _ _ 0 0_B
59_H	Output compare control status register 1	OCS1	R/W		_ _ _ 0 0 0 0 0_B
$5A_H$	Output compare control status register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 _ _ 0 0_B
$5B_H$	Output compare control status register 3	OCS3	R/W		_ _ _ 0 0 0 0 0_B
$5C_H$ to $6B_H$	Prohibited				
$6C_H$	Timer Data register	TCDT	R/W	I/O Timer	0 0 0 0 0 0 0 0_B
$6D_H$	Timer Data register	TCDT	R/W		0 0 0 0 0 0 0 0_B
$6E_H$	Timer Control register	TCCS	R/W		0 0 0 0 0 0 0 0_B
$6F_H$	ROM mirror function selection register	ROMM	R/W	ROM Mirror	_ _ _ _ _ _ _ 1_B
70_H to $7F_H$	Reserved for CAN 0 Interface.				
80_H to $8F_H$	Reserved for CAN 1 Interface.				
90_H to $9D_H$	Prohibited				
$9E_H$	Program address detection control status register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0_B
$9F_H$	Delayed interrupt/release register	DIRR	R/W	Delayed Interrupt	_ _ _ _ _ _ _ 0_B
$A0_H$	Low-power mode control register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0_B
$A1_H$	Clock selection register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0_B

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Address	Register	Abbreviation	Access	Resource name	Initial value
3928H	Output Compare Register 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
3929H	Output Compare Register 0	OCCP0	R/W		XXXXXXXXB
392AH	Output Compare Register 1	OCCP1	R/W		XXXXXXXXB
392BH	Output Compare Register 1	OCCP1	R/W		XXXXXXXXB
392CH	Output Compare Register 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXXB
392DH	Output Compare Register 2	OCCP2	R/W		XXXXXXXXB
392EH	Output Compare Register 3	OCCP3	R/W		XXXXXXXXB
392FH	Output Compare Register 3	OCCP3	R/W		XXXXXXXXB
3930H to 39FFH	Reserved				
3A00H to 3AFFH	Reserved for CAN 0 Interface.				
3B00H to 3BFFH	Reserved for CAN 0 Interface.				
3C00H to 3CFFH	Reserved for CAN 1 Interface.				
3D00H to 3DFFH	Reserved for CAN 1 Interface.				
3E00H to 3FFFH	Reserved				

- Read/write notation
  - R/W : Reading and writing permitted
  - R : Read-only
  - W : Write-only

- Initial value notation
  - 0 : Initial value is “0”.
  - 1 : Initial value is “1”.
  - X : Initial value is undefined.
  - _ : Initial value is unused.

Note: Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

List of Message Buffers (DLC Registers and Data Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A60H	003C60H	DLC register 0	DLCR0	R/W	----XXXXB
003A61H	003C61H				
003A62H	003C62H	DLC register 1	DLCR1	R/W	----XXXXB
003A63H	003C63H				
003A64H	003C64H	DLC register 2	DLCR2	R/W	----XXXXB
003A65H	003C65H				
003A66H	003C66H	DLC register 3	DLCR3	R/W	----XXXXB
003A67H	003C67H				
003A68H	003C68H	DLC register 4	DLCR4	R/W	----XXXXB
003A69H	003C69H				
003A6AH	003C6AH	DLC register 5	DLCR5	R/W	----XXXXB
003A6BH	003C6BH				
003A6CH	003C6CH	DLC register 6	DLCR6	R/W	----XXXXB
003A6DH	003C6DH				
003A6EH	003C6EH	DLC register 7	DLCR7	R/W	----XXXXB
003A6FH	003C6FH				
003A70H	003C70H	DLC register 8	DLCR8	R/W	----XXXX
003A71H	003C71H				
003A72H	003C72H	DLC register 9	DLCR9	R/W	----XXXXB
003A73H	003C73H				
003A74H	003C74H	DLC register 10	DLCR10	R/W	----XXXXB
003A75H	003C75H				
003A76H	003C76H	DLC register 11	DLCR11	R/W	----XXXXB
003A77H	003C77H				
003A78H	003C78H	DLC register 12	DLCR12	R/W	----XXXXB
003A79H	003C79H				
003A7AH	003C7AH	DLC register 13	DLCR13	R/W	----XXXXB
003A7BH	003C7BH				
003A7CH	003C7CH	DLC register 14	DLCR14	R/W	----XXXXB
003A7DH	003C7DH				
003A7EH	003C7EH	DLC register 15	DLCR15	R/W	----XXXXB
003A7FH	003C7FH				
003A80H to 003A87H	003C80H to 003C87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB

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(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Power supply current*	I_{CC}	V_{CC}	Internal frequency : 16 MHz, At normal operating	—	40	55	mA	
			Internal frequency : 16 MHz, At Flash programming/erasing	—	50	70	mA	Flash device
	I_{CCS}		Internal frequency : 16 MHz, At sleep mode	—	12	20	mA	
	I_{CTS}		V_{CC} = 5.0 V ± 10%, Internal frequency : 2 MHz, At pseudo timer mode	—	300	600	µA	
				—	600	1100	µA	MB90F548GL (S) only
				—	200	400	µA	MB90543G(S)/547G(S)/548(S) only
	I_{CCL}		Internal frequency : 8 kHz, At sub operation, T_A = 25 °C	—	400	750	µA	MB90F548GL only
				—	50	100	µA	MASK ROM
				—	150	300	µA	Flash device
	I_{CCLS}		Internal frequency : 8 kHz, At sub sleep, T_A = 25 °C	—	15	40	µA	
	I_{CCT}		Internal frequency : 8 kHz, At timer mode, T_A = 25 °C	—	7	25	µA	
	I_{CCH1}		At stop, T_A = 25 °C	—	5	20	µA	
	I_{CCH2}		At hardware standby mode, T_A = 25 °C	—	50	100	µA	
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVRH, AVRL, C, V_{CC}, V_{SS}	—	—	5	15	pF	

* : The power supply current testing conditions are when using the external clock.

11.4 AC Characteristics

11.4.1 Clock Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Oscillation frequency	f_C	X0, X1	3	—	16	MHz	No multiplier When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			8	—	16	MHz	PLL multiplied by 1 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			4	—	8	MHz	PLL multiplied by 2 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			3	—	5.33	MHz	PLL multiplied by 3 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			3	—	4	MHz	PLL multiplied by 4 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			3	—	5	MHz	When using an oscillator circuit V_{CC} < 4.5 V(MB90F548GL(S)/543G(S)/547G(S)/548G(S))
			3	—	16	MHz	No multiplier When using an external clock
			8	—	16	MHz	PLL multiplied by 1 When using an external clock
			4	—	8	MHz	PLL multiplied by 2 When using an external clock
			3	—	5.33	MHz	PLL multiplied by 3 When using an external clock
			3	—	4	MHz	PLL multiplied by 4 When using an external clock
	f_{CL}	X0A, X1A	—	32.768	—	kHz	

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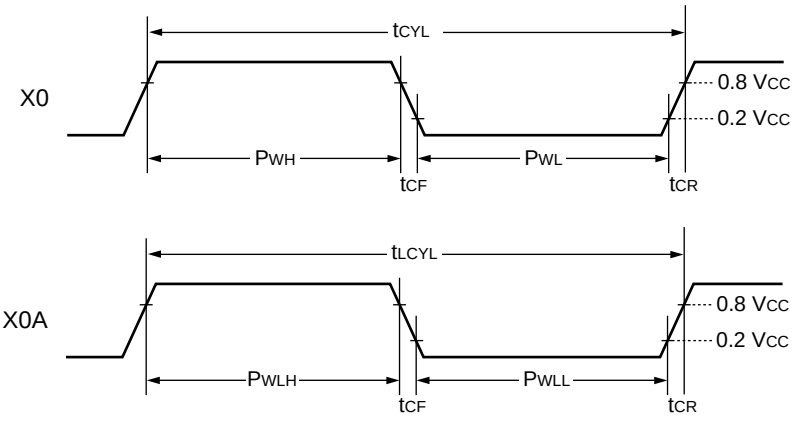
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

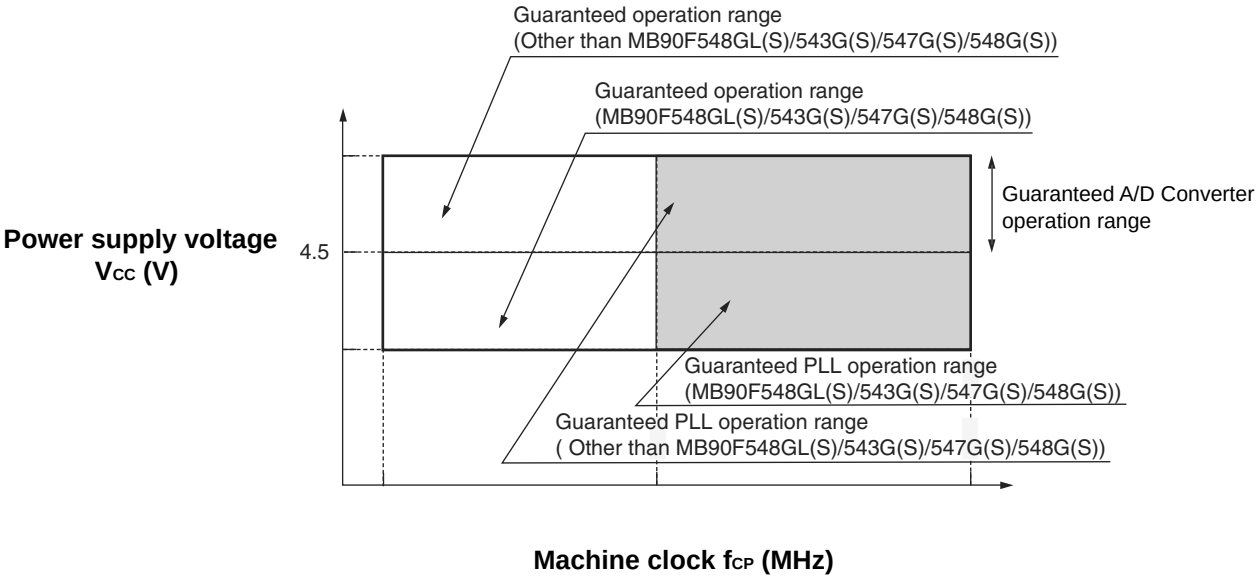
(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	No multiplier When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			62.5	—	125	ns	PLL multiplied by 1 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			125	—	250	ns	PLL multiplied by 2 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			187.5	—	333	ns	PLL multiplied by 3 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			250	—	333	ns	PLL multiplied by 4 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			200	—	333	ns	When using an oscillator circuit V_{CC} < 4.5 V(MB90F548GL(S)/543G(S)/547G(S)/548G(S))
			62.5	—	333	ns	No multiplier When using an external clock
			62.5	—	125	ns	PLL multiplied by 1 When using an external clock
			125	—	250	ns	PLL multiplied by 2 When using an external clock
			187.5	—	333	ns	PLL multiplied by 3 When using an external clock
			250	—	333	ns	PLL multiplied by 4 When using an external clock
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WLH}, P_{WLL}	X0A	—	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using an external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	When using main clock
	f_{LCP}	—	—	8.192	—	kHz	When using sub-clock
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	When using main clock
	t_{LCP}	—	—	122.1	—	µs	When using sub-clock

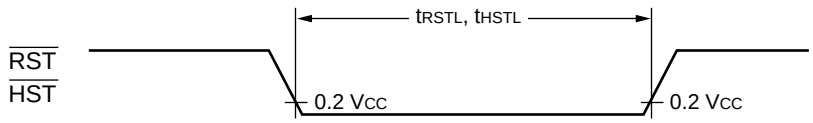
■ **Clock Timing**



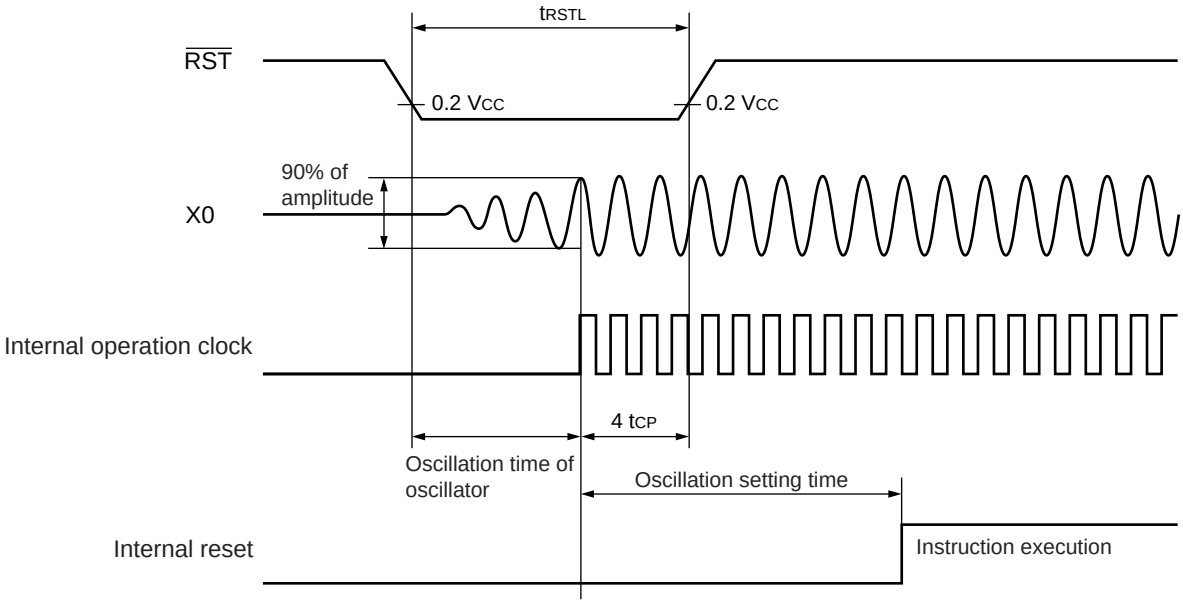
■ **Guaranteed PLL operation range**



■ In under normal operation, pseudo timer mode, sub-clock mode, sub-sleep mode, timer mode



■ In stop mode



11.4.8 Hold Timing

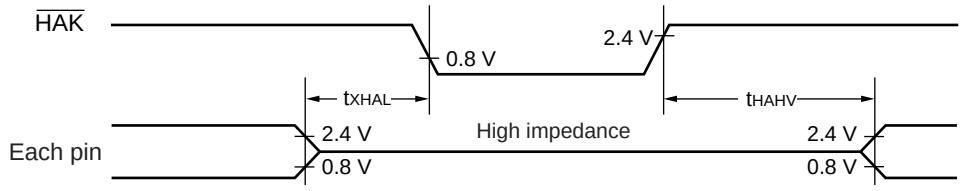
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Pin floating → $\overline{HAK}$↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}	ns	
$\overline{HAK}$↑ time → Pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}	ns	

Note : There is more than 1 cycle from the time HRQ is read to the time the $\overline{HAK}$ is changed.

■ **Hold Timing**



11.4.9 UART0/1, Serial I/O Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	8 t_{CP}	—	ns	
SCK↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		− 80	80	ns	
Valid SIN → SCK↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK2	External clock operation output pins are C_L = 80 pF + 1 TTL.	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK2		4 t_{CP}	—	ns	
SCK↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN → SCK↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

Notes :

- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- For t_{CP} (Machine clock cycle time) , refer to “ (1) Clock Timing”.

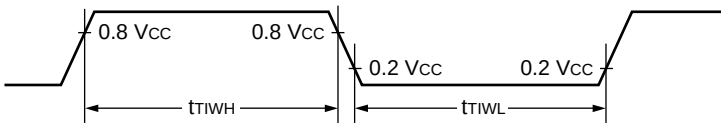
11.4.10 Timer Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	4 t_{CP}	—	ns	
	t_{TIWL}	IN0 to IN7					

■ **Timer Input Timing**



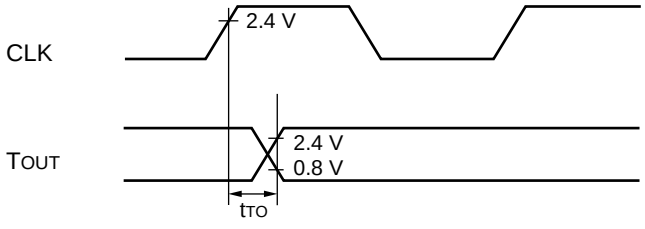
11.4.11 Timer Output Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
CLK↑ → T_{OUT} change time	t_{TO}	TOT0 , TOT1, PPG0 to PPG3	—	30	—	ns	

■ **Timer Output Timing**



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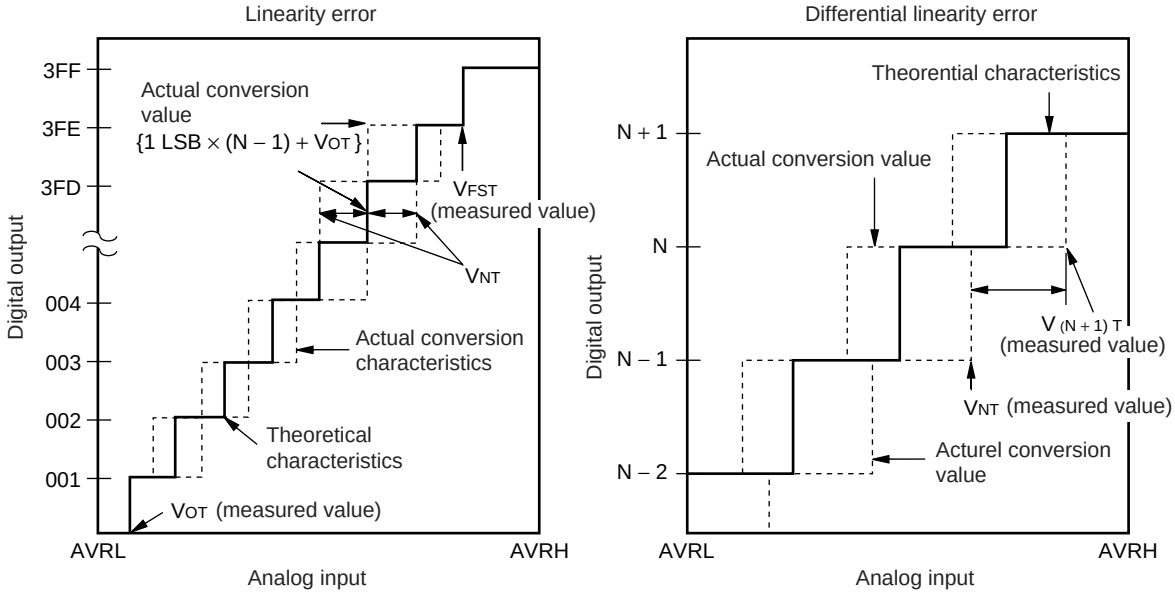


$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage at transition of digital output from "000_H" to "001_H"
V_{FST} : Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

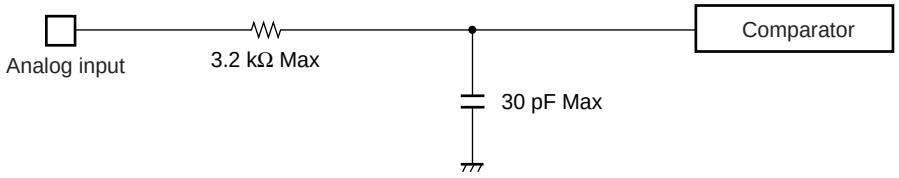
11.5.3 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions, :

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

Note : When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz) .

■ **Equipment of analog input circuit model**

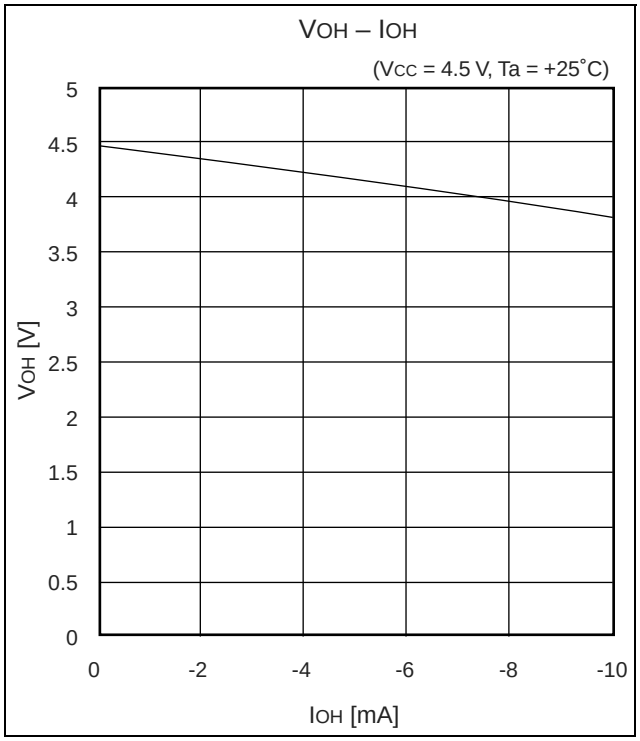


11.5.4 Error

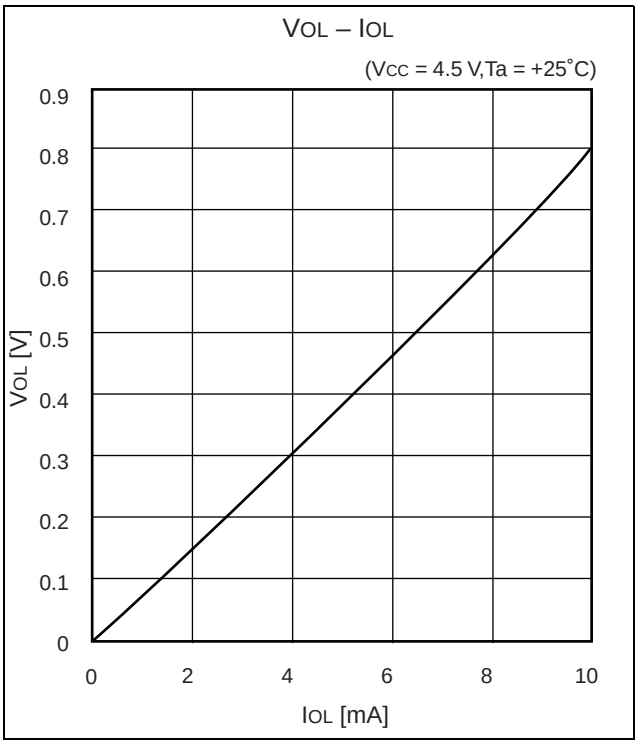
The smaller the | AVRH − AVRL |, the greater the error would become relatively.

12. Example Characteristics

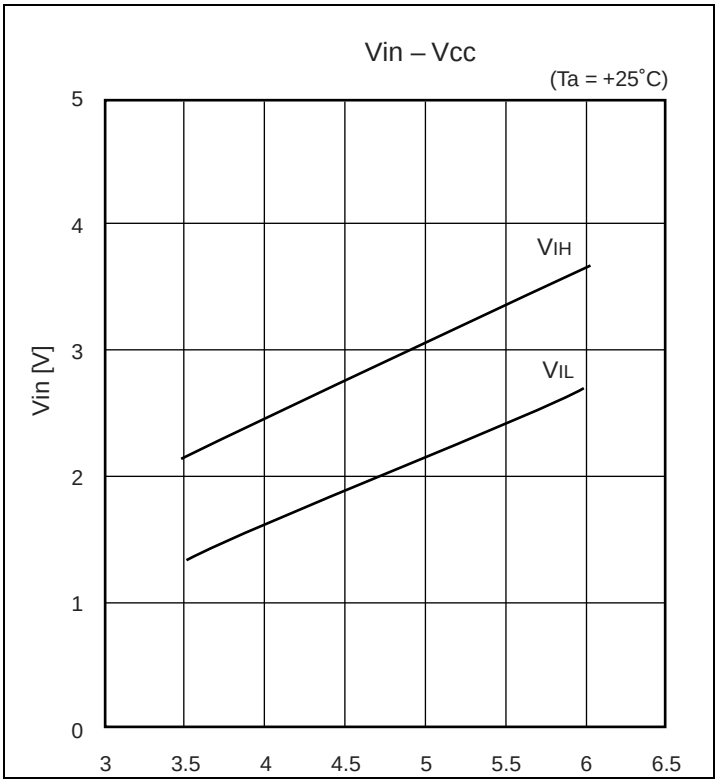
■ “H” level output voltage



■ “L” level output voltage



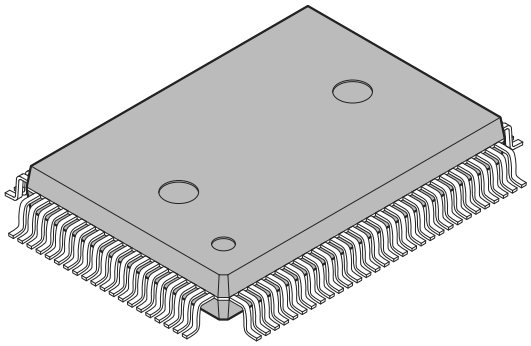
■ “H” level input voltage/ “L” level input voltage (Hysterisis inpiut)

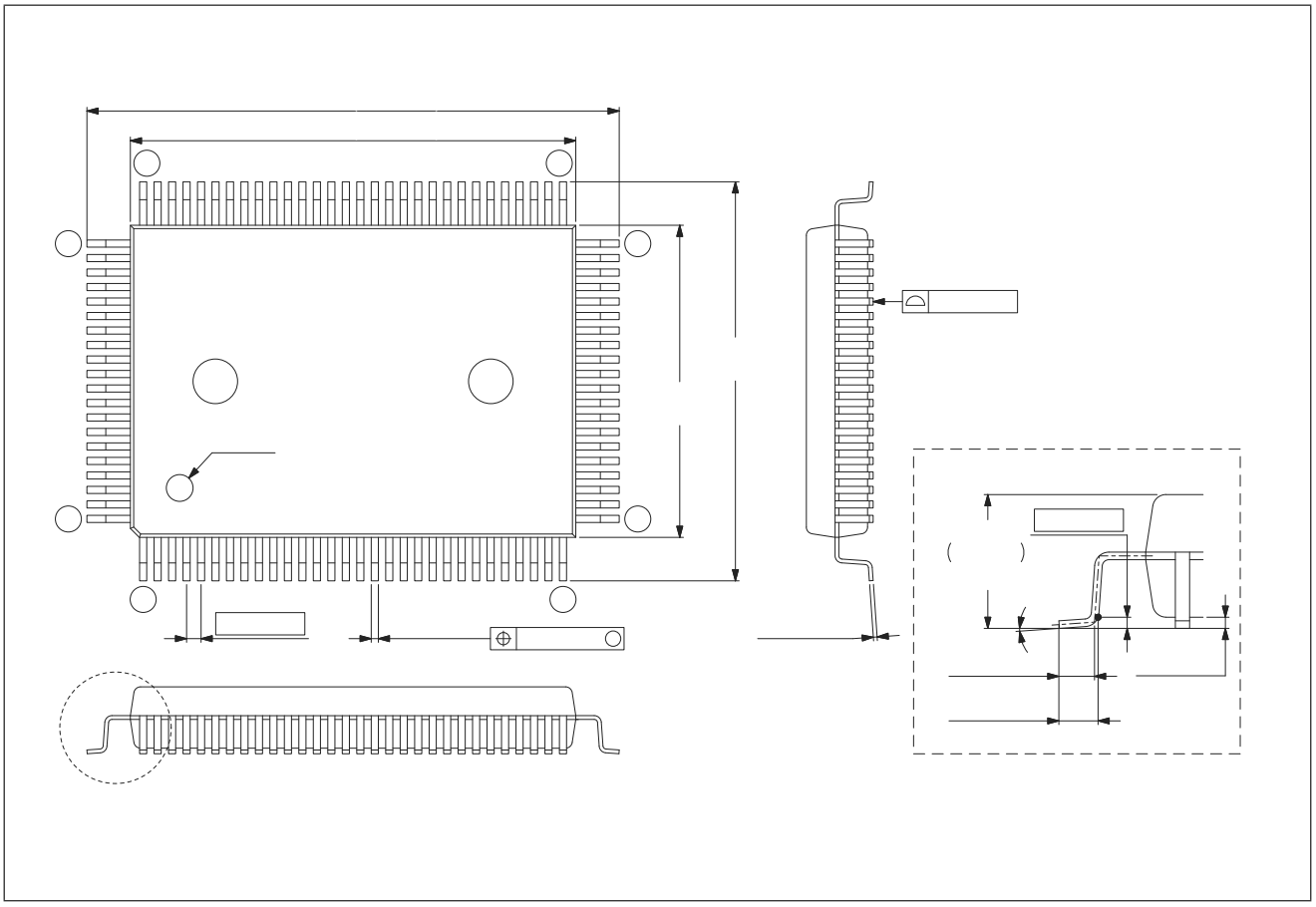


13. Ordering Information

Part number	Package	Remarks
MB90F543GPF MB90F543GSPF MB90F546GPF MB90F546GSPF MB90F548GPF MB90F548GSPF MB90F548GLPF MB90F548GLSPF MB90F549GPF MB90F549GSPF MB90543GPF MB90543GSPF MB90547GPF MB90547GSPF MB90548GPF MB90548GSPF MB90549GPF MB90549GSPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90F543GPMC MB90F543GSPMC MB90F546GPMC MB90F546GSPMC MB90F548GPMC MB90F548GSPMC MB90F548GLPMC MB90F548GLSPMC MB90F549GPMC MB90F549GSPMC MB90543GPMC MB90543GSPMC MB90547GPMC MB90547GSPMC MB90548GPMC MB90548GSPMC MB90549GPMC MB90549GSPMC	100-pin Plastic LQFP (FPT-100P-M20)	

14. Package Dimensions



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