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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspmc-g

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Starting by an external trigger input. Conversion time : 26.3 μ s

FULL-CAN interfaces
 MB90540G series : 2 channels
 MB90545G series : 1 channel
 Conforming to Version 2.0 Part A and Part B

Flexible message buffering (mailbox and FIFO buffering can be mixed)

- External bus interface : Maximum address space 16 Mbytes
- Package: QFP-100, LQFP-100



3. Pin Description

Pin	No. Bin name Circuit type								
LQFP*2	QFP*1	Pin name	Circuit type	Function					
80 81	82 83	X0 X1	A (Oscillation)	High speed crystal oscillator input pins					
78	80	X0A	A	Low speed crystal oscillator input pins. For the one clock system parts, perfom external pull-down processing.					
77	79	X1A	(Oscillation)	Low speed crystal oscillator input pins. For the one clock system parts, leave it open.					
75	77	RST	В	External reset request input pin					
50	52	HST	С	Hardware standby input pin					
82 to 00	95 to 02	P00 to P07		General I/O port with programmable pullup. This function is enabled in the single-chip mode.					
83 10 90	00 10 92	AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.					
01 to 09	02 to 100	P10 to P17		General I/O port with programmable pullup. This function is enabled in the single-chip mode.					
91 to 98 93 to 100		AD08 to AD15]	I/O pins for 8 higher bits of the external address/data bus. This function is enabled when the external bus is enabled.					
00 to 6	1 to 0	P20 to P27		General I/O port with programmable pullup. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to "1".					
9910.0	1 10 8	A16 to A23		8-bit I/O pins for A16 to A23 at the external address/data bus. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to "0".					
7	0	P30		General I/O port with programmable pullup. This function is enabled in the single-chip mode.					
7	9	ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.					
	10	P31		General I/O port with programmable pullup. This function is enabled in the single-chip mode.					
0	10	RD		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.					
		P32		General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the WR/WRL pin output is disabled.					
10	12	WRL WR		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{WR}/\overline{WRL}$ pin output are enabled. \overline{WRL} is write-strobe output pin for the lower 8 bits of the data bus in 16-bit access. \overline{WR} is write-strobe output pin for the 8 bits of the data bus in 8-bit access.					



Pin	No.	Pin name	Circuit type	Function				
LQFP*2	QFP ^{*1}	Finname	Circuit type	Function				
		P33		General I/O port with programmable pullup. This f <u>unction is enabled in the single-chip mode, external bus 8-bit mode or when WRH pin output is disabled.</u>				
11 13		WRH		Write strobe output pin for the 8 higher bits of the data bus. This function enabled when the external bus is enabled, when the external bus 16-bit r is selected, and when the WRH output pin is enabled.				
12	14	P34		General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.				
12	14	HRQ		Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.				
13	15	P35		General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.				
15	15	HAK		Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.				
14	16	P36		General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.				
14 10		RDY		Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.				
15	17	P37		General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the CLK output is disabled.				
15	17	CLK		CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled.				
16	10	P40	C	General I/O port. This function is enabled when UART0 disables the serial data output.				
10	10	SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.				
17	10	P41	C	General I/O port. This function is enabled when UART0 disables serial clock output.				
17	19	SCK0	G	Serial clock I/O pin for UART0. This function is enabled when UART0 enables the serial clock output.				
		P42		General I/O port. This function is always enabled.				
18	20	SINO	G	Serial data input pin for UART0. Set the corresponding Port Direction Register to input if this function is used.				
		P43		General I/O port. This function is always enabled.				
19	21	SIN1	G	Serial data input pin for UART1. Set the corresponding Port Direction Register to input if this function is used.				



6. Block Diagram





7. Memory Map

The memory space of the MB90540G/545G Series is shown below.



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits address are the same, the table in ROM can be referenced without using the "far" specification in the pointer declaration.

For example, an attempt to access $00C000_{H}$ accesses the value at FFC000_{H} in ROM. The ROM area in bank FF exceeds 48 Kbytes, and its entire image cannot be shown in bank 00. The image between FF4000_{H} and FFFFFF_{H} is visible in bank 00, while the image between FF0000_{H} and FF3FFF_{H} is visible only in bank FF.

MB90540G/545G Series



(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value				
3928н	Output Compare Register 0	OCCP0	R/W		XXXXXXXAB				
3929н	Output Compare Register 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB				
392Ан	Output Compare Register 1	OCCP1	R/W		XXXXXXXXB				
392Вн	Output Compare Register 1	OCCP1	R/W		XXXXXXXXB				
392Сн	Output Compare Register 2	OCCP2	R/W		XXXXXXXXB				
392Dн	Output Compare Register 2	OCCP2	R/W	Output Compare 2/2	XXXXXXXAB				
392Ен	Output Compare Register 3	OCCP3	R/W		XXXXXXXAB				
392Fн	Output Compare Register 3	OCCP3	R/W		XXXXXXXXB				
3930н to 39FFн	Reserved								
ЗА00н to ЗАFFн	Reserved for CAN 0 Interface.								
3B00н to 3BFFн	Reserved for CAN 0 Interface.								
3C00н to 3CFFн	Reserved for CAN 1 Interface.								
3D00н to 3DFFн	Reserved for CAN 1 Interface.								
3E00н to 3FFFн	Reserved								

- Read/write notation
 - R/W : Reading and writing permitted
 - R : Read-only
 - W : Write-only

Initial value notation

- 0 : Initial value is "0".
- 1 : Initial value is "1".
- X : Initial value is undefined.
- _ : Initial value is unused.

Note: Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading "X".



9. CAN Controller

The MB90540G series contains two CAN controllers (CAN0 and CAN1), the MB90545G series contains only one (CAN0). The Evaluation Chip MB90V540G also has two CAN controllers.

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
 - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
 - □ 29-bit ID and 8-byte data
 - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
 - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 1 Mbps (when input clock is at 16 MHz)

List of Control Registers

Address		Pagistor	Abbroviation	Accoss	Initial Value	
CAN0	CAN1	Keyistei	Abbreviation	ALLESS		
000070н	000080н	Mossage buffer valid register		D AA/		
000071н	000081 н	Nessage builer valid register	BVALK		000000000000000000000000000000000000000	
000072н	000082н	Transmit request register	TREOR	D (M)	0000000 0000000-	
000073н	000083н		IREQR	R/W		
000074н	000084н	Transmit cancel register	TCANP	\A/		
000075н	000085н		TOANK	vv		
000076н	000086н	Transmit complete register	TCP			
000077н	000087н		TOR			
000078н	000088 _H	Possive complete register	PCP			
000079н	000089н	Receive complete register	NON		0000000 000000B	
00007Ан	00008Ан	Pomoto request receiving register	DDTDD	D AA/		
00007BH	00008Bн	Remote request receiving register			0000000 000000B	
00007Cн	00008Сн	Possive everyup register		D ///	0000000 0000000-	
00007DH	00008Dн	Receive overruit register	NOVER		000000000000000000000000000000000000000	
00007Eн	00008EH	Possive interrupt enable register	DIED			
00007Fн	00008Fн	Teceive interrupt enable register		17/ 17	0000000 0000000B	



Address		Pagistor	Abbroviation	A	Initial Value		
CAN0	CAN1	- Register	Appreviation	Access			
003A24 _H	003C24н				· · · · · · · · · · · · · · · · · · ·		
003А25н	003C25н	ID register 1		DAA	~~~~~		
003А26н	003C26н		IDRI	r/w			
003A27н	003C27н				~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~		
003A28H	003C28н				*****		
003A29н	003C29н	ID register 2		DAM			
003А2Ан	003C2Ан		IDINZ	r./ v v	××××× ×××××××××		
003А2Вн	003C2Bн				~~~~~		
003А2Сн	003С2Сн		IDR3	P \\	××××××××××××××××××××××××××××××××××××××		
003A2Dн	003C2Dн	ID register 2					
003А2Ен	003C2Eн			r/w	····		
003A2Fн	003C2Fн						
003А30н	003С30н		IDR4 F		· · · · · · · · · · · · · · · · · · ·		
003А31н	003C31н	ID register 4		DAM			
003А32н	003С32н			17/77			
003А33н	003С33н				~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~		
003A34H	003C34н				· · · · · · · · · · · · · · · · · · ·		
003А35н	003C35н	ID register 5		DAA	~~~~~~		
003А36н	003C36н		IDK5	r/w	····		
003А37н	003C37н				~~~~~ ~~~~~		
003А38н	003C38н						
003А39н	003C39н		IDB6	DAA	~~~~~~~~~		
003АЗАн	003С3Ан		IDRO	r./ v v	····		
003А3Вн	003С3Вн	7			~~~~~ ~~~~~		



(Continued)

Address		Pagistar	Abbroviation	A	Initial Value	
CAN0	CAN1	- Register	Appreviation	Access	Initial value	
003А3Сн	003C3CH				·····	
003А3Dн	003C3DH	ID register 7				
003А3Ен	003C3EH			R/W		
003A3Fн	003C3FH				~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	
003A40н	003C40н					
003A41н	003C41н	ID register 8			~~~~~	
003А42н	003C42н		IDRO	17/10		
003A43н	003С43н					
003A44н	003C44н				~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	
003A45н	003C45н	ID register 0		D AA/		
003A46н	003C46н		IDK9	R/W		
003A47н	003C47н					
003A48н	003C48н					
003A49н	003C49н	ID register 10		P/\/	~~~~~	
003А4Ан	003C4Ан			1.7.0.0		
003A4Bн	003C4Bн					
003A4Cн	003C4CH			R/W		
003A4Dн	003C4DH	ID register 11				
003A4Eн	003C4Eн		IDKT	IN/ V V	XXXXX XXXXXXXx	
003A4Fн	003C4Fн				~~~~~	
003A50н	003С50н					
003A51н	003C51н	ID register 12				
003А52н	003C52н			17/10		
003А53н	003С53н					
003А54н	003C54н					
003А55н	003C55н	ID register 13		P/\/	~~~~~	
003А56н	003С56н		IDICI3	1.7.0.0		
003А57 н	003C57н				~~~~~	
003A58н	003С58н					
003А59н	003С59н	ID register 14				
003А5Ан	003С5Ан		IDK14	IN/ V V		
003А5Вн	003C5Bн					
003А5Сн	003C5CH					
003А5Dн	003C5DH	ID register 15		P/M		
003А5Eн	003C5EH					
003A5Fн	003C5Fн					



(Continued)

Add	dress	Pagistor	Abbroviation	Access	Initial Value		
CAN0	CAN1	- Register	Abbreviation Access				
003A88н	003C88н				XXXXXXXXB		
to	to	Data register 1 (8 bytes)	DTR1	R/W	to		
003A8Fн	003C8Fн				XXXXXXXXB		
003A90н	003С90н				XXXXXXXXB		
to	to	Data register 2 (8 bytes)	DTR2	R/W	to		
003А97н	003С97н				XXXXXXXXB		
003А98н	003C98н		DTDA	D 444	XXXXXXXB		
t0 00240E	t0	Data register 3 (8 bytes)	DIR3	R/W			
003A9FH	003C9FH						
003AA0H	003CA0H	Data register 4 (8 bytes)					
		Data legister 4 (o bytes)	DTR4	D/ W			
003448	003CA8						
to	to	Data register 5 (8 bytes)	DTR5	R/W	to		
003AAFH	003CAFH		Dinto		XXXXXXXB		
003AB0H	003CB0H				XXXXXXXAB		
to	to	Data register 6 (8 bytes)	DTR6	R/W	to		
003AB7н	003CB7н				XXXXXXXXB		
003АВ8н	003CB8H				XXXXXXXXB		
to	to	Data register 7 (8 bytes)	DTR7	R/W	to		
003ABFн	003CBFн				XXXXXXXXB		
003AC0н	003СС0н		DTR8	R/W	XXXXXXXXB		
to	to	Data register 8 (8 bytes)			to		
003АС7н	003CC7н				XXXXXXXB		
003AC8H	003CC8н		DTDO	DAA	XXXXXXXB		
		Data register 9 (8 bytes)	DIR9	R/W			
to	to	Data register 10 (8 bytes)	DTR10	R/W	to		
003AD7H	003CD7H		BIRIO	r/ v v	XXXXXXXB		
003AD8H	003CD8H				XXXXXXXAB		
to	to	Data register 11 (8 bytes)	DTR11	R/W	to		
003ADFH	003CDFн				XXXXXXXAB		
003AE0н	003CE0H				XXXXXXXXB		
to	to	Data register 12 (8 bytes)	DTR12	R/W	to		
003AE7н	003CE7н				XXXXXXXXB		
003AE8H	003CE8H				XXXXXXXB		
to	to	Data register 13 (8 bytes)	DTR13	R/W	to		
003AEFH	003CEFH				XXXXXXXXB		
003AF0H	003CF0H	Data register 14 (9 hites)		D ///			
003AF7	003CF7	Data register 14 (6 bytes)		r./ VV			
002459	003059						
to	to	Data register 15 (8 bytes)	DTR15	R/W	to		
003AFFH	003CFFH				XXXXXXXB		
	1						



(Continued)

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V \text{ to } 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ °C to } +105 \text{ °C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10\%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ °C to } +105 \text{ °C})

Deremeter	Symbol	Din nome	Value			Unito	Bemerke
Parameter	Symbol	Pin name	Min	Тур	Max	Units	Remarks
			62.5	_	333	ns	No multiplier When using an oscillator circuit $V_{cc} = 5.0 V \pm 10\%$
			62.5	_	125	ns	PLL multiplied by 1 When using an oscillator circuit $V_{CC} = 5.0 V \pm 10\%$
			125		250	ns	PLL multiplied by 2 When using an oscillator circuit $V_{CC} = 5.0 \text{ V} \pm 10\%$
			187.5		333	ns	PLL multiplied by 3 When using an oscillator circuit $V_{CC} = 5.0 \text{ V} \pm 10\%$
Clock cycle time	tcy∟	X0, X1	250		333	ns	PLL multiplied by 4 When using an oscillator circuit $V_{CC} = 5.0 V \pm 10\%$
			200	_	333	ns	When using an oscillator circuit Vcc < 4.5 V(MB90F548GL(S)/543G(S)/ 547G(S)/548G(S))
			62.5	_	333	ns	No multiplier When using an external clock
			62.5	_	125	ns	PLL multiplied by 1 When using an external clock
			125		250	ns	PLL multiplied by 2 When using an external clock
			187.5		333	ns	PLL multiplied by 3 When using an external clock
			250	_	333	ns	PLL multiplied by 4 When using an external clock
	t LCYL	X0A, X1A	-	30.5	-	μs	
Input clock pulse width	Pwh, Pwl	X0	10		—	ns	Duty ratio is about 20^{0} /2 to 70^{0} /2
	Pwlh, Pwll	X0A	-	15.2	-	μs	
Input clock rise and fall time	tcr, tcf	X0	_	_	5	ns	When using an external clock
Machine clock frequency	fср	_	1.5	_	16	MHz	When using main clock
	f LCP	-	_	8.192	_	kHz	When using sub-clock
Machina clack avela tima	t _{CP}	_	62.5	_	666	ns	When using main clock
machine clock cycle lime	t LCP	_	_	122.1	_	μs	When using sub-clock









11.4.7 Ready Input Timing

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40 \text{ }^{\circ}\text{C to } + 105 \text{ }^{\circ}\text{C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40 \text{ }^{\circ}\text{C to } + 105 \text{ }^{\circ}\text{C})

Parameter	Symbol Pin name		Condition	Value		Units	Pomarks
	Symbol	Finitianie	Condition	Min	Max	Units	Nemarks
RDY setup time	tryhs	RDY		45	-	ns	
RDY hold time	tryнн	RDY	_	0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.





11.4.8 Hold Timing

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V \text{ to } 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ }^{\circ}\text{C} \text{ to } + 105 \text{ }^{\circ}\text{C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10\%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ }^{\circ}\text{C} \text{ to } + 105 \text{ }^{\circ}\text{C})

Parameter	Symbol	Din namo	Condition	Value		Unite	Pomarks
	Symbol	Fininanie	Condition	Min	Max	Units	Remarks
Pin floating $\rightarrow \overline{\text{HAK}}\downarrow$ time	t xhal	HAK		30	tcp	ns	
$\overline{\text{HAK}}$ time \rightarrow Pin valid time	tнанv	HAK		t _{CP}	2 tcp	ns	

Note : There is more than 1 cycle from the time HRQ is read to the time the \overline{HAK} is changed.



11.4.9 UART0/1, Serial I/O Timing

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V \text{ to } 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ °C to } + 105 \text{ °C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ °C to } + 105 \text{ °C})

Boromotor	Symbol	Din nomo	Condition	Value		dition Value		Unito	Bomorko
Farameter	Symbol	Fin hame	Condition	Min	Max	Units	Remarks		
Serial clock cycle time	tscyc	SCK0 to SCK2		8 tcp	-	ns			
$SCK \downarrow \to SOT$ delay time	tslov	SCK0 to SCK2, SOT0 to SOT2	Internal clock operation	- 80	80	ns			
Valid SIN \rightarrow SCK [↑]	tıvsн	SCK0 to SCK2, SIN0 to SIN2	output pins are $C_{L} = 80$ pF + 1 TTL.	100	_	ns			
$SCK^{\uparrow} \to Valid SIN hold time$	tsнix	SCK0 to SCK2, SIN0 to SIN2		60	_	ns			
Serial clock "H" pulse width	tshsL	SCK0 to SCK2		4 t _{CP}	-	ns			
Serial clock "L" pulse width	tslsh	SCK0 to SCK2		4 tcp	-	ns			
$SCK \downarrow \to SOT$ delay time	tslov	SCK0 to SCK2, SOT0 to SOT2	External clock operation output pins are $C_{L} = 80$	_	150	ns			
Valid SIN \rightarrow SCK [↑]	tıvsн	SCK0 to SCK2, SIN0 to SIN2	pF + 1 TTL.	60	_	ns			
$SCK^{\uparrow} \rightarrow Valid SIN hold time$	tsніх	SCK0 to SCK2, SIN0 to SIN2		60	_	ns			

Notes :

- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- For tcp (Machine clock cycle time), refer to "(1) Clock Timing".



11.4.10 Timer Input Timing

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V \text{ to } 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ }^{\circ}\text{C} \text{ to } +105 \text{ }^{\circ}\text{C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10\%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ }^{\circ}\text{C} \text{ to } +105 \text{ }^{\circ}\text{C})

Parameter	Symbol	Pin name	Condition	Value		Unite	Bomorko
				Min	Max	Units	Nemarks
Input pulse width	tтіwн	TIN0, TIN1	_	4 tcp	_	ns	
	t⊤ıw∟	IN0 to IN7					



11.4.11 Timer Output Timing

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V \text{ to } 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ °C to } + 105 \text{ °C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ °C to } + 105 \text{ °C})

Parameter	Symbol	Pin name	Condition	Value		Unite	Bomarks
Falameter				Min	Max	Units	Remarks
$CLK\uparrow \rightarrow T_{OUT}$ change time	tто	TOT0 , TOT1, PPG0 to PPG3	_	30	_	ns	











Power supply current (MB90F549G)





13. Ordering Information

Part number	Package	Remarks
MB90F543GPF		
MB90F543GSPF		
MB90F546GPF		
MB90F546GSPF		
MB90F548GPF		
MB90F548GSPF		
MB90F548GLPF		
MB90F548GLSPF		
MB90F549GPF	100-pin Plastic QFP	
MB90F549GSPF	(FPT-100P-M06)	
MB90543GPF		
MB90543GSPF		
MB90547GPF		
MB90547GSPF		
MB90548GPF		
MB90548GSPF		
MB90549GPF		
MB90549GSPF		
MB90F543GPMC		
MB90F543GSPMC		
MB90F546GPMC		
MB90F546GSPMC		
MB90F548GPMC		
MB90F548GSPMC		
MB90F548GLPMC		
MB90F548GLSPMC		
MB90F549GPMC	100-pin Plastic LQFP	
MB90F549GSPMC	(FPT-100P-M20)	
MB90543GPMC		
MB90543GSPMC		
MB90547GPMC		
MB90547GSPMC		
MB90548GPMC		
MB90548GSPMC		
MB90549GPMC		
MB90549GSPMC		





15. Major Changes

Spansion Publication Number: DS07-13703-7E

Section	Change Results			
■ PRODUCT LINEUP	Changed the name in peripheral resource.			
	16-bit I/O Timer \rightarrow 16-bit Free-run Timer			
■ I/O CIRCUIT TYPE	Changed the name of input typ.			
	Hysteresis \rightarrow CMOS Hysteresis			
	$HYS \rightarrow CMOS Hysteresis$			
■ BLOCK DIAGRAM	Changed the arrow direction of SOT1 signal at UART1(SCI). " $\leftarrow \rightarrow$ " (input/output) \rightarrow " \leftarrow " (output)			
■ I/O MAP	Changed the text of "Note".			
■ INTERRUPT MAP	Changed the name of peripheral resource of the pin number: #19.			
	I/O Timer \rightarrow 16-bit Free-run Timer			
ELECTRICAL CHARACTERISTICS 2. Recommended Conditions	Changed the remarks of "parameter: Power supply voltage".			
3. DC Characteristics	Changed the maximum value of symbol : VILM of parameter: Input voltage. Vcc + 0.3 \rightarrow Vss + 0.3			
	Added the following remarks for parameter : Pull-down resistance. Except Flash device			
4. AC Characteristics (1) Clock Timing	Added the value when using an external clock in Oscillation frequency and Clock cycle time on (1) Clock Timing for parameter.			
	Added the item of A/D converter operation range in figure of " Guaranteed PLL operation range"			
(3) Reset and Hardware Standby Input Timing	Changed the following item.			
	(3) Reset and Hardware Standby Input Timing Remarks:			
	$2t_{CP} \rightarrow 2t_{LCP}$			
(4) Power On Reset	Changed as follows;			
	Due to repetitive operation \rightarrow Waiting time until power-on			
5. A/D Converter	Changed the unit of Zero transition voltage and Full scale transition voltage. mV \rightarrow V			
ORDERING INFORMATION	Added the MB90F548GLPMC in Part Numbers.			

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: MB90F543G(S)/546G(S)/548G(S)/549G(S)/549G(S)/V540G/MB90543G(S)/547G(S)/548G(S)/F548GL(S) CMOS F2MC-16LX MB90540G/545G Series 16-bit Proprietary Microcontroller Document Number: 002-07696 Orig. of Change Submission Revision ECN **Description of Change** Date ** Migrated to Cypress and assigned document number 002-07696. No change to document contents or format. AKIH 11/13/2008 _ *A 5537115 AKIH 11/30/2016 Updated to Cypress template



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