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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

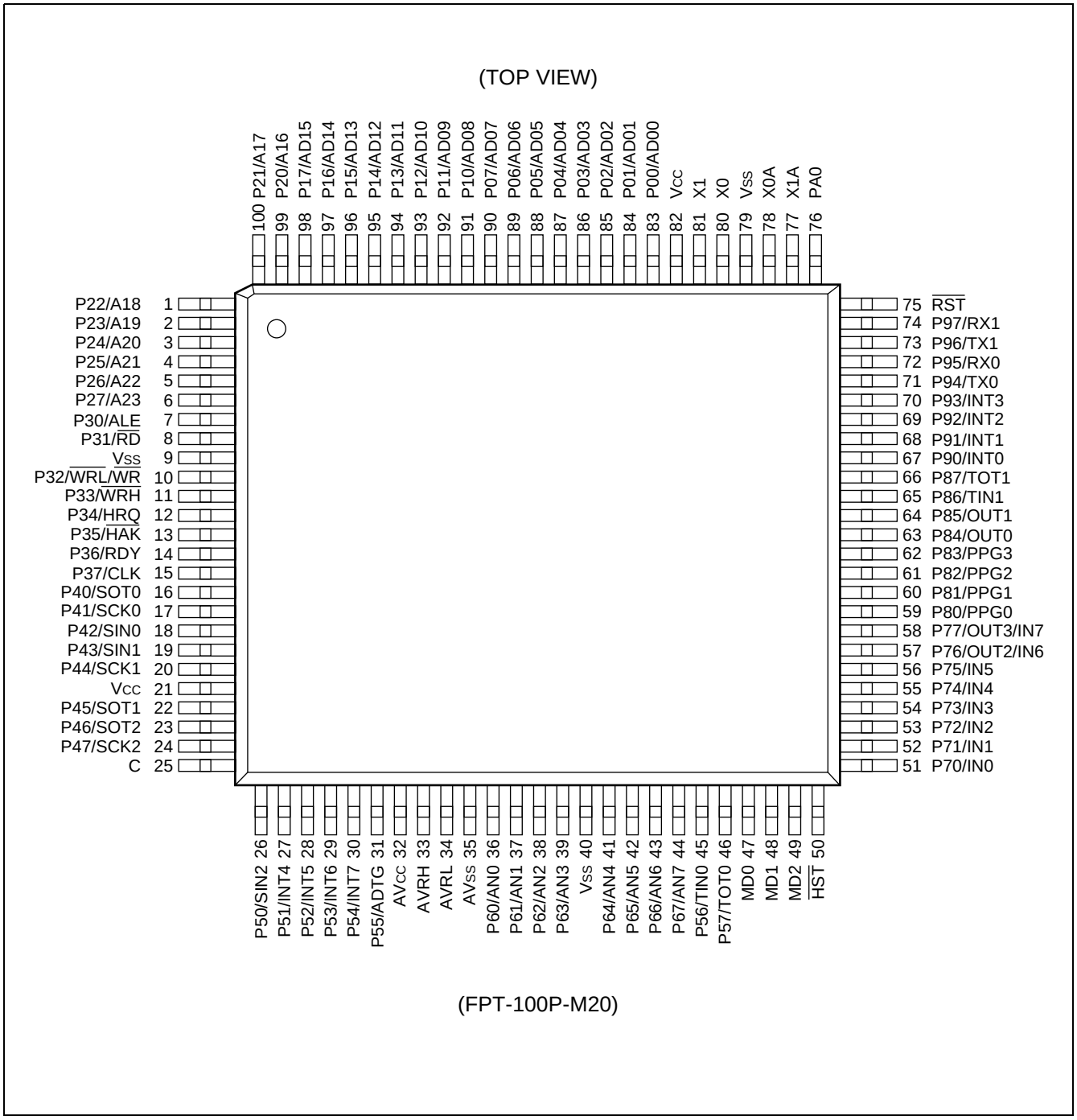
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543gspmc-ge1

*2 : It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*3 : Operating Voltage Range

Products	Operation guarantee range
MB90F543G(S)/F546G(S)/F548G(S)/ MB90549G(S)/F549G(S)/V540/V540G	4.5 V to 5.5 V
MB90F548GL(S)/543G(S)/547G(S)/548G(S)	3.5 V to 5.5 V


(TOP VIEW)
100 P21/A17
99 P20/A16
98 P17/AD15
97 P16/AD14
96 P15/AD13
95 P14/AD12
94 P13/AD11
93 P12/AD10
92 P11/AD09
91 P10/AD08
90 P07/AD07
89 P06/AD06
88 P05/AD05
87 P04/AD04
86 P03/AD03
85 P02/AD02
84 P01/AD01
83 P00/AD00
82 VCC
81 X1
80 X0
79 VSS
78 X0A
77 X1A
76 PA0
P22/A18 1
P23/A19 2
P24/A20 3
P25/A21 4
P26/A22 5
P27/A23 6
P30/ALE 7
P31/RD 8
VSS 9
P32/WRL/WR 10
P33/WRH 11
P34/HRQ 12
P35/HAK 13
P36/RDY 14
P37/CLK 15
P40/SOT0 16
P41/SCK0 17
P42/SIN0 18
P43/SIN1 19
P44/SCK1 20
VCC 21
P45/SOT1 22
P46/SOT2 23
P47/SCK2 24
C 25
75 RST
74 P97/RX1
73 P96/TX1
72 P95/RX0
71 P94/TX0
70 P93/INT3
69 P92/INT2
68 P91/INT1
67 P90/INT0
66 P87/TOT1
65 P86/TIN1
64 P85/OUT1
63 P84/OUT0
62 P83/PPG3
61 P82/PPG2
60 P81/PPG1
59 P80/PPG0
58 P77/OUT3/IN7
57 P76/OUT2/IN6
56 P75/IN5
55 P74/IN4
54 P73/IN3
53 P72/IN2
52 P71/IN1
51 P70/IN0
P50/SIN2 26
P51/INT4 27
P52/INT5 28
P53/INT6 29
P54/INT7 30
P55/ADTG 31
AVCC 32
AVRH 33
AVRL 34
AVSS 35
P60/AN0 36
P61/AN1 37
P62/AN2 38
P63/AN3 39
VSS 40
P64/AN4 41
P65/AN5 42
P66/AN6 43
P67/AN7 44
P56/TIN0 45
P57/TOT0 46
MD0 47
MD1 48
MD2 49
HST 50

(FPT-100P-M20)

3. Pin Description

Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
80 81	82 83	X0 X1	A (Oscillation)	High speed crystal oscillator input pins
78	80	X0A	A (Oscillation)	Low speed crystal oscillator input pins. For the one clock system parts, perfom external pull-down processing.
77	79	X1A		Low speed crystal oscillator input pins. For the one clock system parts, leave it open.
75	77	$\overline{\text{RST}}$	B	External reset request input pin
50	52	$\overline{\text{HST}}$	C	Hardware standby input pin
83 to 90	85 to 92	P00 to P07	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
91 to 98	93 to 100	P10 to P17	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		AD08 to AD15		I/O pins for 8 higher bits of the external address/data bus. This function is enabled when the external bus is enabled.
99 to 6	1 to 8	P20 to P27	I	General I/O port with programmable pullup. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to “1”.
		A16 to A23		8-bit I/O pins for A16 to A23 at the external address/data bus. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to “0”.
7	9	P30	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
8	10	P31	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		$\overline{\text{RD}}$		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.
10	12	P32	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the $\overline{\text{WR}}$/$\overline{\text{WRL}}$ pin output is disabled.
		$\overline{\text{WRL}}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{\text{WR}}$/$\overline{\text{WRL}}$ pin output are enabled. $\overline{\text{WRL}}$ is write-strobe output pin for the lower 8 bits of the data bus in 16-bit access. $\overline{\text{WR}}$ is write-strobe output pin for the 8 bits of the data bus in 8-bit access.
		$\overline{\text{WR}}$		

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Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
72	74	P95	D	General I/O port. This function is always enabled.
		RX0		RX input pin for CAN0 Interface. When the CAN function is used, output from the other functions must be stopped.
73	75	P96	D	General I/O port. This function is enabled when CAN1 disables the output.
		TX1		TX output pin for CAN1. This function is enabled when CAN1 enables the output (only MB90540G series) .
74	76	P97	D	General I/O port. This function is always enabled.
		RX1		RX input pin for CAN1 Interface. When the CAN function is used, output from the other functions must be stopped (only MB90540G series) .
76	78	PA0	D	General I/O port. This function is always enabled.
32	34	AV_{CC}	Power supply	Power supply pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AV_{CC} is applied to V_{CC}.
35	37	AV_{SS}	Power supply	Power supply pin for the A/D Converter.
33	35	AVRH	Power supply	External reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV_{CC}.
34	36	AVRL	Power supply	External reference voltage input pin for the A/D Converter.
47, 48	49, 50	MD0, MD1	C	Input pins for specifying the operating mode. The pins must be directly connected to V_{CC} or V_{SS}.
49	51	MD2	F	Input pin for specifying the operating mode. The pin must be directly connected to V_{CC} or V_{SS}.
25	27	C	—	Power supply stabilization capacitor pin. It should be connected externally to an 0.1 µF ceramic capacitor.
21, 82	23, 84	V_{CC}	Power supply	Input pin for power supply (5.0 V) .
9, 40, 79	11, 42, 81	V_{SS}	Power supply	Input pin for power supply (0.0 V) .

*1 : FPT-100P-M06

*2 : FPT-100P-M20

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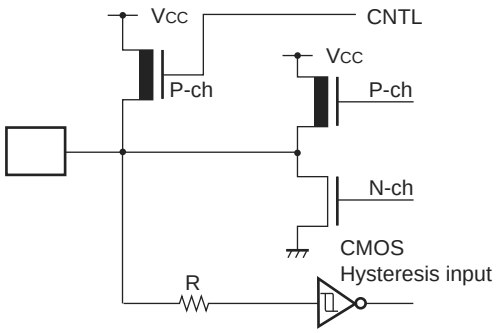
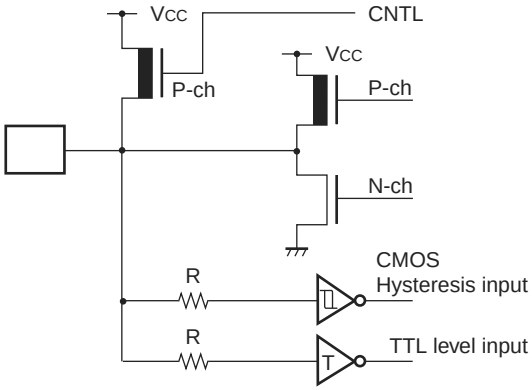
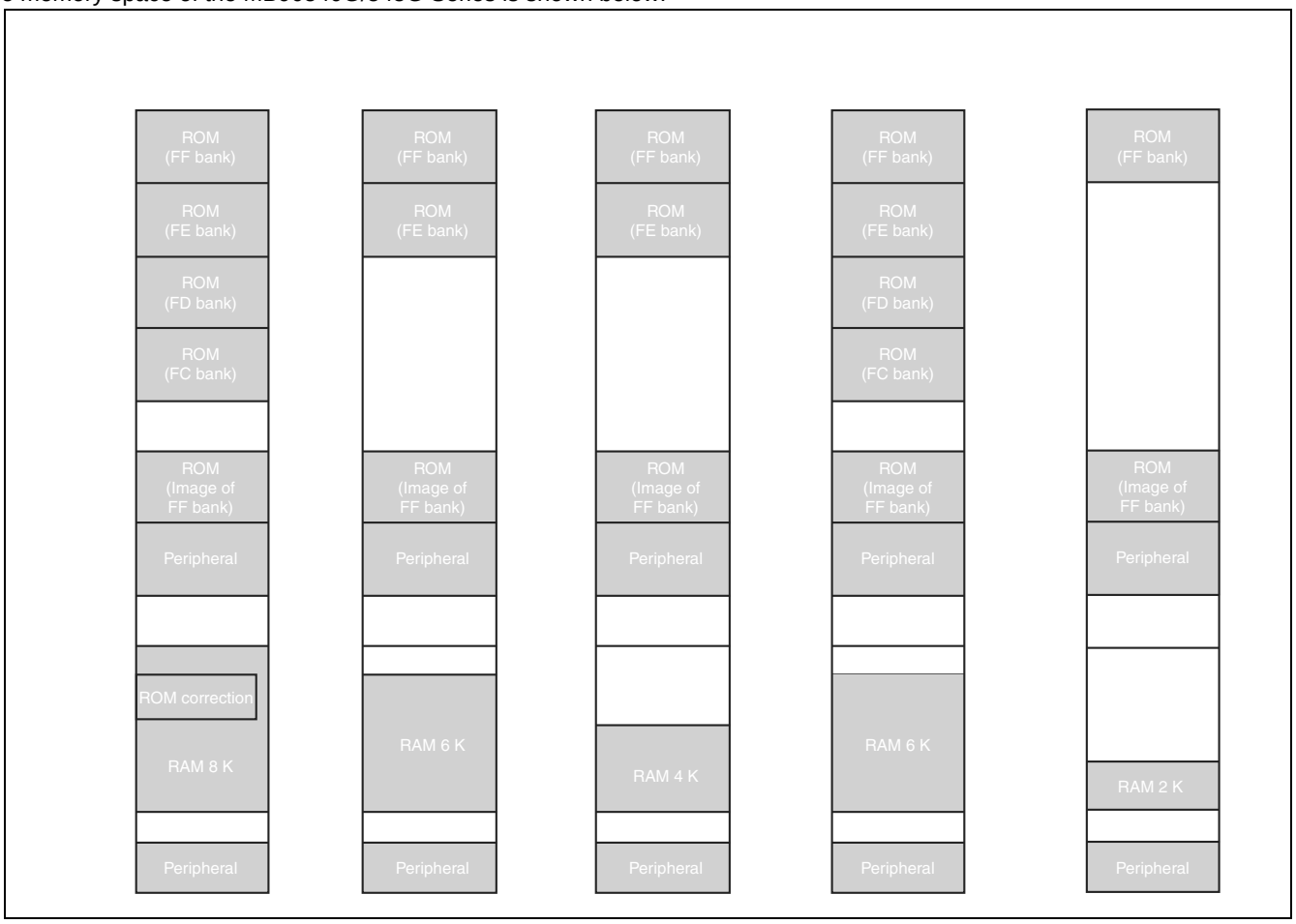
Circuit type	Diagram	Remarks
H		■ CMOS level output ■ CMOS Hysteresis input ■ Programmable pull-up resistor : 50 kΩ approx.
I		■ CMOS level output ■ CMOS Hysteresis input ■ TTL level input (Flash devices in Flash writer mode only) ■ Programmable pullup resistor : 50 kΩ approx.

7. Memory Map

The memory space of the MB90540G/545G Series is shown below.



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits address are the same, the table in ROM can be referenced without using the “far” specification in the pointer declaration.
For example, an attempt to access $00C000_H$ accesses the value at $FFC000_H$ in ROM.The ROM area in bank FF exceeds 48 Kbytes, and its entire image cannot be shown in bank 00.The image between $FF4000_H$ and $FFFFFF_H$ is visible in bank 00, while the image between $FF0000_H$ and $FF3FFF_H$ is visible only in bank FF.

Address	Register	Abbreviation	Access	Resource name	Initial value
$A2_H$ to $A4_H$	Prohibited				
$A5_H$	Automatic ready function select register	ARSR	W	External Memory Access	0 0 1 1 _ _ 0 0_B
$A6_H$	External address output control register	HACR	W		0 0 0 0 0 0 0 0_B
$A7_H$	Bus control signal selection register	ECSR	W		0 0 0 0 0 0 0 $_B$
$A8_H$	Watchdog Timer control register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1_B
$A9_H$	Time Base Timer Control register	TBTC	R/W	Time Base Timer	1 - - 0 0 1 0 0_B
AA_H	Watch timer control register	WTC	R/W	Watch Timer	1 X 0 0 0 0 0 0_B
AB_H to AD_H	Prohibited				
AE_H	Flash memory control status register (Flash only, otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0_B
AF_H	Prohibited				
$B0_H$	Interrupt control register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1_B
$B1_H$	Interrupt control register 01	ICR01	R/W		0 0 0 0 0 1 1 1_B
$B2_H$	Interrupt control register 02	ICR02	R/W		0 0 0 0 0 1 1 1_B
$B3_H$	Interrupt control register 03	ICR03	R/W		0 0 0 0 0 1 1 1_B
$B4_H$	Interrupt control register 04	ICR04	R/W		0 0 0 0 0 1 1 1_B
$B5_H$	Interrupt control register 05	ICR05	R/W		0 0 0 0 0 1 1 1_B
$B6_H$	Interrupt control register 06	ICR06	R/W		0 0 0 0 0 1 1 1_B
$B7_H$	Interrupt control register 07	ICR07	R/W		0 0 0 0 0 1 1 1_B
$B8_H$	Interrupt control register 08	ICR08	R/W		0 0 0 0 0 1 1 1_B
$B9_H$	Interrupt control register 09	ICR09	R/W		0 0 0 0 0 1 1 1_B
BA_H	Interrupt control register 10	ICR10	R/W		0 0 0 0 0 1 1 1_B
BB_H	Interrupt control register 11	ICR11	R/W		0 0 0 0 0 1 1 1_B
BC_H	Interrupt control register 12	ICR12	R/W		0 0 0 0 0 1 1 1_B
BD_H	Interrupt control register 13	ICR13	R/W		0 0 0 0 0 1 1 1_B
BE_H	Interrupt control register 14	ICR14	R/W		0 0 0 0 0 1 1 1_B
BF_H	Interrupt control register 15	ICR15	R/W		0 0 0 0 0 1 1 1_B
$C0_H$ to FF_H	External				

Address	Register	Abbreviation	Access	Resource name	Initial value
$1FF0_H$	Program address detection register 0	PADR0	R/W	Address Match Detection Function	$XXXXXXXX_B$
$1FF1_H$	Program address detection register 0	PADR0	R/W		$XXXXXXXX_B$
$1FF2_H$	Program address detection register 0	PADR0	R/W		$XXXXXXXX_B$
$1FF3_H$	Program address detection register 1	PADR1	R/W		$XXXXXXXX_B$
$1FF4_H$	Program address detection register 1	PADR1	R/W		$XXXXXXXX_B$
$1FF5_H$	Program address detection register 1	PADR1	R/W		$XXXXXXXX_B$

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Address	Register	Abbreviation	Access	Resource name	Initial value
3928H	Output Compare Register 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
3929H	Output Compare Register 0	OCCP0	R/W		XXXXXXXXB
392AH	Output Compare Register 1	OCCP1	R/W		XXXXXXXXB
392BH	Output Compare Register 1	OCCP1	R/W		XXXXXXXXB
392CH	Output Compare Register 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXXB
392DH	Output Compare Register 2	OCCP2	R/W		XXXXXXXXB
392EH	Output Compare Register 3	OCCP3	R/W		XXXXXXXXB
392FH	Output Compare Register 3	OCCP3	R/W		XXXXXXXXB
3930H to 39FFH	Reserved				
3A00H to 3AFFH	Reserved for CAN 0 Interface.				
3B00H to 3BFFH	Reserved for CAN 0 Interface.				
3C00H to 3CFFH	Reserved for CAN 1 Interface.				
3D00H to 3DFFH	Reserved for CAN 1 Interface.				
3E00H to 3FFFH	Reserved				

- Read/write notation
  - R/W : Reading and writing permitted
  - R : Read-only
  - W : Write-only

- Initial value notation
  - 0 : Initial value is “0”.
  - 1 : Initial value is “1”.
  - X : Initial value is undefined.
  - _ : Initial value is unused.

Note: Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

9. CAN Controller

The MB90540G series contains two CAN controllers (CAN0 and CAN1) , the MB90545G series contains only one (CAN0) . The Evaluation Chip MB90V540G also has two CAN controllers.

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 1 Mbps (when input clock is at 16 MHz)

List of Control Registers

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070_H	000080_H	Message buffer valid register	BVALR	R/W	$00000000\ 00000000_B$
000071_H	000081_H				
000072_H	000082_H	Transmit request register	TREQR	R/W	$00000000\ 00000000_B$
000073_H	000083_H				
000074_H	000084_H	Transmit cancel register	TCANR	W	$00000000\ 00000000_B$
000075_H	000085_H				
000076_H	000086_H	Transmit complete register	TCR	R/W	$00000000\ 00000000_B$
000077_H	000087_H				
000078_H	000088_H	Receive complete register	RCR	R/W	$00000000\ 00000000_B$
000079_H	000089_H				
$00007A_H$	$00008A_H$	Remote request receiving register	RRTRR	R/W	$00000000\ 00000000_B$
$00007B_H$	$00008B_H$				
$00007C_H$	$00008C_H$	Receive overrun register	ROVRR	R/W	$00000000\ 00000000_B$
$00007D_H$	$00008D_H$				
$00007E_H$	$00008E_H$	Receive interrupt enable register	RIER	R/W	$00000000\ 00000000_B$
$00007F_H$	$00008F_H$				

(Continued)

10. Interrupt Map

Interrupt cause	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC$_H$	—	—
INT9 instruction	N/A	#09	FFFFD8$_H$	—	—
Exception	N/A	#10	FFFFD4$_H$	—	—
CAN 0 RX	N/A	#11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN 0 TX/NS	N/A	#12	FFFFCC$_H$		
CAN 1 RX	N/A	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 1 TX/NS	N/A	#14	FFFFC4$_H$		
External Interrupt INT0/INT1	*1	#15	FFFFC0$_H$	ICR02	0000B2$_H$
Time Base Timer	N/A	#16	FFFFBC$_H$		
16-bit Reload Timer 0	*1	#17	FFFFB8$_H$	ICR03	0000B3$_H$
8/10-bit A/D Converter	*1	#18	FFFFB4$_H$		
16-bit Free-run Timer	N/A	#19	FFFFB0$_H$	ICR04	0000B4$_H$
External Interrupt INT2/INT3	*1	#20	FFFFAC$_H$		
Serial I/O	*1	#21	FFFFA8$_H$	ICR05	0000B5$_H$
8/16-bit PPG 0/1	N/A	#22	FFFFA4$_H$		
Input Capture 0	*1	#23	FFFFA0$_H$	ICR06	0000B6$_H$
External Interrupt INT4/INT5	*1	#24	FFFF9C$_H$		
Input Capture 1	*1	#25	FFFF98$_H$	ICR07	0000B7$_H$
8/16-bit PPG 2/3	N/A	#26	FFFF94$_H$		
External Interrupt INT6/INT7	*1	#27	FFFF90$_H$	ICR08	0000B8$_H$
Watch Timer	N/A	#28	FFFF8C$_H$		
8/16-bit PPG 4/5	N/A	#29	FFFF88$_H$	ICR09	0000B9$_H$
Input Capture 2/3	*1	#30	FFFF84$_H$		
8/16-bit PPG 6/7	N/A	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 0	*1	#32	FFFF7C$_H$		
Output Compare 1	*1	#33	FFFF78$_H$	ICR11	0000BB$_H$
Input Capture 4/5	*1	#34	FFFF74$_H$		
Output Compare 2/3 - Input Capture 6/7	*1	#35	FFFF70$_H$	ICR12	0000BC$_H$
16-bit Reload Timer 1	*1	#36	FFFF6C$_H$		
UART 0 RX	*2	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 0 TX	*1	#38	FFFF64$_H$		
UART 1 RX	*2	#39	FFFF60$_H$	ICR14	0000BE$_H$
UART 1 TX	*1	#40	FFFF5C$_H$		
Flash Memory	N/A	#41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed interrupt	N/A	#42	FFFF54$_H$		

(Continued)

11.2 Recommended Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value			Units	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.5	5.0	5.5	V	Under normal operation : Other than MB90F548GL(S)/543G(S)/547G(S)/548G(S)
						Under normal operation when A/D conveter is used : MB90F548GL(S)/543G(S)/547G(S)/548G(S)
		3.5	5.0	5.5	V	Under normal operation when A/D conveter is not used : MB90F548GL(S)/543G(S)/547G(S)/548G(S)
		3.0	−	5.5	V	Maintain RAM data in stop mode
Smooth capacitor	C_S	0.022	0.1	1.0	µF	*
Operating temperature	T_A	−40	−	+105	°C	

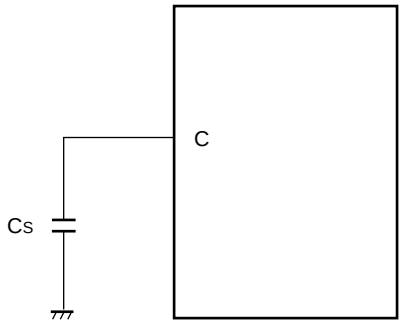
*: Use a ceramic capacitor or a capacitor of better 4. AC characteristics. The bypass capacitor should be greater than this capacitor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

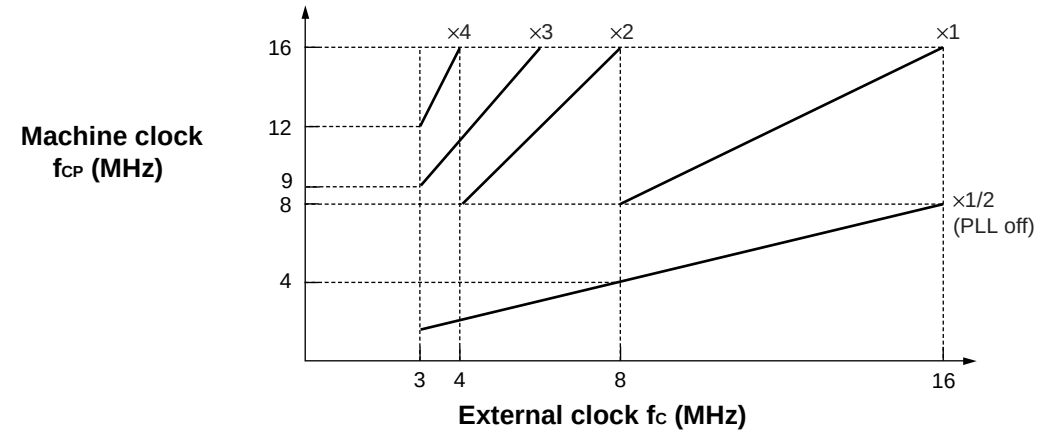
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ **C Pin Connection Diagram**

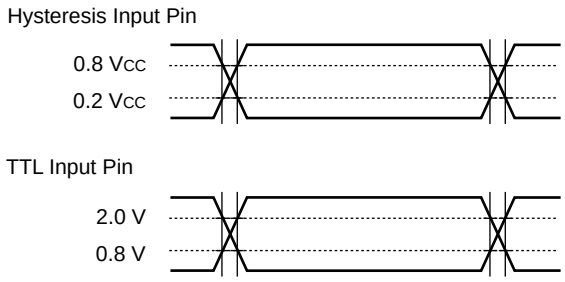


■ **External clock frequency and Machine clock frequency**

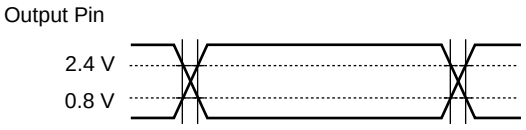


AC characteristics are set to the measured reference voltage values below.

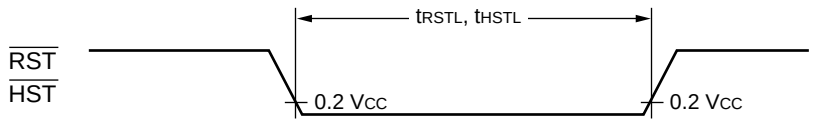
■ **Input signal waveform**



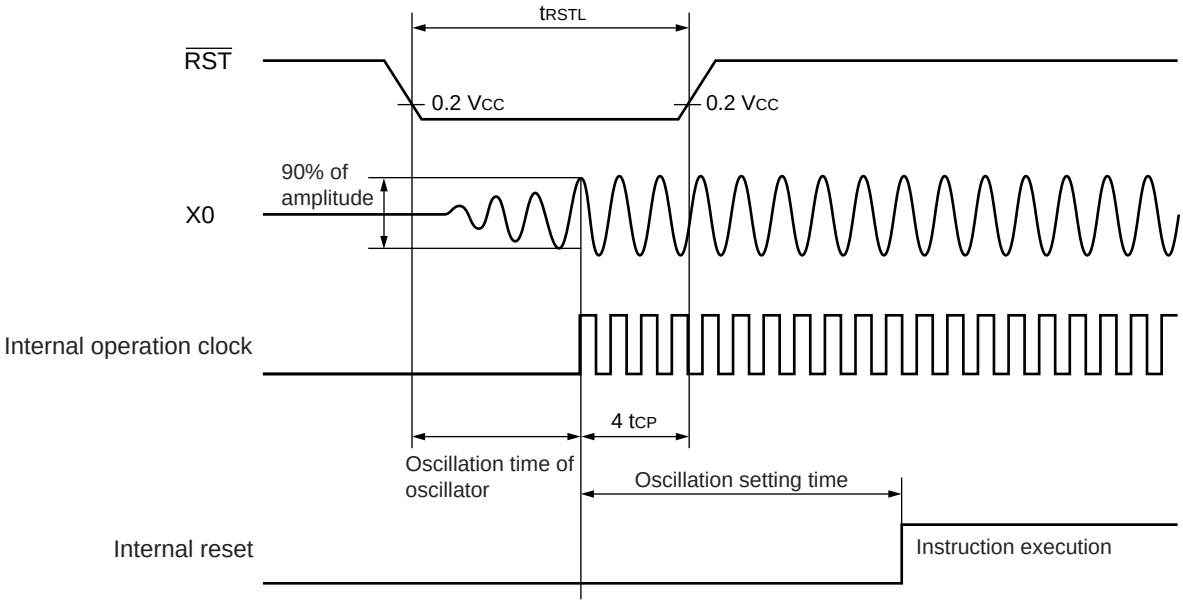
■ **Output signal waveform**



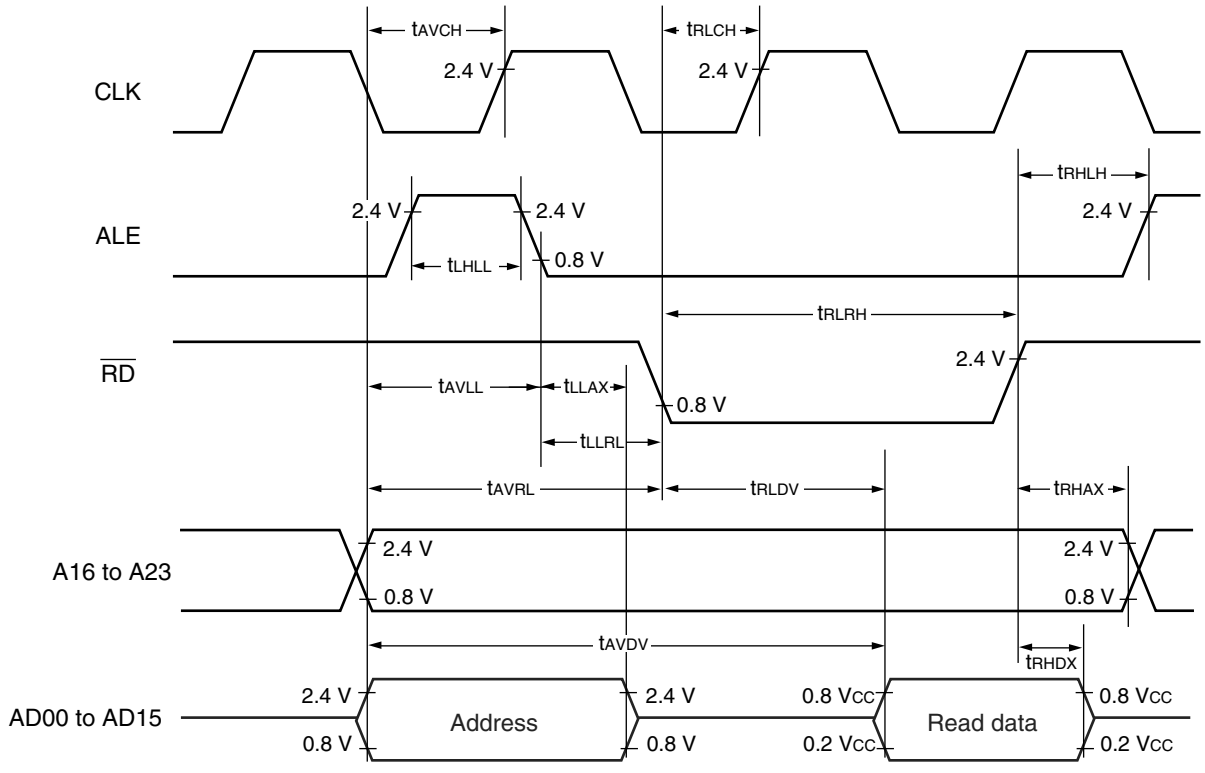
■ In under normal operation, pseudo timer mode, sub-clock mode, sub-sleep mode, timer mode



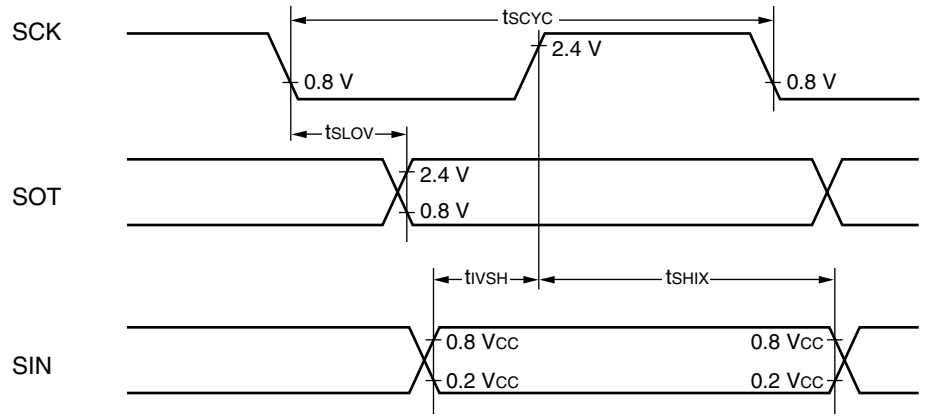
■ In stop mode



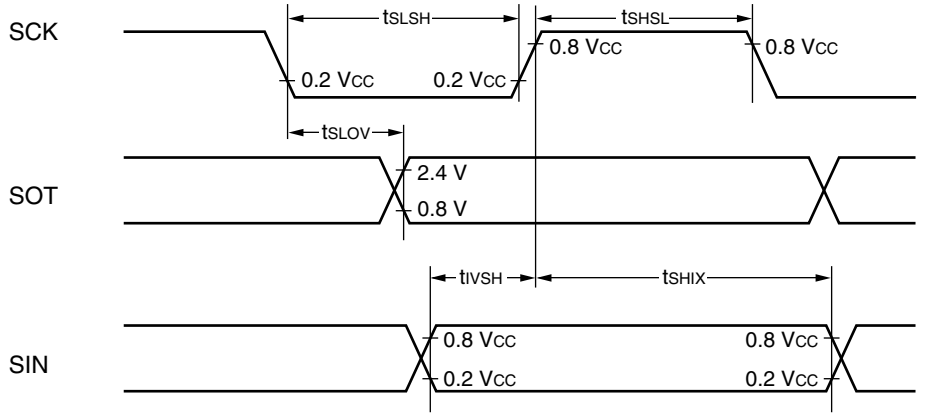
■ **Bus Timing (Read)**



■ Internal Shift Clock Mode



■ External Shift Clock Mode



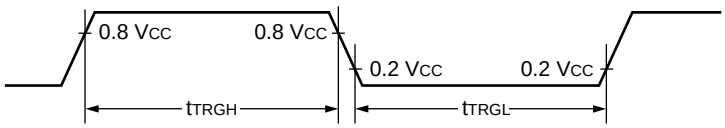
11.4.12 Trigger Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

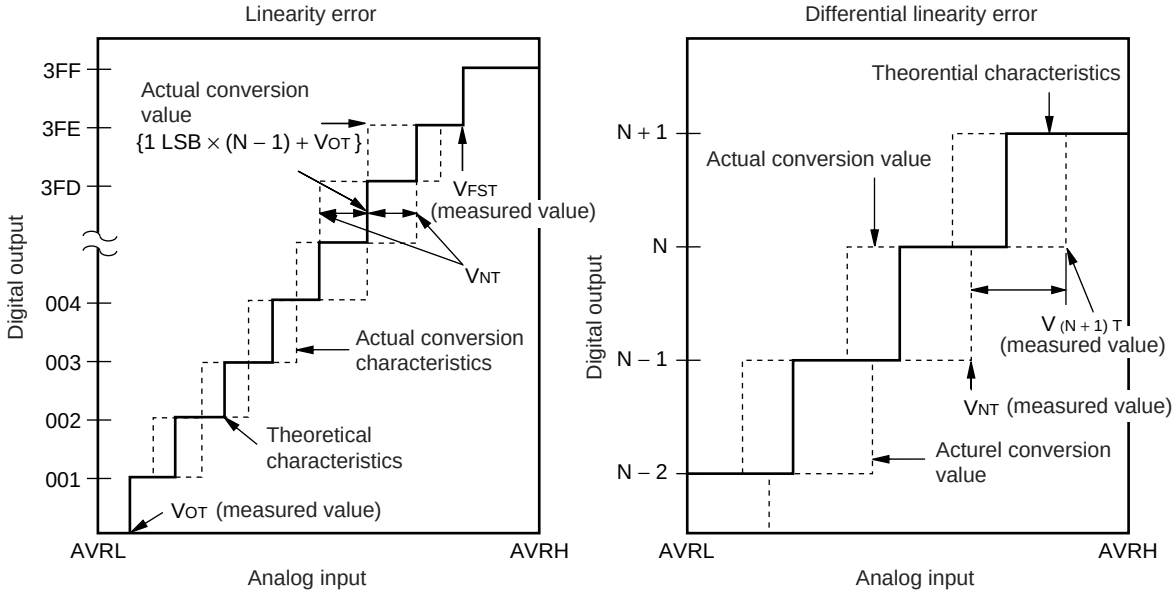
(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT7, ADTG	—	5 t_{CP}	—	ns	Under nomal operation
				1	—	µs	In stop mode

■ **Trigger Input Timing**



(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage at transition of digital output from "000_H" to "001_H"
V_{FST} : Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

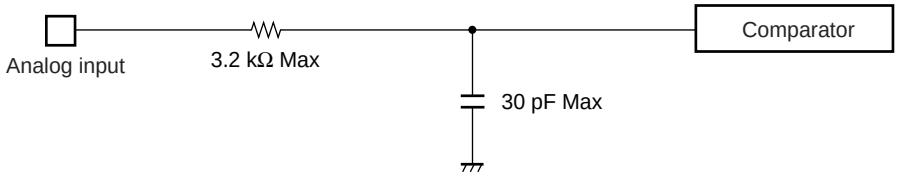
11.5.3 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions, :

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

Note : When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz) .

■ **Equipment of analog input circuit model**

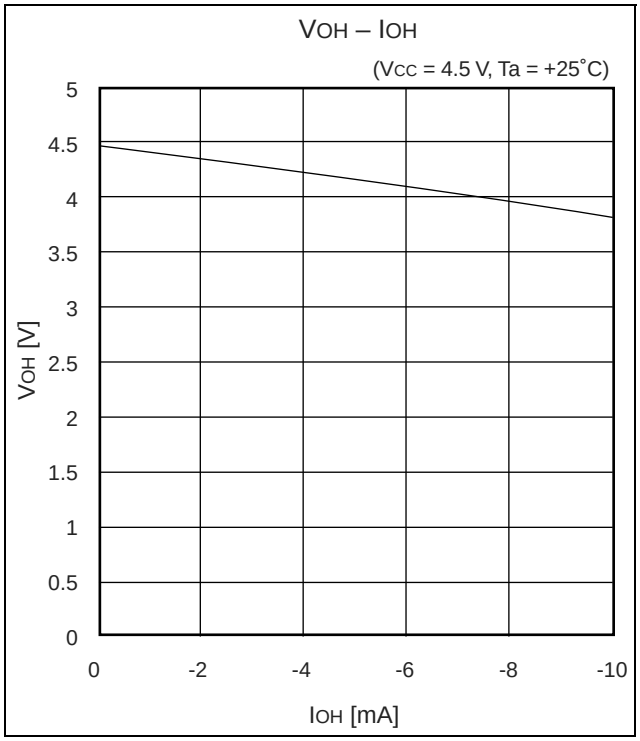


11.5.4 Error

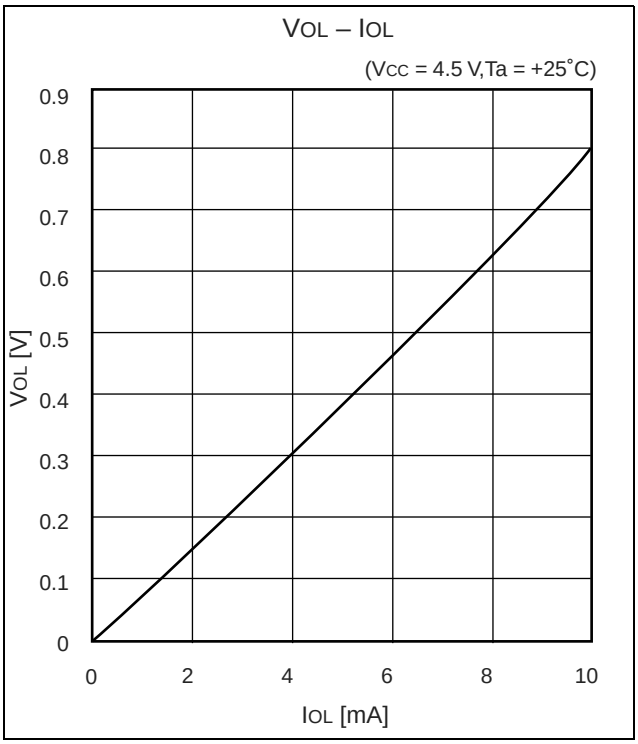
The smaller the | AVRH − AVRL |, the greater the error would become relatively.

12. Example Characteristics

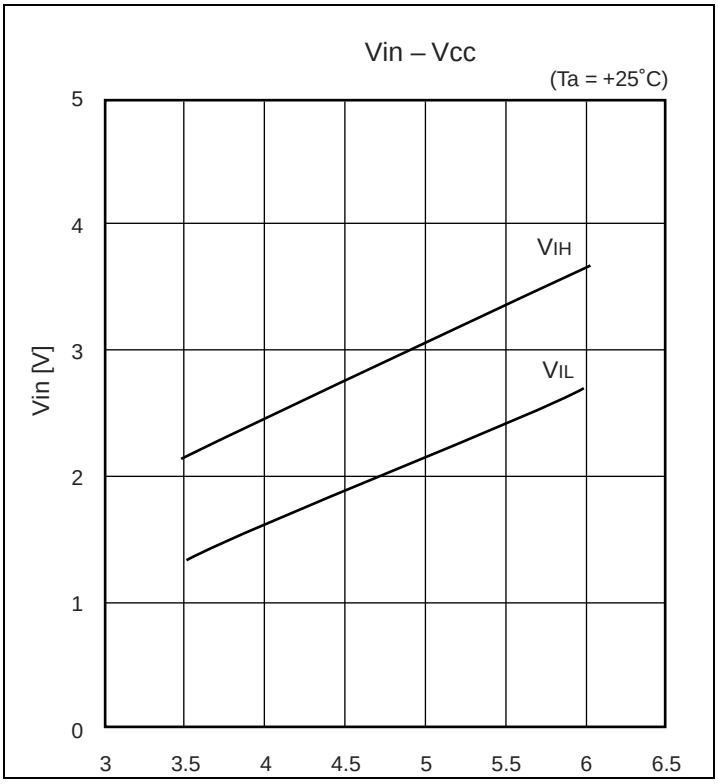
■ “H” level output voltage

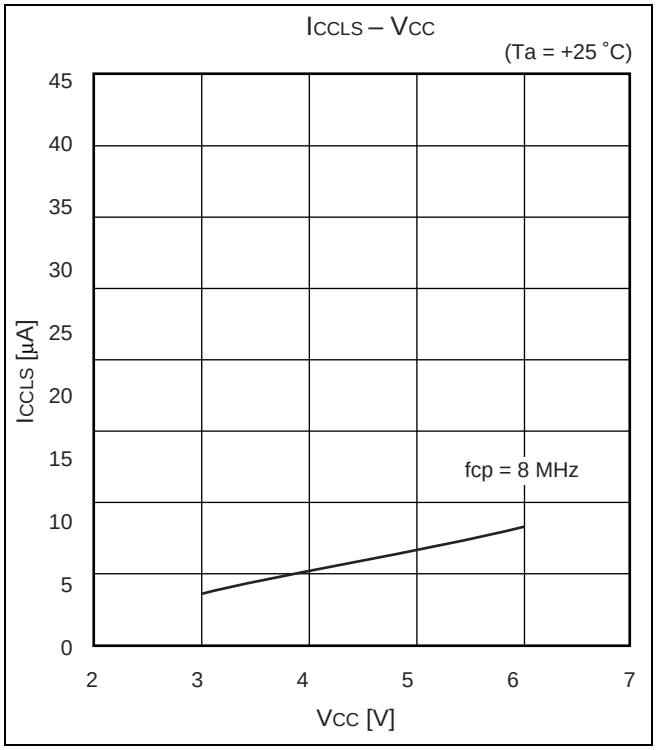


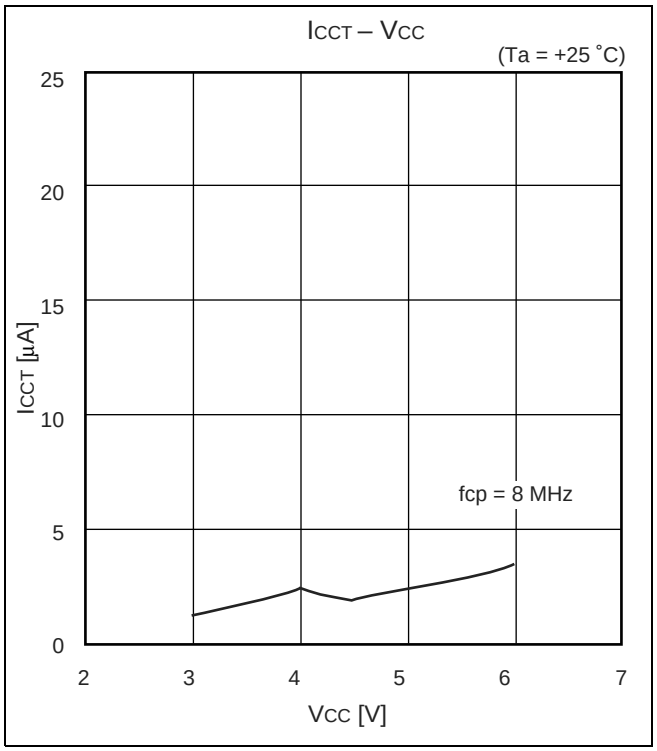
■ “L” level output voltage

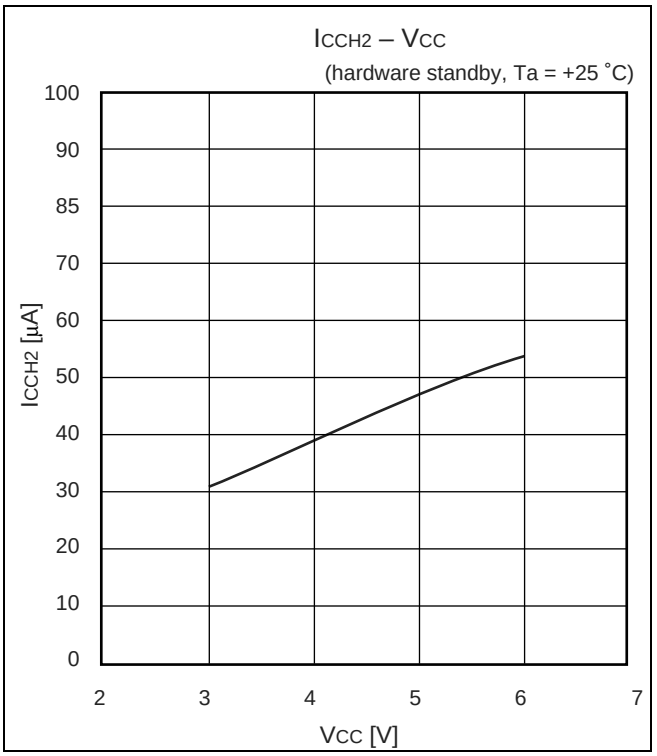


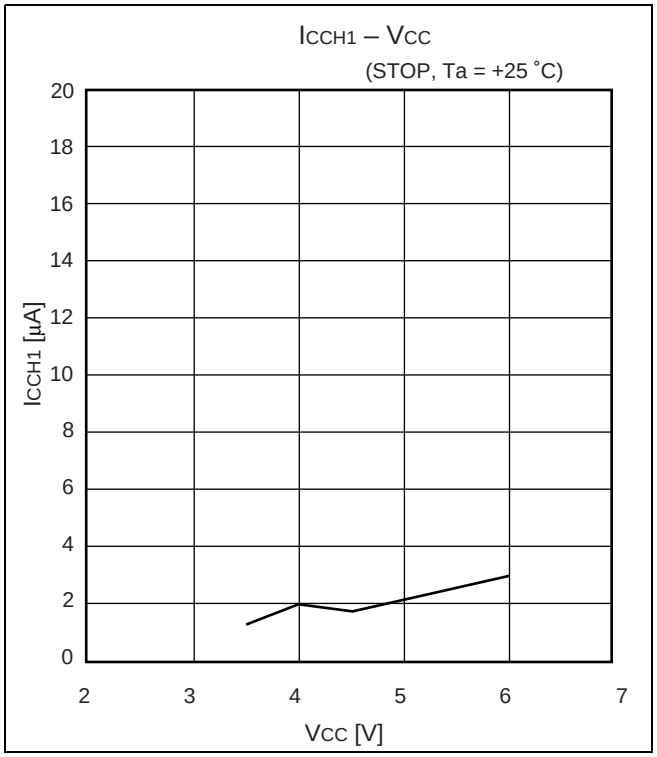
■ “H” level input voltage/ “L” level input voltage (Hysterisis inpiut)




ICCLS – VCC
(Ta = +25 ˚C)
ICCLS [µA]
45
40
35
30
25
20
15
10
5
0
fcp = 8 MHz
2
3
4
5
6
7
VCC [V]


ICCT – VCC
(Ta = +25 ˚C)
ICCT [µA]
25
20
15
10
5
0
fcp = 8 MHz
2
3
4
5
6
7
VCC [V]


ICCH2 – VCC
(hardware standby, Ta = +25 ˚C)
ICCH2 [µA]
100
90
85
70
60
50
40
30
20
10
0
2
3
4
5
6
7
VCC [V]


ICCH1 – VCC
(STOP, Ta = +25 ˚C)
ICCH1 [µA]
20
18
16
14
12
10
8
6
4
2
0
2
3
4
5
6
7
VCC [V]

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