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What is "[Embedded - Microcontrollers](#)"?

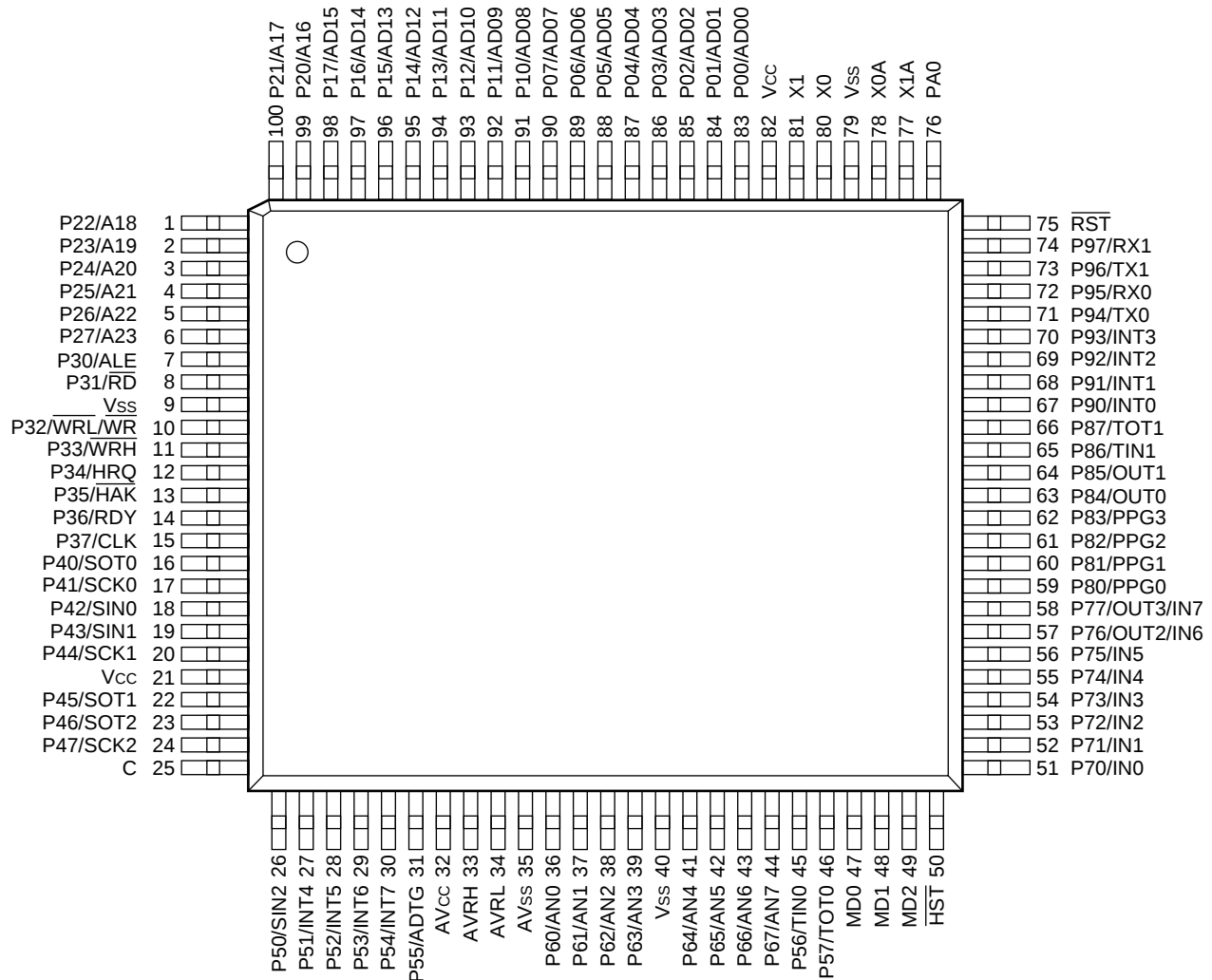
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

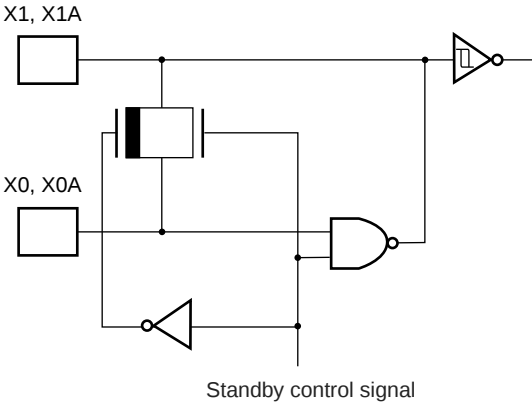
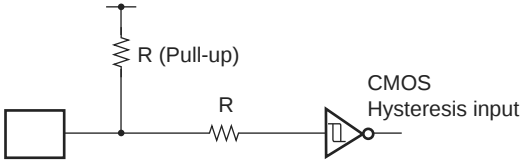
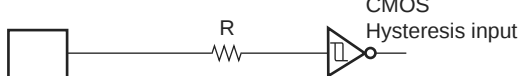
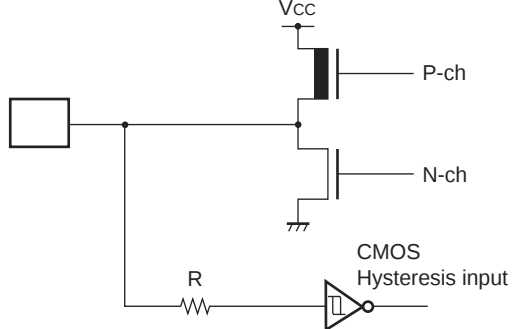
Product Status	Active
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f543pf-g

(TOP VIEW)



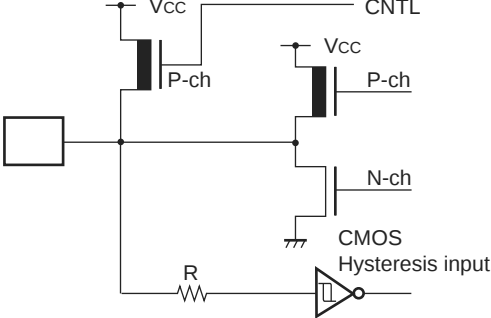
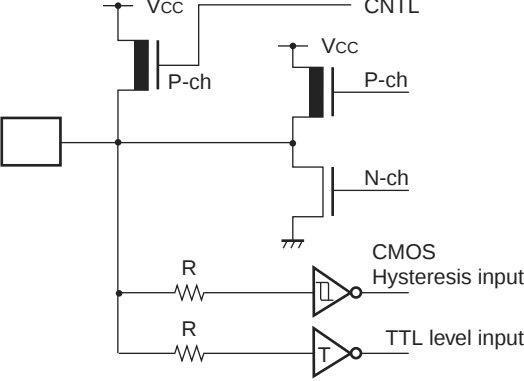
(FPT-100P-M20)

4. I/O Circuit Type

Circuit type	Diagram	Remarks
A	 Standby control signal	■ High-speed oscillation feedback resistor : 1 MΩ approx. ■ Low-speed oscillation feedback resistor: 10 MΩ approx.
B	 R (Pull-up) R CMOS Hysteresis input	■ CMOS Hysteresis input ■ Pull-up resistor : 50 kΩ approx.
C	 R CMOS Hysteresis input	■ CMOS Hysteresis input
D	 Vcc P-ch N-ch CMOS Hysteresis input R	■ CMOS level output ■ CMOS Hysteresis input

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Circuit type	Diagram	Remarks
H		■ CMOS level output ■ CMOS Hysteresis input ■ Programmable pull-up resistor : 50 kΩ approx.
I		■ CMOS level output ■ CMOS Hysteresis input ■ TTL level input (Flash devices in Flash writer mode only) ■ Programmable pullup resistor : 50 kΩ approx.

Address	Register	Abbreviation	Access	Resource name	Initial value
24 _H	Serial mode register 1	SMR1	R/W	UART1	0 0 0 0 0 0 0 0 _B
25 _H	Serial control register 1	SCR1	R/W		0 0 0 0 0 1 0 0 _B
26 _H	Serial input data register 1/ Serial output data register 1	SIDR1/SODR1	R/W		XXXXXXXX _B
27 _H	Serial status register 1	SSR1	R/W		0 0 0 0 1 _ 0 0 _B
28 _H	UART1 prescaler control register	CDCR	R/W		0 _ _ 1 1 1 1 _B
29 _H	Serial Edge select register	SES1	R/W		_ _ _ _ _ 0 _B
2A _H	Prohibited				
2B _H	Serial I/O prescaler	SCDCR	R/W	Extended I/O Serial Interface	0 _ _ 1 1 1 1 _B
2C _H	Serial mode control register	SMCS	R/W		_ _ _ 0 0 0 0 _B
2D _H	Serial mode control register	SMCS	R/W		0 0 0 0 0 1 0 _B
2E _H	Serial data register	SDR	R/W		XXXXXXXX _B
2F _H	Serial Edge select register	SES2	R/W		_ _ _ _ _ 0 _B
30 _H	External interrupt enable register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0 _B
31 _H	External interrupt request register	EIRR	R/W		XXXXXXXX _B
32 _H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0 _B
33 _H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0 _B
34 _H	A/D control status register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0 _B
35 _H	A/D control status register 1	ADCS1	R/W		0 0 0 0 0 0 0 0 _B
36 _H	A/D data register 0	ADCR0	R		XXXXXXXX _B
37 _H	A/D data register 1	ADCR1	R/W		0 0 0 0 1 _ XX _B
38 _H	PPG0 operation mode control register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 _ _ 1 _B
39 _H	PPG1 operation mode control register	PPGC1	R/W		0 _ 0 0 0 0 1 _B
3A _H	PPG0/1 clock selection register	PPG01	R/W		0 0 0 0 0 _ _ _B
3B _H	Prohibited				
3C _H	PPG2 operation mode control register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 _ _ 1 _B
3D _H	PPG3 operation mode control register	PPGC3	R/W		0 _ 0 0 0 0 1 _B
3E _H	PPG2/3 Clock Selection Register	PPG23	R/W		0 0 0 0 0 _ _ _B
3F _H	Prohibited				
40 _H	PPG4 operation mode control register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 _ _ 1 _B
41 _H	PPG5 operation mode control register	PPGC5	R/W		0 _ 0 0 0 0 1 _B
42 _H	PPG4/5 clock selection register	PPG45	R/W		0 0 0 0 0 _ _ _B
43 _H	Prohibited				
44 _H	PPG6 operation mode control register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 _ _ 1 _B
45 _H	PPG7 operation mode control register	PPGC7	R/W		0 _ 0 0 0 0 1 _B
46 _H	PPG6/7 clock selection register	PPG67	R/W		0 0 0 0 0 _ _ _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
3900 _H	Reload L	PRLLO	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX _B
3901 _H	Reload H	PRLH0	R/W		XXXXXXXX _B
3902 _H	Reload L	PRLLO	R/W		XXXXXXXX _B
3903 _H	Reload H	PRLH1	R/W		XXXXXXXX _B
3904 _H	Reload L	PRLLO	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX _B
3905 _H	Reload H	PRLH2	R/W		XXXXXXXX _B
3906 _H	Reload L	PRLLO	R/W		XXXXXXXX _B
3907 _H	Reload H	PRLH3	R/W		XXXXXXXX _B
3908 _H	Reload L	PRLLO	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX _B
3909 _H	Reload H	PRLH4	R/W		XXXXXXXX _B
390A _H	Reload L	PRLLO	R/W		XXXXXXXX _B
390B _H	Reload H	PRLH5	R/W		XXXXXXXX _B
390C _H	Reload L	PRLLO	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX _B
390D _H	Reload H	PRLH6	R/W		XXXXXXXX _B
390E _H	Reload L	PRLLO	R/W		XXXXXXXX _B
390F _H	Reload H	PRLH7	R/W		XXXXXXXX _B
3910 _H to 3917 _H	Reserved				
3918 _H	Input Capture Register 0	IPCP0	R	Input Capture 0/1	XXXXXXXX _B
3919 _H	Input Capture Register 0	IPCP0	R		XXXXXXXX _B
391A _H	Input Capture Register 1	IPCP1	R		XXXXXXXX _B
391B _H	Input Capture Register 1	IPCP1	R		XXXXXXXX _B
391C _H	Input Capture Register 2	IPCP2	R	Input Capture 2/3	XXXXXXXX _B
391D _H	Input Capture Register 2	IPCP2	R		XXXXXXXX _B
391E _H	Input Capture Register 3	IPCP3	R		XXXXXXXX _B
391F _H	Input Capture Register 3	IPCP3	R		XXXXXXXX _B
3920 _H	Input Capture Register 4	IPCP4	R	Input Capture 4/5	XXXXXXXX _B
3921 _H	Input Capture Register 4	IPCP4	R		XXXXXXXX _B
3922 _H	Input Capture Register 5	IPCP5	R		XXXXXXXX _B
3923 _H	Input Capture Register 5	IPCP5	R		XXXXXXXX _B
3924 _H	Input Capture Register 6	IPCP6	R	Input Capture 6/7	XXXXXXXX _B
3925 _H	Input Capture Register 6	IPCP6	R		XXXXXXXX _B
3926 _H	Input Capture Register 7	IPCP7	R		XXXXXXXX _B
3927 _H	Input Capture Register 7	IPCP7	R		XXXXXXXX _B

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A3C _H	003C3C _H	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX _B
003A3D _H	003C3D _H				
003A3E _H	003C3E _H				XXXXX--- XXXXXXXX _B
003A3F _H	003C3F _H				
003A40 _H	003C40 _H	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX _B
003A41 _H	003C41 _H				
003A42 _H	003C42 _H				XXXXX--- XXXXXXXX _B
003A43 _H	003C43 _H				
003A44 _H	003C44 _H	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX _B
003A45 _H	003C45 _H				
003A46 _H	003C46 _H				XXXXX--- XXXXXXXX _B
003A47 _H	003C47 _H				
003A48 _H	003C48 _H	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX _B
003A49 _H	003C49 _H				
003A4A _H	003C4A _H				XXXXX--- XXXXXXXX _B
003A4B _H	003C4B _H				
003A4C _H	003C4C _H	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX _B
003A4D _H	003C4D _H				
003A4E _H	003C4E _H				XXXXX--- XXXXXXXX _B
003A4F _H	003C4F _H				
003A50 _H	003C50 _H	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX _B
003A51 _H	003C51 _H				
003A52 _H	003C52 _H				XXXXX--- XXXXXXXX _B
003A53 _H	003C53 _H				
003A54 _H	003C54 _H	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX _B
003A55 _H	003C55 _H				
003A56 _H	003C56 _H				XXXXX--- XXXXXXXX _B
003A57 _H	003C57 _H				
003A58 _H	003C58 _H	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX _B
003A59 _H	003C59 _H				
003A5A _H	003C5A _H				XXXXX--- XXXXXXXX _B
003A5B _H	003C5B _H				
003A5C _H	003C5C _H	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX _B
003A5D _H	003C5D _H				
003A5E _H	003C5E _H				XXXXX--- XXXXXXXX _B
003A5F _H	003C5F _H				

(Continued)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A88 _H to 003A8F _H	003C88 _H to 003C8F _H	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
003A90 _H to 003A97 _H	003C90 _H to 003C97 _H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
003A98 _H to 003A9F _H	003C98 _H to 003C9F _H	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
003AA0 _H to 003AA7 _H	003CA0 _H to 003CA7 _H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
003AA8 _H to 003AAF _H	003CA8 _H to 003CAF _H	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
003AB0 _H to 003AB7 _H	003CB0 _H to 003CB7 _H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
003AB8 _H to 003ABF _H	003CB8 _H to 003CBF _H	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
003AC0 _H to 003AC7 _H	003CC0 _H to 003CC7 _H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
003AC8 _H to 003ACF _H	003CC8 _H to 003CCF _H	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
003AD0 _H to 003AD7 _H	003CD0 _H to 003CD7 _H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
003AD8 _H to 003ADF _H	003CD8 _H to 003CDF _H	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
003AE0 _H to 003AE7 _H	003CE0 _H to 003CE7 _H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
003AE8 _H to 003AEF _H	003CE8 _H to 003CEF _H	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B
003AF0 _H to 003AF7 _H	003CF0 _H to 003CF7 _H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
003AF8 _H to 003AFF _H	003CF8 _H to 003CFF _H	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Units	Remarks
		Min	Max		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *1
	$AVRH, AVRL$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH/AVRL, AVRH \geq AVRL$ *1
Input voltage	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Output voltage	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Maximum clamp current	I_{CLAMP}	- 2.0	+ 2.0	mA	*6
Total maximum clamp current	$\Sigma I_{CLAMP} $	—	20	mA	*6
"L" level max output current	I_{OL}	—	15	mA	*3
"L" level avg. output current	I_{OLAV}	—	4	mA	*4
"L" level max overall output current	ΣI_{OL}	—	100	mA	
"L" level avg. overall output current	ΣI_{OLAV}	—	50	mA	*5
"H" level max output current	I_{OH}	—	-15	mA	*3
"H" level avg. output current	I_{OHAV}	—	-4	mA	*4
"H" level max overall output current	ΣI_{OH}	—	-100	mA	
"H" level avg. overall output current	ΣI_{OHAV}	—	-50	mA	*5
Power consumption	P_D	—	500	mW	Flash device
		—	400	mW	MASK ROM
Operating temperature	T_A	-40	+105	°C	
Storage temperature	T_{STG}	-55	+150	°C	

*1 : AV_{CC} , $AVRH$, $AVRL$ should not exceed V_{CC} . Also, $AVRH$, $AVRL$ should not exceed AV_{CC} , and $AVRL$ does not exceed $AVRH$.

*2 : V_I and V_O should not exceed $V_{CC} + 0.3\text{ V}$. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supercedes the V_I rating.

*3 : The maximum output current is a peak value for a corresponding pin.

*4 : Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5 : Total average current is an average current value observed for a 100 ms period for all corresponding pins.

*6 :

- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The + B signal should always be applied with a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the + B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a + B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- Care must be taken not to leave the + B input pin open.

(Continued)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

Parameter	Sym- bol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Power supply current*	I _{CC}	V _{CC}	Internal frequency : 16 MHz, At normal operating	—	40	55	mA	
			Internal frequency : 16 MHz, At Flash programming/erasing	—	50	70	mA	Flash device
	I _{CCS}		Internal frequency : 16 MHz, At sleep mode	—	12	20	mA	
	I _{CTS}		V _{CC} = 5.0 V ± 10%, Internal frequency : 2 MHz, At pseudo timer mode	—	300	600	μA	
				—	600	1100	μA	MB90F548GL (S) only
				—	200	400	μA	MB90543G(S)/547G(S)/548(S) only
	I _{CCL}		Internal frequency : 8 kHz, At sub operation, T _A = 25 °C	—	400	750	μA	MB90F548GL only
				—	50	100	μA	MASK ROM
				—	150	300	μA	Flash device
	I _{CCLS}		Internal frequency : 8 kHz, At sub sleep, T _A = 25 °C	—	15	40	μA	
I _{CCT}	Internal frequency : 8 kHz, At timer mode, T _A = 25 °C	—	7	25	μA			
I _{CCH1}	At stop, T _A = 25 °C	—	5	20	μA			
I _{CCH2}	At hardware standby mode, T _A = 25 °C	—	50	100	μA			
Input capacity	C _{IN}	Other than AV _{CC} , AV _{SS} , AVRH, AVRL, C, V _{CC} , V _{SS}	—	—	5	15	pF	

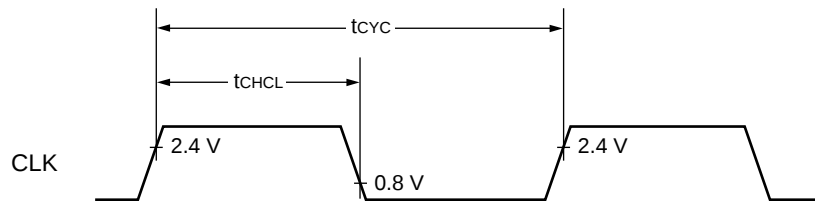
* : The power supply current testing conditions are when using the external clock.

11.4.2 Clock Output Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	$V_{CC} = 5\text{ V} \pm 10\%$	62.5	—	ns	
CLK $\uparrow \rightarrow$ CLK $\downarrow$	t_{CHCL}			20	—	ns	



11.4.3 Reset and Hardware Standby Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value		Units	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	$4\ t_{CP}$	—	ns	Under normal operation
			Oscillation time of oscillator + $4\ t_{CP}$	—	ms	In stop mode
			100	—	μs	In pseudo timer mode (MB90543G (S) /547G (S) /548G (S))
			$4\ t_{CP}$	—	ns	In pseudo timer mode (Other than MB90543G (S) /547G (S) /548G (S))
			$2\ t_{LCP}$	—	μs	In sub-clock mode, sub-sleep mode, timer mode
Hardware standby input time	t_{HSTL}	HST	$4\ t_{CP}$	—	ns	Under normal operation

Note : " t_{cp} " represents one cycle time of the machine clock.

Oscillation time of oscillator is time that amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ns.

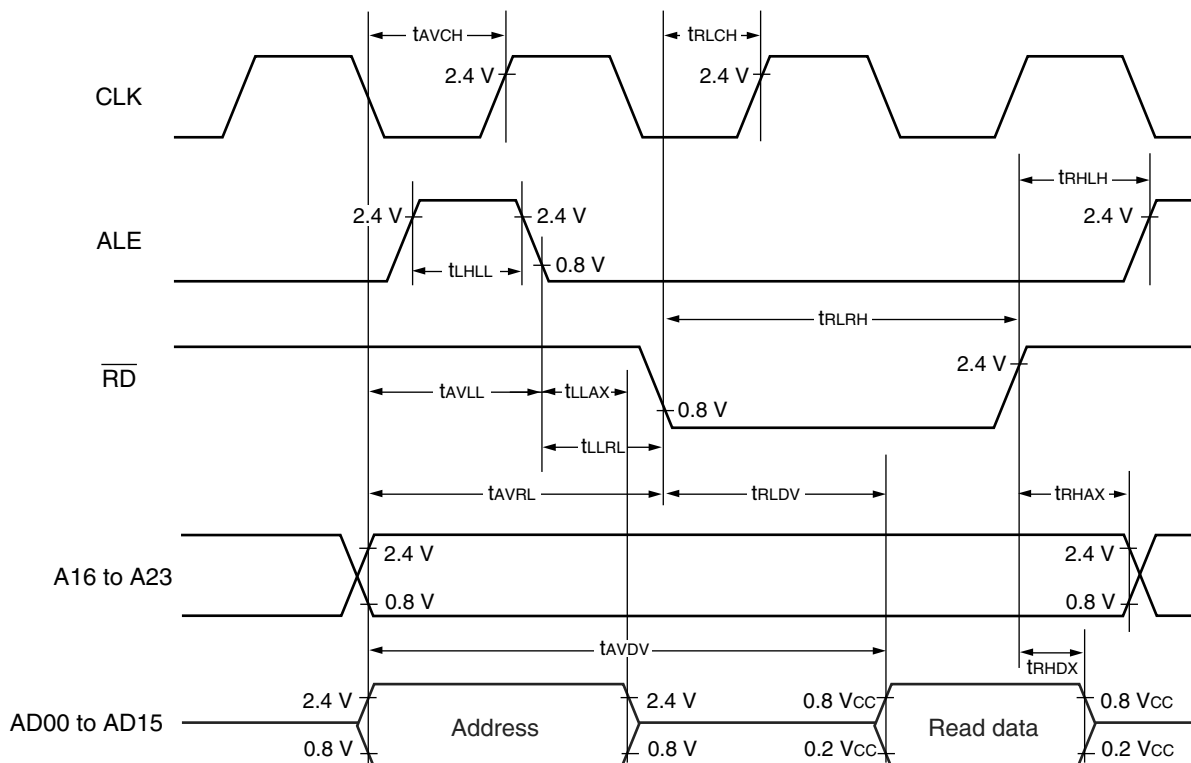
Any reset can not fully initialize the Flash Memory if it is performing the automatic algorithm.

11.4.5 Bus Timing (Read)

 (MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ °C to }+105\text{ °C}$)

 (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ °C to }+105\text{ °C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 20$	—	ns	
Valid address → ALE↓ time	t_{AVLL}	ALE, A16 to A23, AD00 to AD15		$t_{CP}/2 - 20$	—	ns	
ALE↓ → Address valid time	t_{LLAX}	ALE, AD00 to AD15		$t_{CP}/2 - 15$	—	ns	
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	A16 to A23, AD00 to AD15, RD		$t_{CP} - 15$	—	ns	
Valid address → Valid data input	t_{AVDV}	A16 to A23, AD00 to AD15		—	$5 t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	RD		$3 t_{CP}/2 - 20$	—	ns	
$\overline{RD}$ ↓ → Valid data input	t_{RLDV}	$\overline{RD}$, AD00 to AD15		—	$3 t_{CP}/2 - 60$	ns	
$\overline{RD}$ ↑ → Data hold time	t_{RHDX}	$\overline{RD}$, AD00 to AD15		0	—	ns	
$\overline{RD}$ ↑ → ALE↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	—	ns	
RD↑ → Address valid time	t_{RHAX}	RD, A16 to A23		$t_{CP}/2 - 10$	—	ns	
Valid address → CLK↑ time	t_{AVCH}	A16 to A23, AD00 to AD15, CLK		$t_{CP}/2 - 20$	—	ns	
$\overline{RD}$ ↓ → CLK↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 20$	—	ns	
ALE↓ → $\overline{RD}$ ↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	—	ns	

■ Bus Timing (Read)


11.4.8 Hold Timing

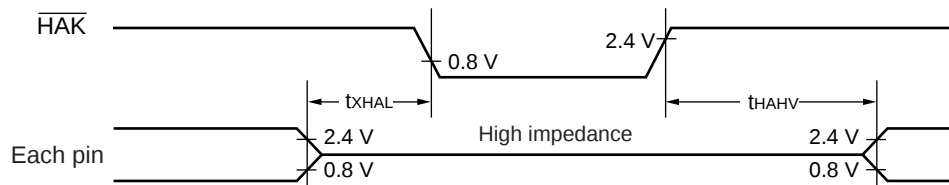
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Pin floating → $\overline{\text{HAK}}\downarrow$ time	t_{XHAL}	$\overline{\text{HAK}}$	—	30	t_{CP}	ns	
$\overline{\text{HAK}}\uparrow$ time → Pin valid time	t_{HAHV}	$\overline{\text{HAK}}$	—	t_{CP}	$2 t_{CP}$	ns	

Note : There is more than 1 cycle from the time HRQ is read to the time the $\overline{\text{HAK}}$ is changed.

■ Hold Timing



11.4.9 UART0/1, Serial I/O Timing

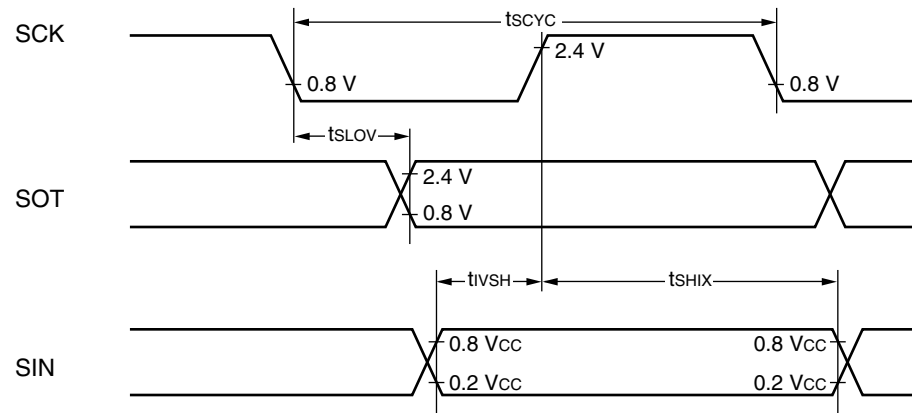
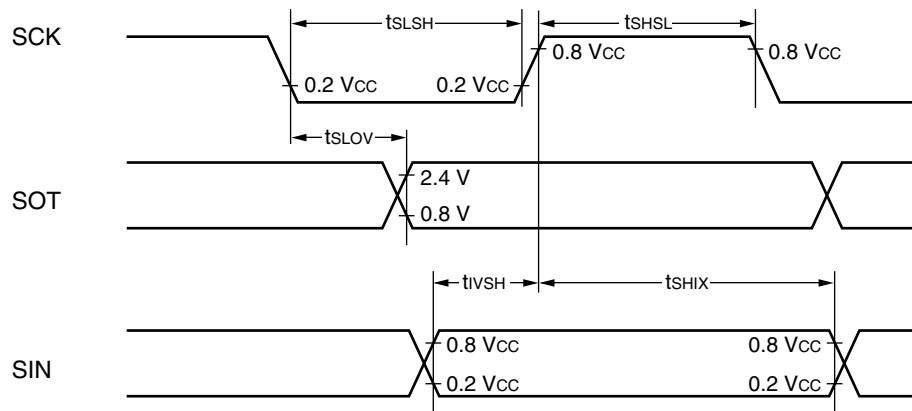
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

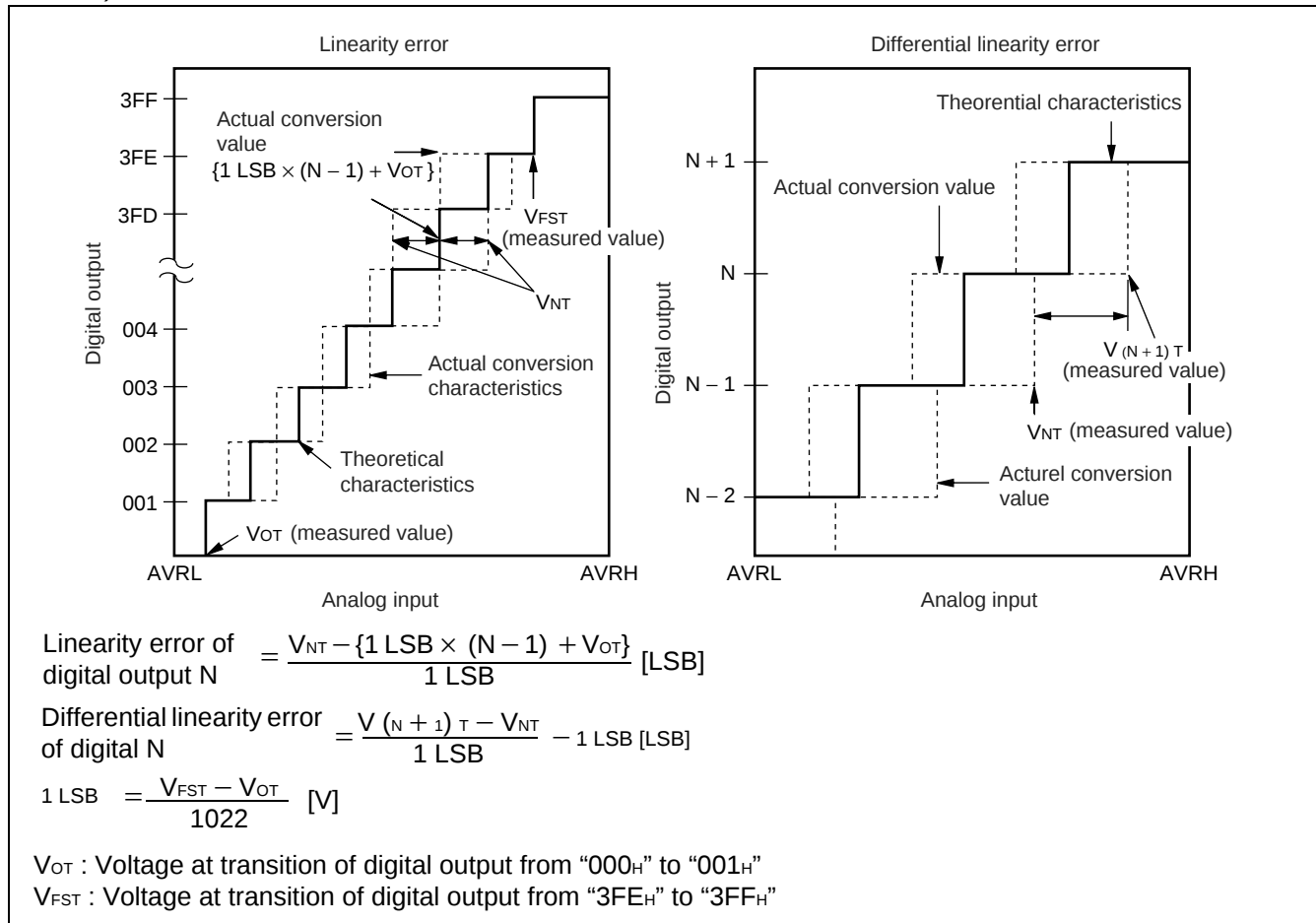
Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$8 t_{CP}$	—	ns	
SCK $\downarrow$ → SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		— 80	80	ns	
Valid SIN → SCK $\uparrow$	t_{VSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK $\uparrow$ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK2	External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$4 t_{CP}$	—	ns	
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK2		$4 t_{CP}$	—	ns	
SCK $\downarrow$ → SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN → SCK $\uparrow$	t_{VSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK $\uparrow$ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

Notes :

- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- For t_{CP} (Machine clock cycle time) , refer to “ (1) Clock Timing”.

Internal Shift Clock Mode

External Shift Clock Mode


(Continued)

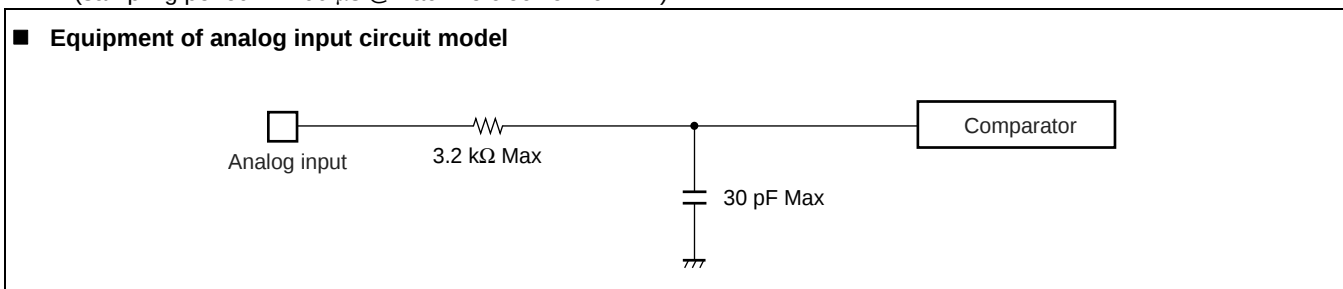


11.5.3 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions, :

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

Note : When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz) .

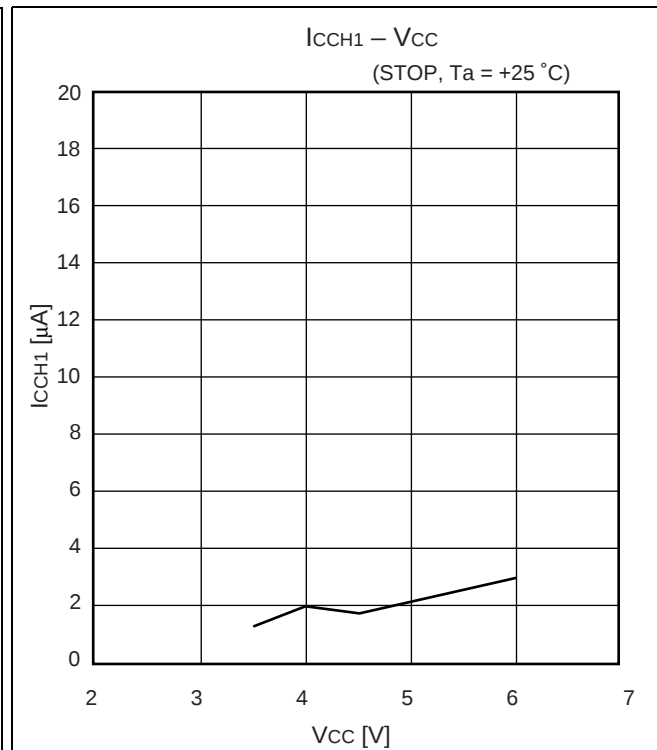
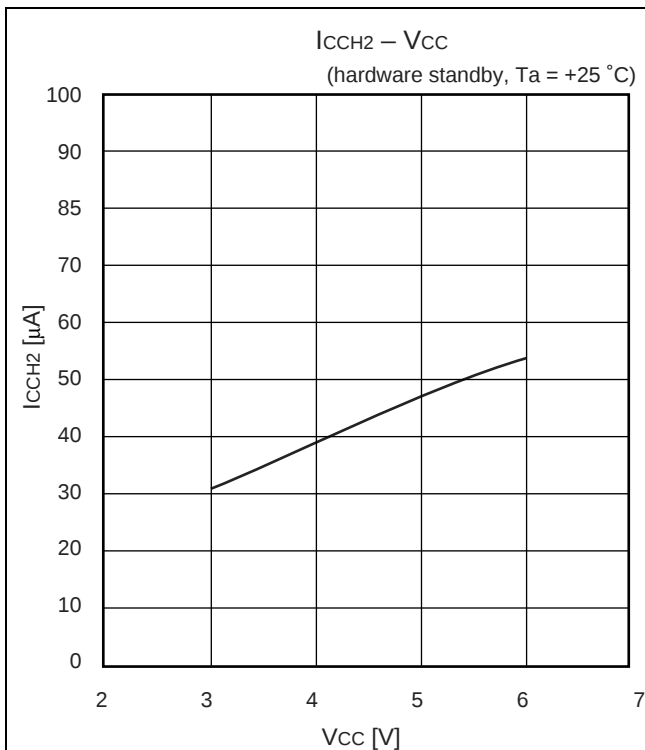
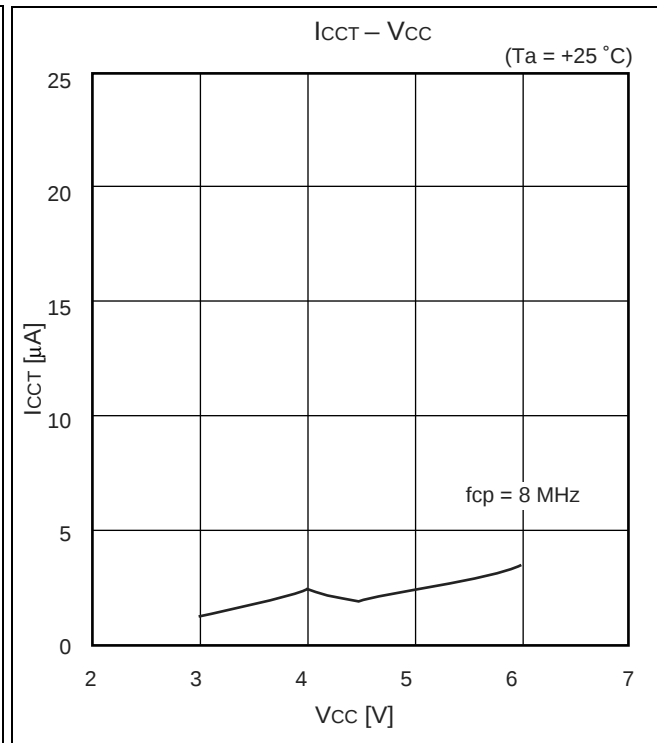
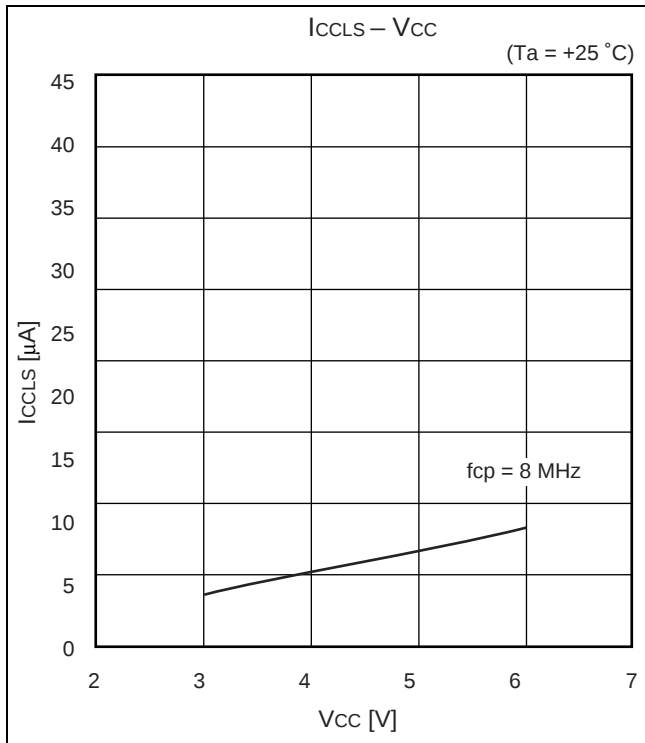


11.5.4 Error

The smaller the | AVRH – AVRL |, the greater the error would become relatively.

11.6 Flash Memory Program/Erase Characteristics

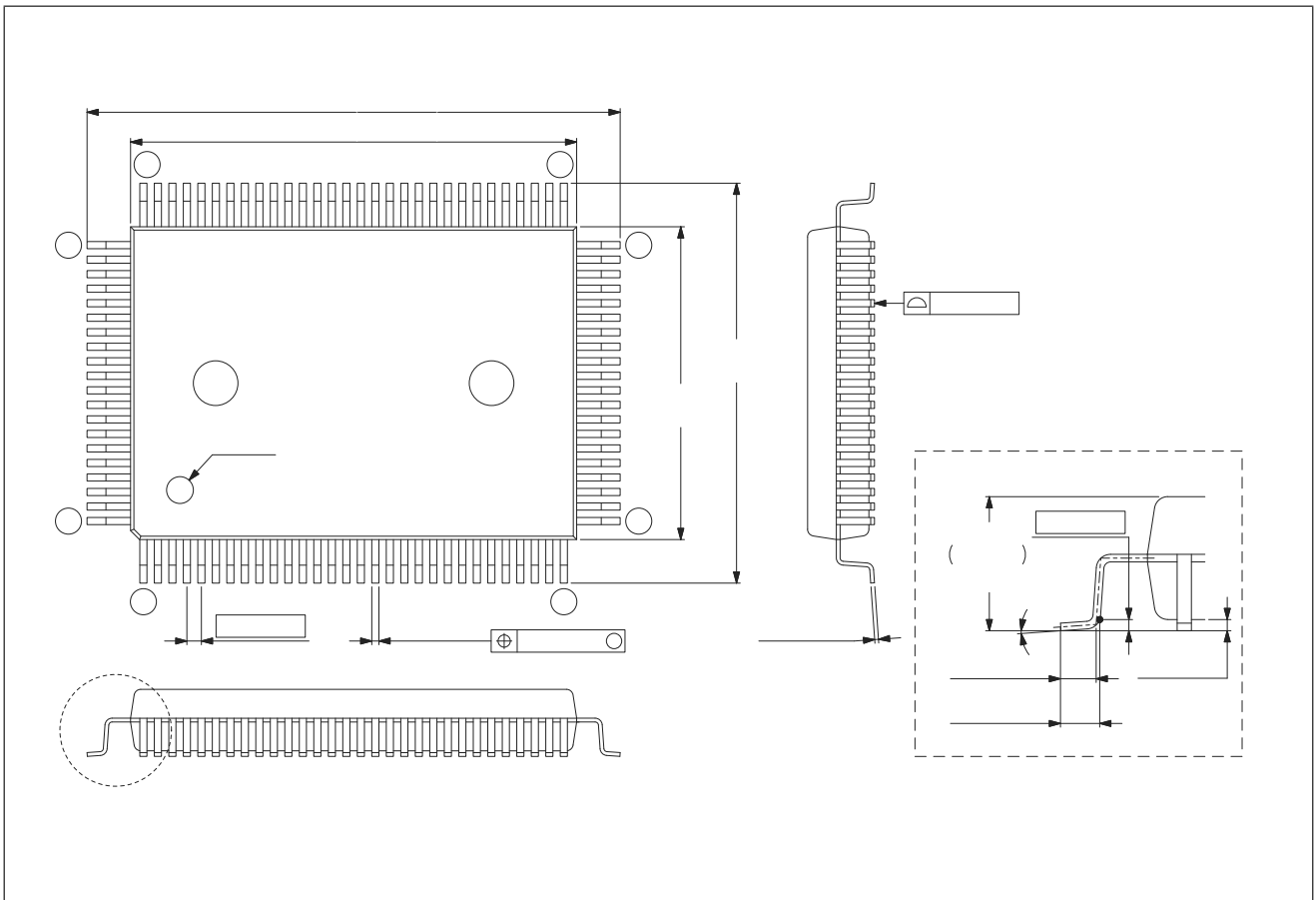
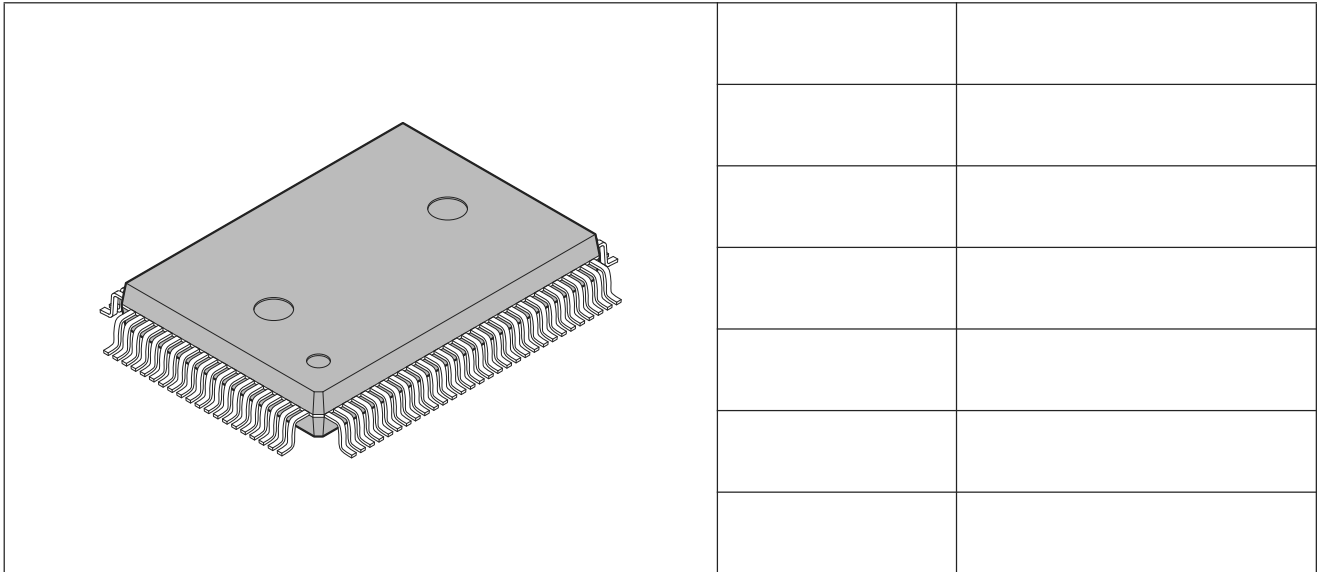
Parameter	Condition	Value			Units	Remarks	
		Min	Typ	Max			
Sector erase time	T _A = + 25 °C V _{CC} = 5.0 V	—	1	15	s	Excludes 00H programming prior erasure	
Chip erase time		—	5	—	s	MB90F543G (S) /F548G (S) /F548GL (S)	Excludes 00H programming prior erasure
			7	—	s	MB90F549G (S) /F546G (S)	
Word (16 bit width) programming time		—	—	16	3,600	μs	Excludes system-level overhead
Erase/Program cycle	—	10,000	—	—	cycle		



13. Ordering Information

Part number	Package	Remarks
MB90F543GPF MB90F543GSPF MB90F546GPF MB90F546GSPF MB90F548GPF MB90F548GSPF MB90F548GLPF MB90F548GLSPF MB90F549GPF MB90F549GSPF MB90543GPF MB90543GSPF MB90547GPF MB90547GSPF MB90548GPF MB90548GSPF MB90549GPF MB90549GSPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90F543GPMC MB90F543GSPMC MB90F546GPMC MB90F546GSPMC MB90F548GPMC MB90F548GSPMC MB90F548GLPMC MB90F548GLSPMC MB90F549GPMC MB90F549GSPMC MB90543GPMC MB90543GSPMC MB90547GPMC MB90547GSPMC MB90548GPMC MB90548GSPMC MB90549GPMC MB90549GSPMC	100-pin Plastic LQFP (FPT-100P-M20)	

14. Package Dimensions



(Continued)

(Continued)

