Infineon Technologies - MB90F546GSPMC-G-FL Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

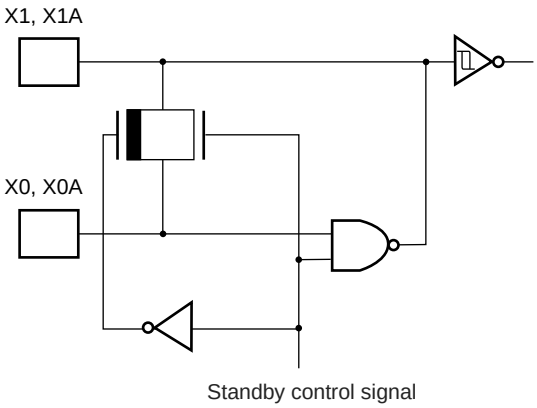
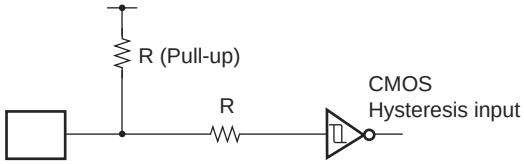
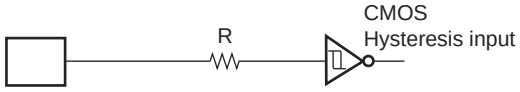
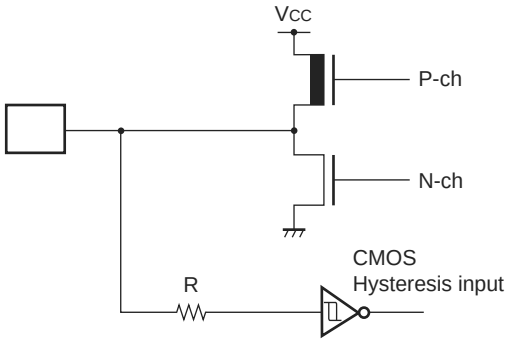
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f546gspmc-g-fl

Starting by an external trigger input.
Conversion time : 26.3 μs

- FULL-CAN interfaces
  MB90540G series : 2 channels
  MB90545G series : 1 channel
  Conforming to Version 2.0 Part A and Part B
  Flexible message buffering (mailbox and FIFO buffering can be mixed)
- External bus interface : Maximum address space 16 Mbytes
- Package: QFP-100, LQFP-100

4. I/O Circuit Type

Circuit type	Diagram	Remarks
A		■ High-speed oscillation feedback resistor : 1 MΩ approx. ■ Low-speed oscillation feedback resistor: 10 MΩ approx.
B		■ CMOS Hysteresis input ■ Pull-up resistor : 50 kΩ approx.
C		■ CMOS Hysteresis input
D		■ CMOS level output ■ CMOS Hysteresis input

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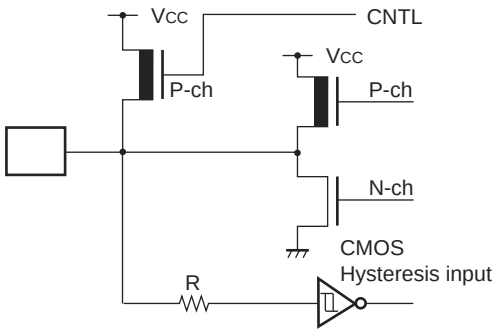
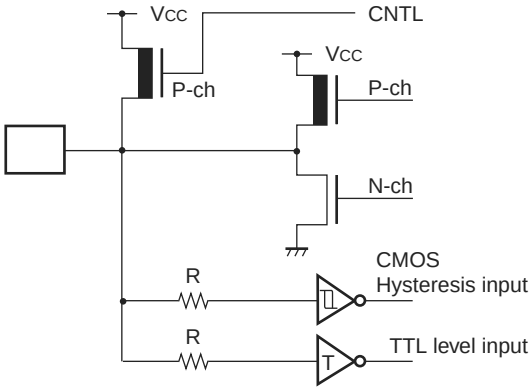
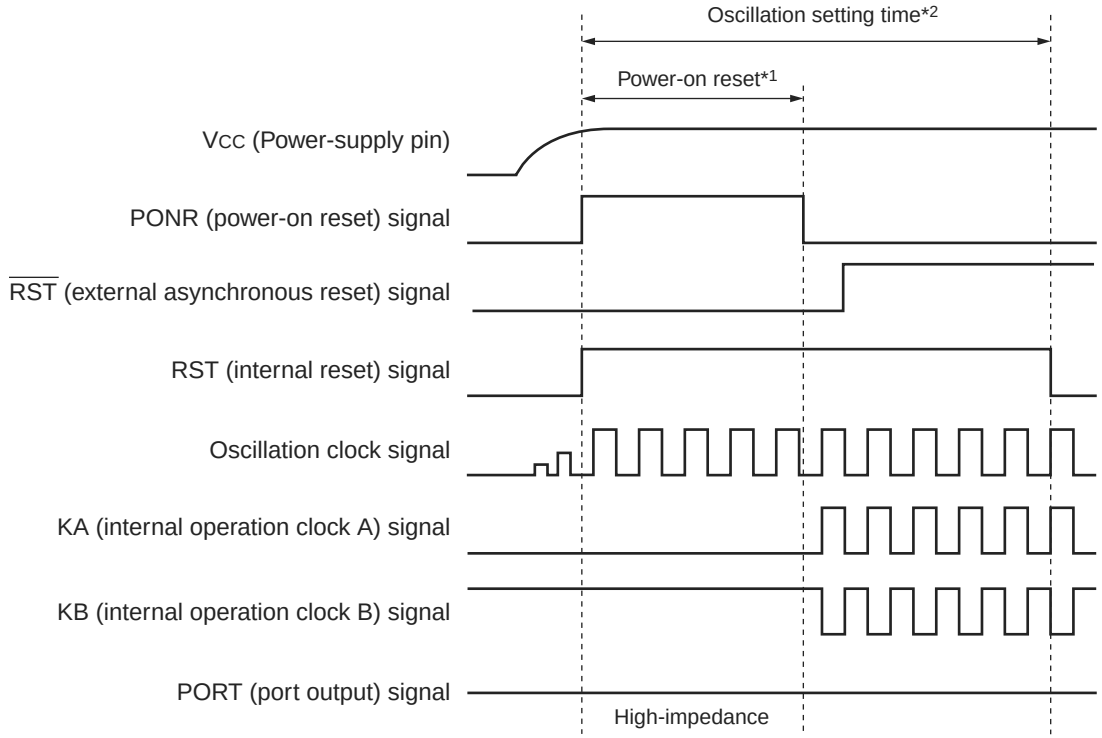
Circuit type	Diagram	Remarks
H		■ CMOS level output ■ CMOS Hysteresis input ■ Programmable pull-up resistor : 50 kΩ approx.
I		■ CMOS level output ■ CMOS Hysteresis input ■ TTL level input (Flash devices in Flash writer mode only) ■ Programmable pullup resistor : 50 kΩ approx.

■ $\overline{\text{RST}}$ pin is “L”



*1 : Power-on reset time : “Period of clock frequency” × 2^{17} (Clock frequency of 16 MHz : 8.19 ms)

*2 : Oscillation setting time : “Period of clock frequency” × 2^{18} (Clock frequency of 16 MHz : 16.38 ms)

(13) Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(14) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions

In the Signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”) , the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00_H”.

If the values of the corresponding bank registers (DTB, ADB, USB, SSB) are set to other than “00_H”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

(15) Using REALOS

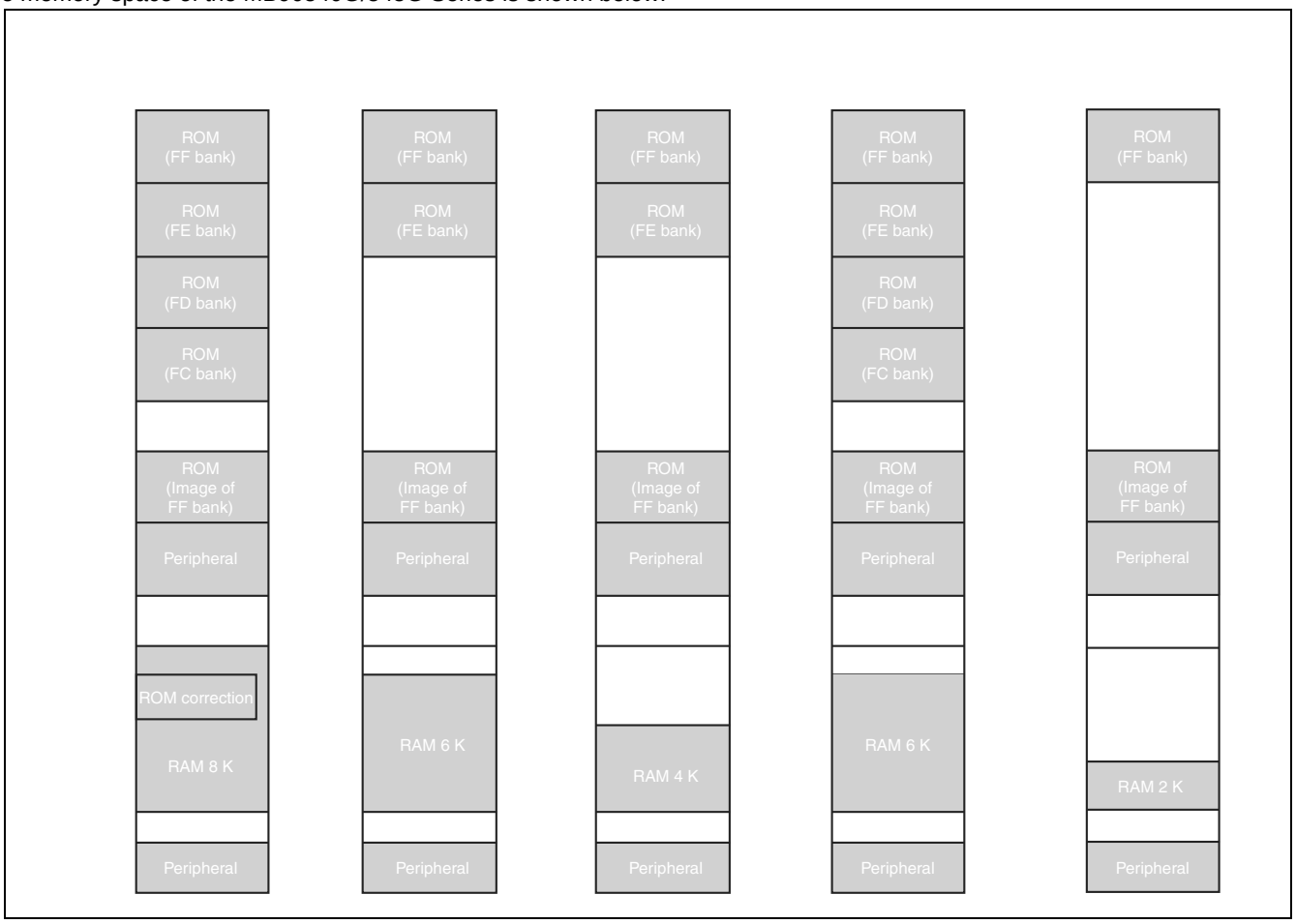
The use of EI²OS is not possible with the REALOS real time operating system.

(16) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

7. Memory Map

The memory space of the MB90540G/545G Series is shown below.



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits address are the same, the table in ROM can be referenced without using the “far” specification in the pointer declaration.
For example, an attempt to access $00C000_H$ accesses the value at $FFC000_H$ in ROM.The ROM area in bank FF exceeds 48 Kbytes, and its entire image cannot be shown in bank 00.The image between $FF4000_H$ and $FFFFFF_H$ is visible in bank 00, while the image between $FF0000_H$ and $FF3FFF_H$ is visible only in bank FF.

Address	Register	Abbreviation	Access	Resource name	Initial value
$A2_H$ to $A4_H$	Prohibited				
$A5_H$	Automatic ready function select register	ARSR	W	External Memory Access	0 0 1 1 _ _ 0 0_B
$A6_H$	External address output control register	HACR	W		0 0 0 0 0 0 0 0_B
$A7_H$	Bus control signal selection register	ECSR	W		0 0 0 0 0 0 0 $_B$
$A8_H$	Watchdog Timer control register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1_B
$A9_H$	Time Base Timer Control register	TBTC	R/W	Time Base Timer	1 - - 0 0 1 0 0_B
AA_H	Watch timer control register	WTC	R/W	Watch Timer	1 X 0 0 0 0 0 0_B
AB_H to AD_H	Prohibited				
AE_H	Flash memory control status register (Flash only, otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0_B
AF_H	Prohibited				
$B0_H$	Interrupt control register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1_B
$B1_H$	Interrupt control register 01	ICR01	R/W		0 0 0 0 0 1 1 1_B
$B2_H$	Interrupt control register 02	ICR02	R/W		0 0 0 0 0 1 1 1_B
$B3_H$	Interrupt control register 03	ICR03	R/W		0 0 0 0 0 1 1 1_B
$B4_H$	Interrupt control register 04	ICR04	R/W		0 0 0 0 0 1 1 1_B
$B5_H$	Interrupt control register 05	ICR05	R/W		0 0 0 0 0 1 1 1_B
$B6_H$	Interrupt control register 06	ICR06	R/W		0 0 0 0 0 1 1 1_B
$B7_H$	Interrupt control register 07	ICR07	R/W		0 0 0 0 0 1 1 1_B
$B8_H$	Interrupt control register 08	ICR08	R/W		0 0 0 0 0 1 1 1_B
$B9_H$	Interrupt control register 09	ICR09	R/W		0 0 0 0 0 1 1 1_B
BA_H	Interrupt control register 10	ICR10	R/W		0 0 0 0 0 1 1 1_B
BB_H	Interrupt control register 11	ICR11	R/W		0 0 0 0 0 1 1 1_B
BC_H	Interrupt control register 12	ICR12	R/W		0 0 0 0 0 1 1 1_B
BD_H	Interrupt control register 13	ICR13	R/W		0 0 0 0 0 1 1 1_B
BE_H	Interrupt control register 14	ICR14	R/W		0 0 0 0 0 1 1 1_B
BF_H	Interrupt control register 15	ICR15	R/W		0 0 0 0 0 1 1 1_B
$C0_H$ to FF_H	External				

Address	Register	Abbreviation	Access	Resource name	Initial value
$1FF0_H$	Program address detection register 0	PADR0	R/W	Address Match Detection Function	$XXXXXXXX_B$
$1FF1_H$	Program address detection register 0	PADR0	R/W		$XXXXXXXX_B$
$1FF2_H$	Program address detection register 0	PADR0	R/W		$XXXXXXXX_B$
$1FF3_H$	Program address detection register 1	PADR1	R/W		$XXXXXXXX_B$
$1FF4_H$	Program address detection register 1	PADR1	R/W		$XXXXXXXX_B$
$1FF5_H$	Program address detection register 1	PADR1	R/W		$XXXXXXXX_B$

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003B00H	003D00H	Control status register	CSR	R/W, R	00---000 0----0-1B
003B01H	003D01H				
003B02H	003D02H	Last event indicator register	LEIR	R/W	-------- 000-0000B
003B03H	003D03H				
003B04H	003D04H	Receive/transmit error counter register	RTEC	R	00000000 00000000B
003B05H	003D05H				
003B06H	003D06H	Bit timing register	BTR	R/W	-1111111 11111111B
003B07H	003D07H				
003B08H	003D08H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXXB
003B09H	003D09H				
003B0AH	003D0AH	Transmit RTR register	TRTRR	R/W	00000000 00000000B
003B0BH	003D0BH				
003B0CH	003D0CH	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXXB
003B0DH	003D0DH				
003B0EH	003D0EH	Transmit request enable register	TIER	R/W	00000000 00000000B
003B0FH	003D0FH				
003B10H	003D10H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXXB
003B11H	003D11H				
003B12H	003D12H				XXXXXXXX XXXXXXXXB
003B13H	003D13H				
003B14H	003D14H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXXB
003B15H	003D15H				
003B16H	003D16H				XXXXX--- XXXXXXXXB
003B17H	003D17H				
003B18H	003D18H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXXB
003B19H	003D19H				
003B1AH	003D1AH				XXXXX--- XXXXXXXXB
003B1BH	003D1BH				

List of Message Buffers (ID Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A00H to 003A1FH	003C00H to 003C1FH	General-purpose RAM	—	R/W	XXXXXXXXB to XXXXXXXXB
003A20H	003C20H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXXB
003A21H	003C21H				
003A22H	003C22H				XXXXX--- XXXXXXXXB
003A23H	003C23H				

10. Interrupt Map

Interrupt cause	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC$_H$	—	—
INT9 instruction	N/A	#09	FFFFD8$_H$	—	—
Exception	N/A	#10	FFFFD4$_H$	—	—
CAN 0 RX	N/A	#11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN 0 TX/NS	N/A	#12	FFFFCC$_H$		
CAN 1 RX	N/A	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 1 TX/NS	N/A	#14	FFFFC4$_H$		
External Interrupt INT0/INT1	*1	#15	FFFFC0$_H$	ICR02	0000B2$_H$
Time Base Timer	N/A	#16	FFFFBC$_H$		
16-bit Reload Timer 0	*1	#17	FFFFB8$_H$	ICR03	0000B3$_H$
8/10-bit A/D Converter	*1	#18	FFFFB4$_H$		
16-bit Free-run Timer	N/A	#19	FFFFB0$_H$	ICR04	0000B4$_H$
External Interrupt INT2/INT3	*1	#20	FFFFAC$_H$		
Serial I/O	*1	#21	FFFFA8$_H$	ICR05	0000B5$_H$
8/16-bit PPG 0/1	N/A	#22	FFFFA4$_H$		
Input Capture 0	*1	#23	FFFFA0$_H$	ICR06	0000B6$_H$
External Interrupt INT4/INT5	*1	#24	FFFF9C$_H$		
Input Capture 1	*1	#25	FFFF98$_H$	ICR07	0000B7$_H$
8/16-bit PPG 2/3	N/A	#26	FFFF94$_H$		
External Interrupt INT6/INT7	*1	#27	FFFF90$_H$	ICR08	0000B8$_H$
Watch Timer	N/A	#28	FFFF8C$_H$		
8/16-bit PPG 4/5	N/A	#29	FFFF88$_H$	ICR09	0000B9$_H$
Input Capture 2/3	*1	#30	FFFF84$_H$		
8/16-bit PPG 6/7	N/A	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 0	*1	#32	FFFF7C$_H$		
Output Compare 1	*1	#33	FFFF78$_H$	ICR11	0000BB$_H$
Input Capture 4/5	*1	#34	FFFF74$_H$		
Output Compare 2/3 - Input Capture 6/7	*1	#35	FFFF70$_H$	ICR12	0000BC$_H$
16-bit Reload Timer 1	*1	#36	FFFF6C$_H$		
UART 0 RX	*2	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 0 TX	*1	#38	FFFF64$_H$		
UART 1 RX	*2	#39	FFFF60$_H$	ICR14	0000BE$_H$
UART 1 TX	*1	#40	FFFF5C$_H$		
Flash Memory	N/A	#41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed interrupt	N/A	#42	FFFF54$_H$		

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*1 : The interrupt request flag is cleared by the EI²OS interrupt clear signal.

*2 : The interrupt request flag is cleared by the EI²OS interrupt clear signal. A stop request is available.

Notes :

- N/A : The interrupt request flag is not cleared by the EI²OS interrupt clear signal.
- For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.
- At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by a hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.
- If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0.0$ V)

Parameter	Symbol	Value		Units	Remarks
		Min	Max		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *1
	AVRH, AVRL	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq$ AVRH/AVRL, AVRH $\geq$ AVRL *1
Input voltage	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Output voltage	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Maximum clamp current	I_{CLAMP}	−2.0	+2.0	mA	*6
Total maximum clamp current	$\Sigma\lvert I_{CLAMP} \rvert$	−	20	mA	*6
“L” level max output current	I_{OL}	−	15	mA	*3
“L” level avg. output current	I_{OLAV}	−	4	mA	*4
“L” level max overall output current	ΣI_{OL}	−	100	mA	
“L” level avg. overall output current	ΣI_{OLAV}	−	50	mA	*5
“H” level max output current	I_{OH}	−	−15	mA	*3
“H” level avg. output current	I_{OHAV}	−	−4	mA	*4
“H” level max overall output current	ΣI_{OH}	−	−100	mA	
“H” level avg. overall output current	ΣI_{OHAV}	−	−50	mA	*5
Power consumption	P_D	−	500	mW	Flash device
		−	400	mW	MASK ROM
Operating temperature	T_A	−40	+105	°C	
Storage temperature	T_{STG}	−55	+150	°C	

*1 : AV_{CC}, AVRH, AVRL should not exceed V_{CC}. Also, AVRH, AVRL should not exceed AV_{CC}, and AVRL does not exceed AVRH.

*2 : V_I and V_O should not exceed $V_{CC} + 0.3$ V. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supercedes the V_I rating.

*3 : The maximum output current is a peak value for a corresponding pin.

*4 : Average output current is an average current value observed for a 100 ms period for a corresponding pin.

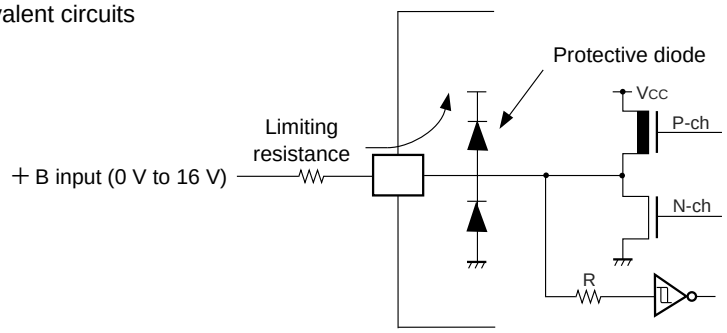
*5 : Total average current is an average current value observed for a 100 ms period for all corresponding pins.

*6 :

- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The + B signal should always be applied with a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the + B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a + B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- Care must be taken not to leave the + B input pin open.

- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept + B signal input.
- Sample recommended circuits :

■ Input/Output Equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

11.3 DC Characteristics

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Input H voltage	V_{IHS}	CMOS hysteresis input pin	−	0.8 V_{CC}	−	V_{CC} + 0.3	V	
	V_{IH}	TTL input pin	−	2.0	−	−	V	
	V_{IHM}	MD input pin	−	V_{CC} − 0.3	−	V_{CC} + 0.3	V	
Input L voltage	V_{ILS}	CMOS hysteresis input pin	−	V_{CC} − 0.3	−	0.2 V_{CC}	V	
	V_{IL}	TTL input pin	−	−	−	0.8	V	
	V_{ILM}	MD input pin	−	V_{SS} − 0.3	−	V_{SS} + 0.3	V	
Output H voltage	V_{OH}	All output pins	V_{CC} = 4.5 V, I_{OH} = −4.0 mA	V_{CC} − 0.5	−	−	V	
Output L voltage	V_{OL}	All output pins	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	−	−	0.4	V	
Input leak current	I_{IL}	−	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	−5	−	5	µA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, RST	−	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	−	25	50	100	kΩ	Except Flash devices

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(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Power supply current*	I_{CC}	V_{CC}	Internal frequency : 16 MHz, At normal operating	—	40	55	mA	
			Internal frequency : 16 MHz, At Flash programming/erasing	—	50	70	mA	Flash device
	I_{CCS}		Internal frequency : 16 MHz, At sleep mode	—	12	20	mA	
	I_{CTS}		V_{CC} = 5.0 V ± 10%, Internal frequency : 2 MHz, At pseudo timer mode	—	300	600	µA	
				—	600	1100	µA	MB90F548GL (S) only
				—	200	400	µA	MB90543G(S)/547G(S)/548(S) only
	I_{CCL}		Internal frequency : 8 kHz, At sub operation, T_A = 25 °C	—	400	750	µA	MB90F548GL only
				—	50	100	µA	MASK ROM
				—	150	300	µA	Flash device
	I_{CCLS}		Internal frequency : 8 kHz, At sub sleep, T_A = 25 °C	—	15	40	µA	
	I_{CCT}		Internal frequency : 8 kHz, At timer mode, T_A = 25 °C	—	7	25	µA	
	I_{CCH1}		At stop, T_A = 25 °C	—	5	20	µA	
	I_{CCH2}		At hardware standby mode, T_A = 25 °C	—	50	100	µA	
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVRH, AVRL, C, V_{CC}, V_{SS}	—	—	5	15	pF	

* : The power supply current testing conditions are when using the external clock.

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(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	No multiplier When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			62.5	—	125	ns	PLL multiplied by 1 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			125	—	250	ns	PLL multiplied by 2 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			187.5	—	333	ns	PLL multiplied by 3 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			250	—	333	ns	PLL multiplied by 4 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			200	—	333	ns	When using an oscillator circuit V_{CC} < 4.5 V(MB90F548GL(S)/543G(S)/547G(S)/548G(S))
			62.5	—	333	ns	No multiplier When using an external clock
			62.5	—	125	ns	PLL multiplied by 1 When using an external clock
			125	—	250	ns	PLL multiplied by 2 When using an external clock
			187.5	—	333	ns	PLL multiplied by 3 When using an external clock
			250	—	333	ns	PLL multiplied by 4 When using an external clock
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WLH}, P_{WLL}	X0A	—	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using an external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	When using main clock
	f_{LCP}	—	—	8.192	—	kHz	When using sub-clock
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	When using main clock
	t_{LCP}	—	—	122.1	—	µs	When using sub-clock

11.4.4 Power On Reset

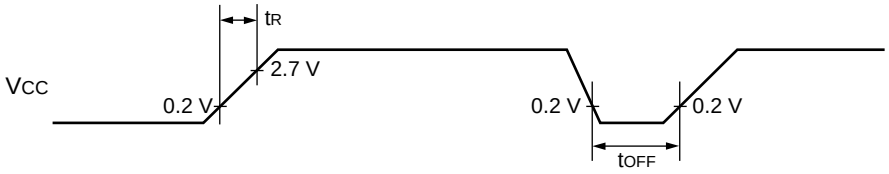
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

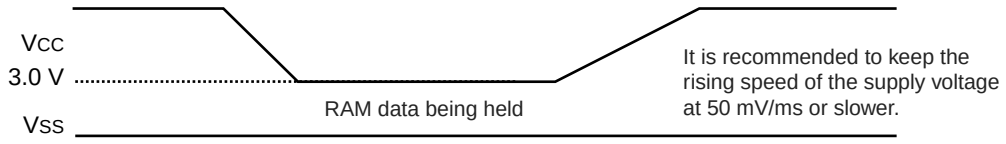
Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	*
Power off time	t_{OFF}	V_{CC}		50	—	ms	Waiting time until power-on

* : V_{CC} must be kept lower than 0.2 V before power-on.

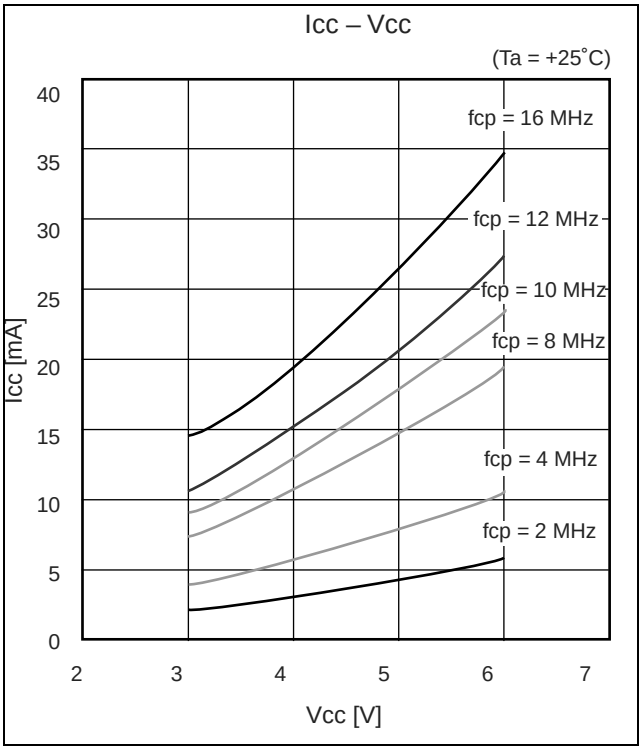
Notes : ■ The above values are used for creating a power-on reset.
■ Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.

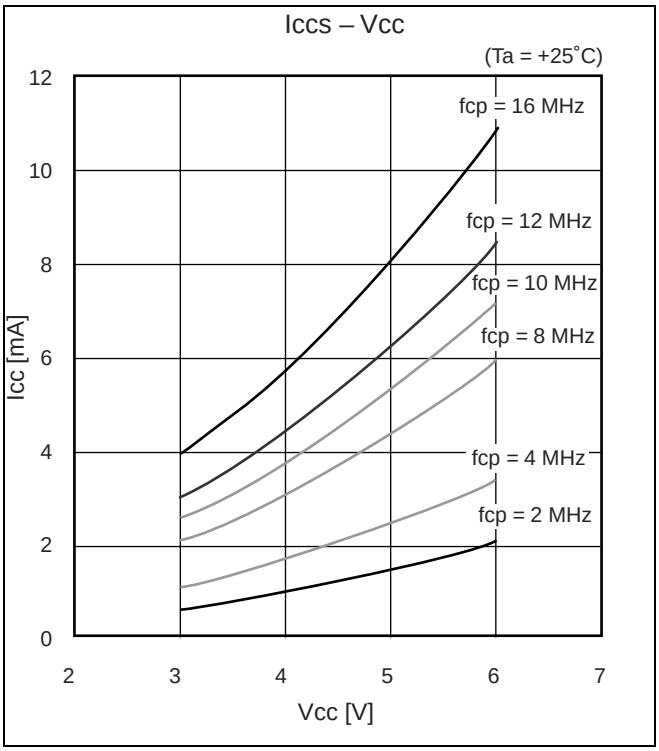


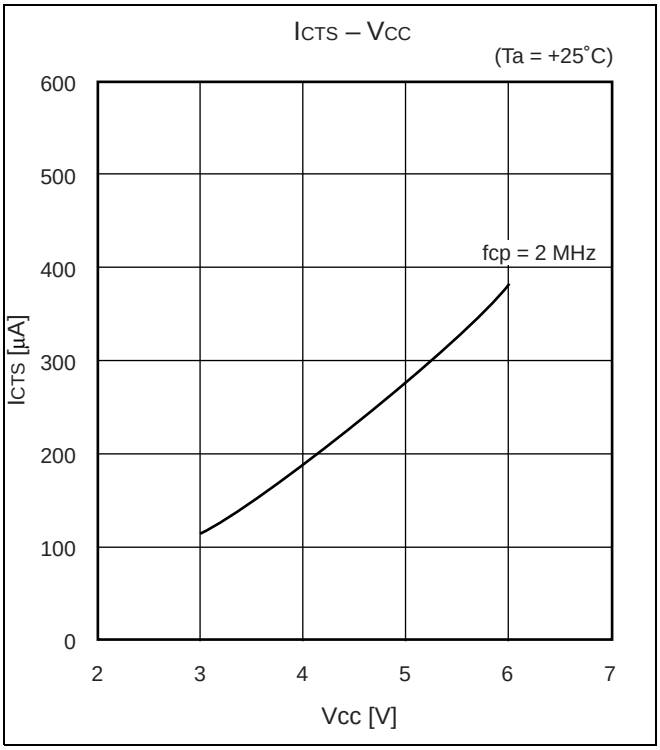
Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.

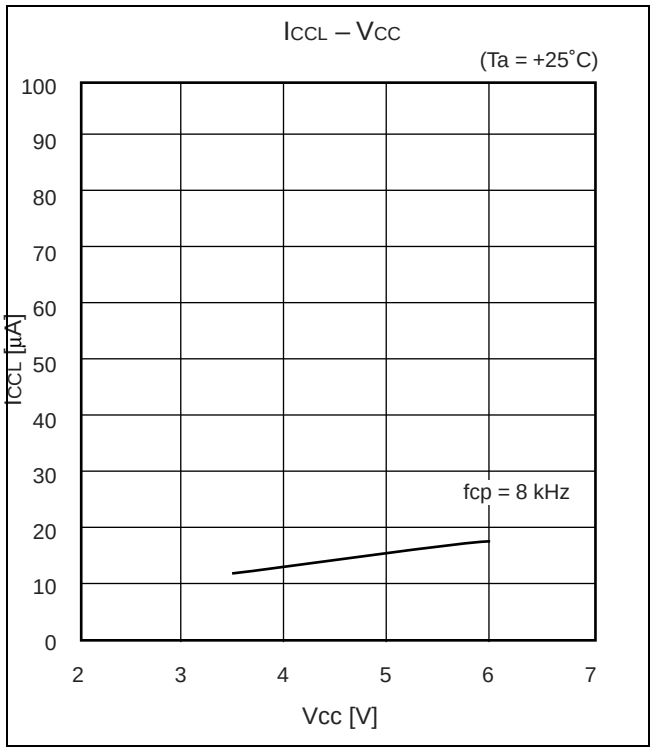


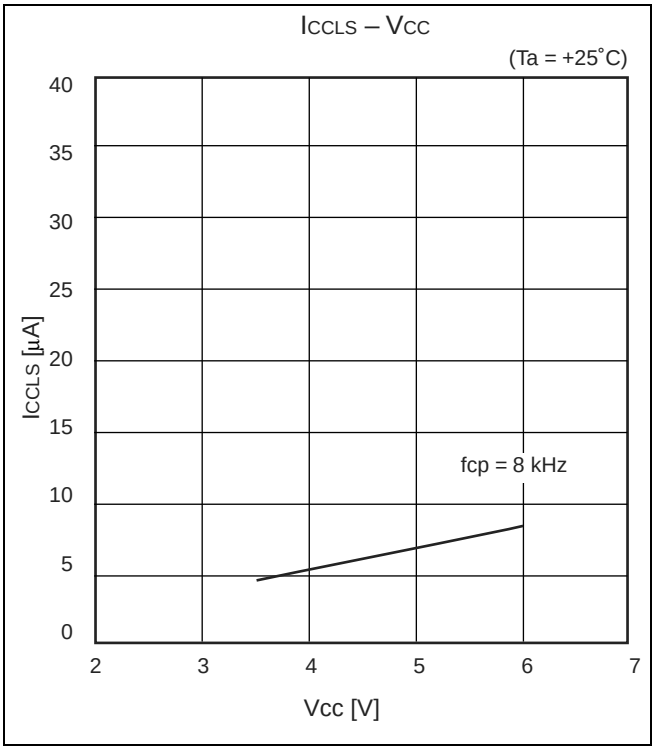
■ Power supply current (MB90549G)

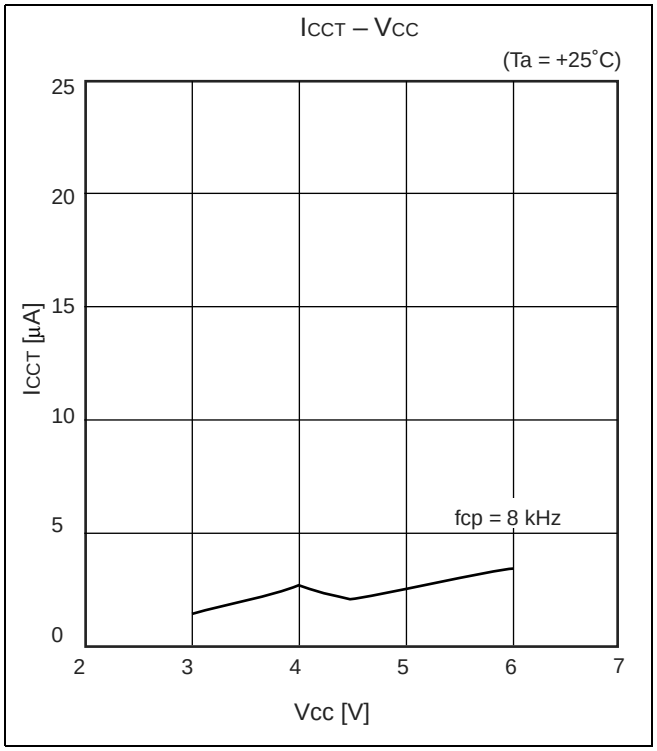


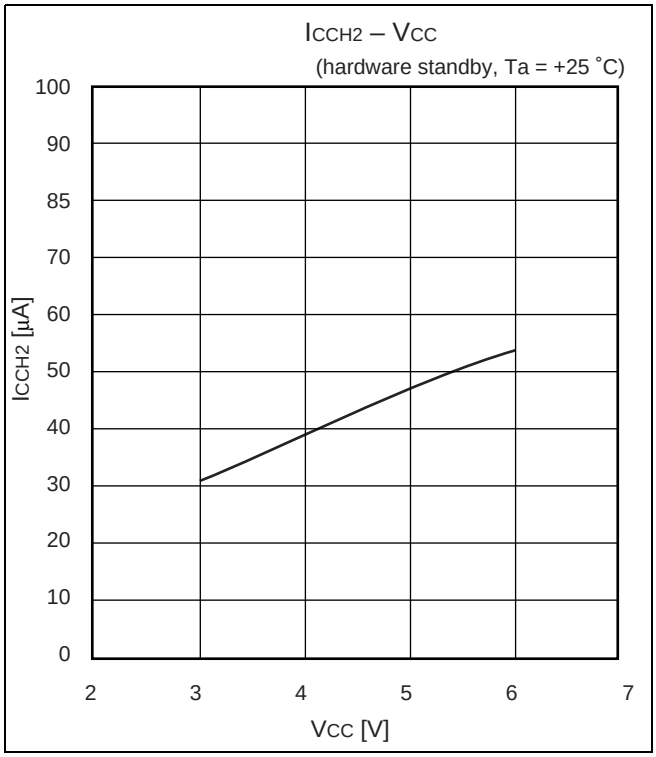


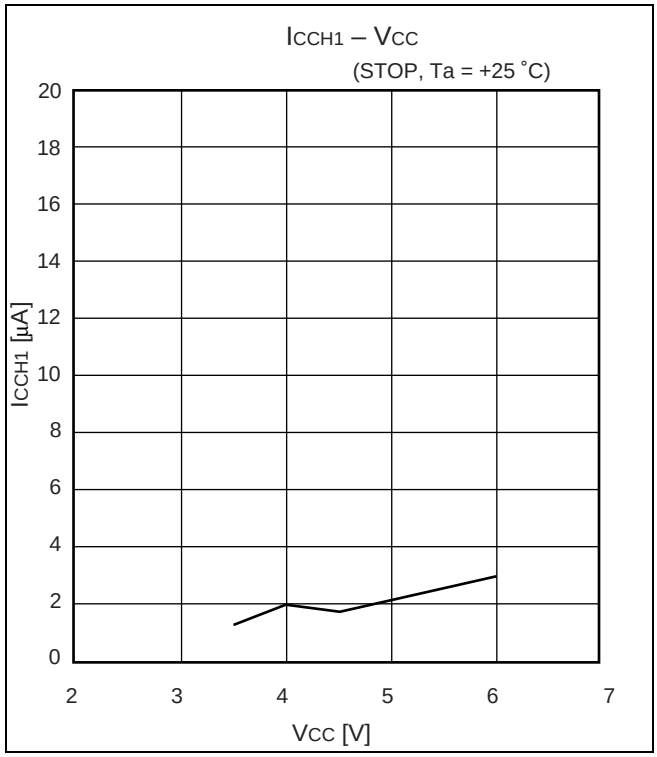


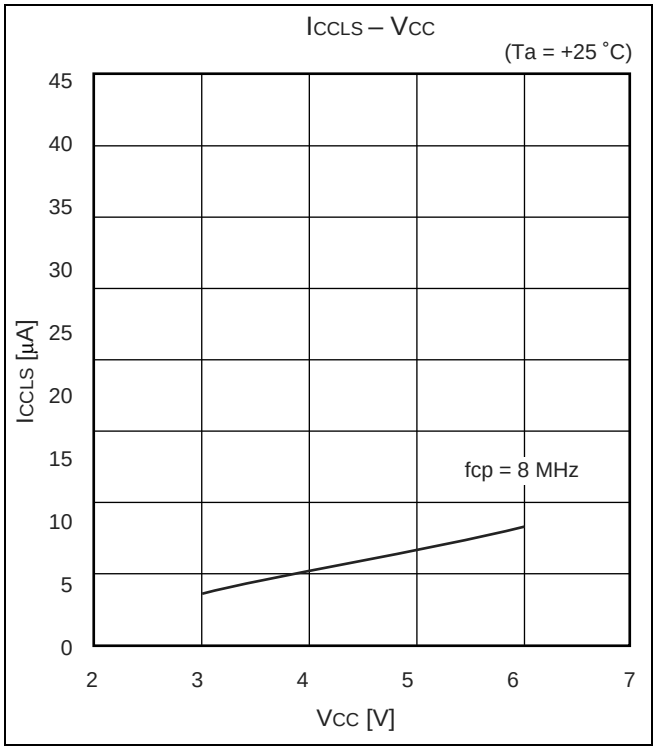


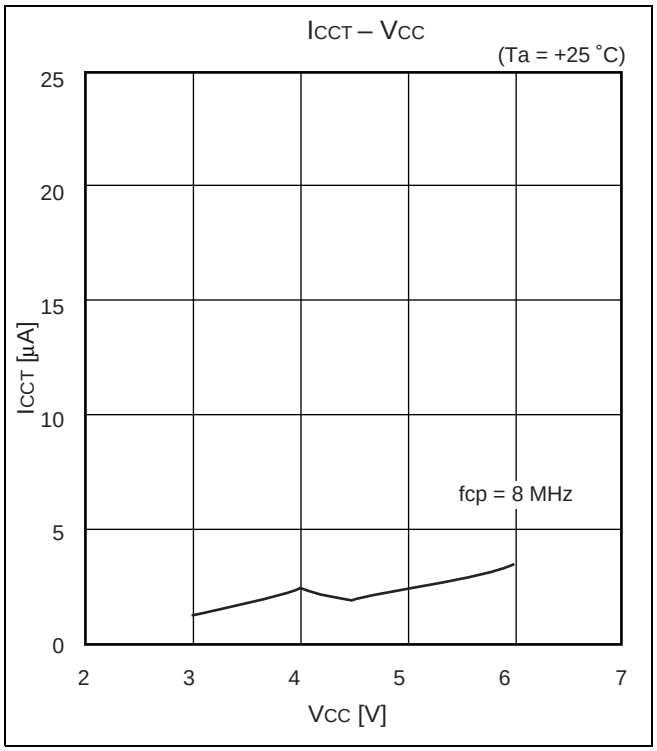

ICCLS – VCC
(Ta = +25˚C)
ICCLS [µA]
40
35
30
25
20
15
10
5
0
fcp = 8 kHz
2
3
4
5
6
7
Vcc [V]

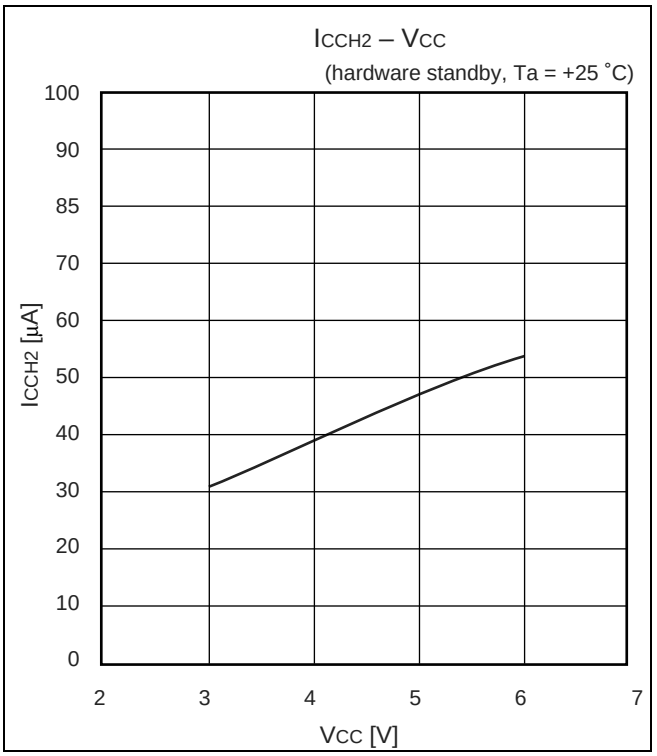

ICCT – VCC
(Ta = +25˚C)
ICCT [µA]
25
20
15
10
5
0
fcp = 8 kHz
2
3
4
5
6
7
Vcc [V]

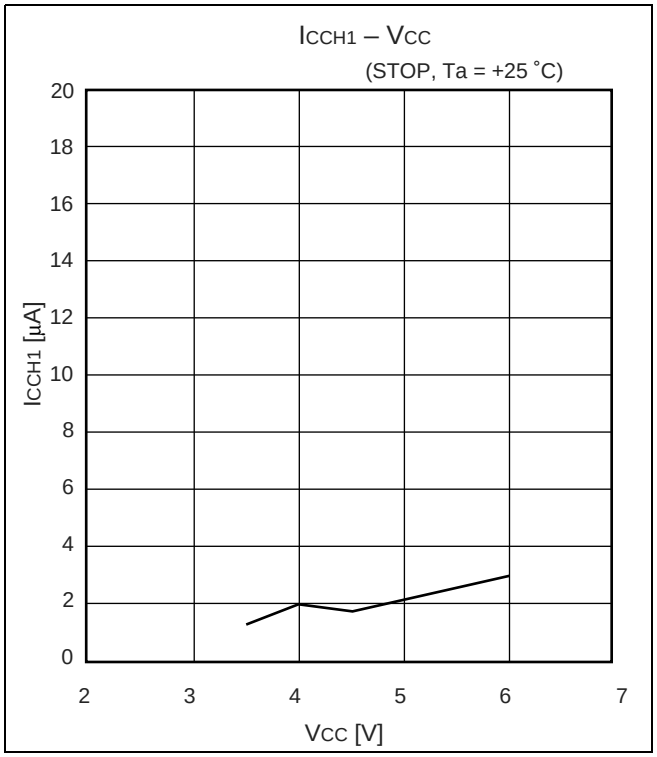

ICCH2 – VCC
(hardware standby, Ta = +25 ˚C)
ICCH2 [µA]
100
90
85
70
60
50
40
30
20
10
0
2
3
4
5
6
7
VCC [V]


ICCH1 – VCC
(STOP, Ta = +25 ˚C)
ICCH1 [µA]
20
18
16
14
12
10
8
6
4
2
0
2
3
4
5
6
7
VCC [V]

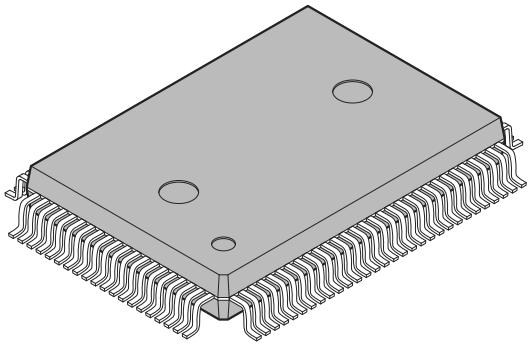

ICCLS – VCC
(Ta = +25 ˚C)
ICCLS [µA]
45
40
35
30
25
20
15
10
5
0
fcp = 8 MHz
2
3
4
5
6
7
VCC [V]

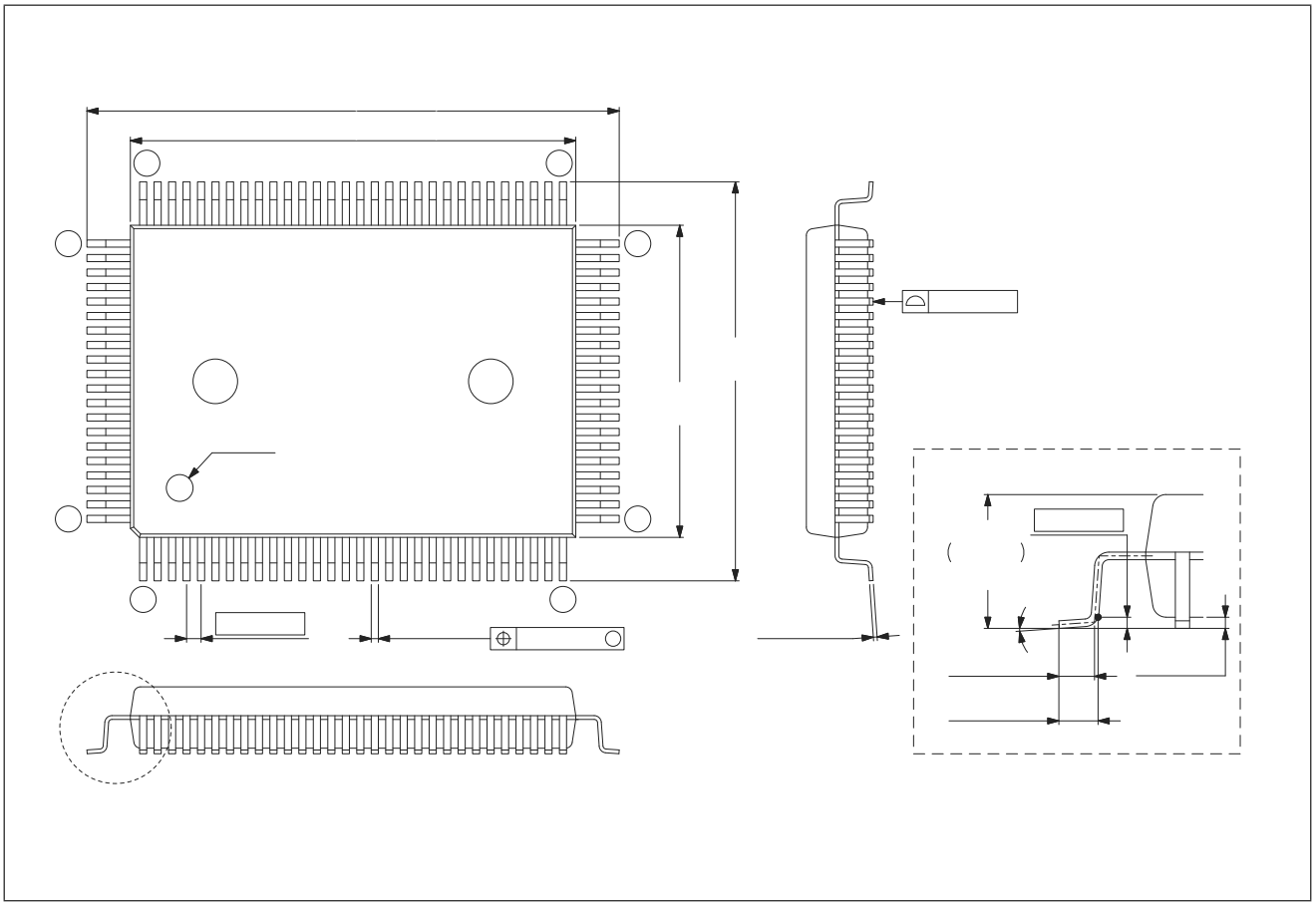

ICCT – VCC
(Ta = +25 ˚C)
ICCT [µA]
25
20
15
10
5
0
fcp = 8 MHz
2
3
4
5
6
7
VCC [V]


ICCH2 – VCC
(hardware standby, Ta = +25 ˚C)
ICCH2 [µA]
100
90
85
70
60
50
40
30
20
10
0
2
3
4
5
6
7
VCC [V]


ICCH1 – VCC
(STOP, Ta = +25 ˚C)
ICCH1 [µA]
20
18
16
14
12
10
8
6
4
2
0
2
3
4
5
6
7
VCC [V]

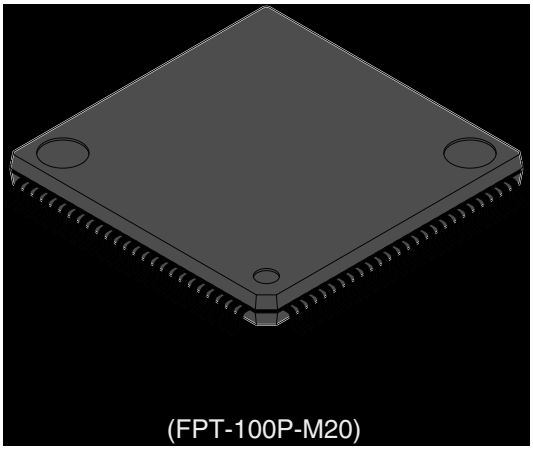
14. Package Dimensions



(Continued)

(Continued)



(FPT-100P-M20)