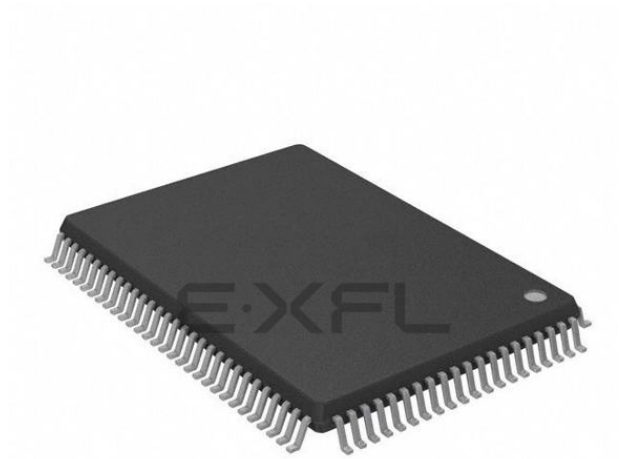


**Welcome to E-XFL.COM**

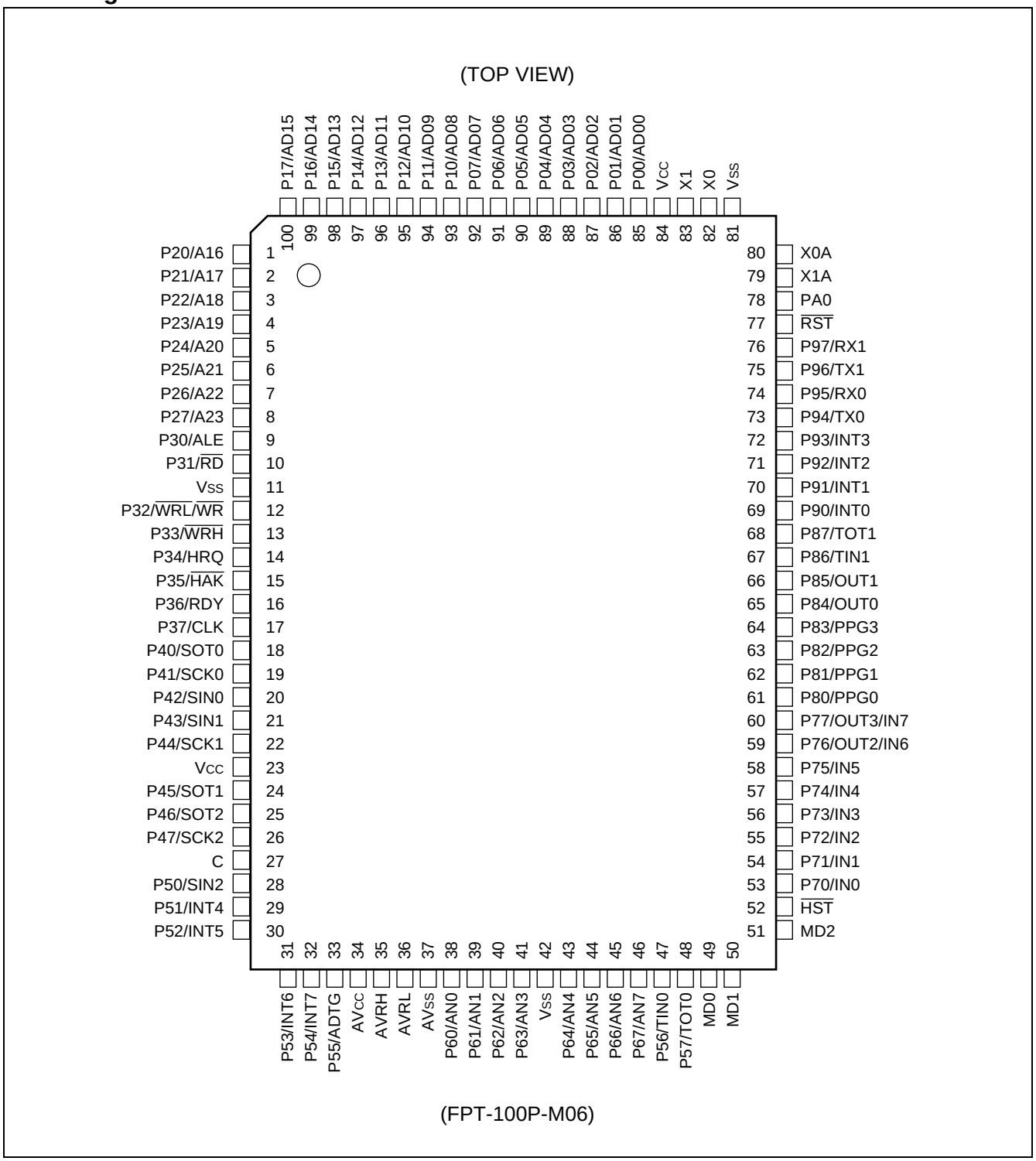
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | F²MC-16LX |
| Core Size | 16-Bit |
| Speed | 16MHz |
| Connectivity | CANbus, EBI/EMI, SCI, Serial I/O, UART/USART |
| Peripherals | POR, WDT |
| Number of I/O | 81 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 8x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BQFP |
| Supplier Device Package | 100-QFP (14x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb90f548gpf-g |

## 2. Pin Assignment



| Pin No. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP*2 | QFP*1 | | | |
| 20 | 22 | P44 | G | General I/O port. This function is enabled when UART1 disables the clock output. |
| | | SCK1 | | Serial clock pulse I/O pin for UART1. This function is enabled when UART1 enables the serial clock output. |
| 22 | 24 | P45 | G | General I/O port. This function is enabled when UART1 disables the serial data output. |
| | | SOT1 | | Serial data output pin for UART1. This function is enabled when UART1 enables the serial data output. |
| 23 | 25 | P46 | G | General I/O port. This function is enabled when the Extended I/O serial interface disables the serial data output. |
| | | SOT2 | | Serial data output pin for the Extended I/O serial interface. This function is enabled when the Extended I/O serial interface enables the serial data output. |
| 24 | 26 | P47 | G | General I/O port. This function is enabled when the Extended I/O serial interface disables the clock output. |
| | | SCK2 | | Serial clock pulse I/O pin for the Extended I/O serial interface . This function is enabled when the Extended I/O serial interface enables the Serial clock output. |
| 26 | 28 | P50 | D | General I/O port. This function is always enabled. |
| | | SIN2 | | Serial data input pin for the Extended I/O serial interface . Set the corresponding Port Direction Register to input if this function is used. |
| 27 to 30 | 29 to 32 | P51 to P54 | D | General I/O port. This function is always enabled. |
| | | INT4 to INT7 | | External interrupt request input pins for INT4 to INT7. Set the corresponding Port Direction Register to input if this function is used. |
| 31 | 33 | P55 | D | General I/O port. This function is always enabled. |
| | | ADTG | | Trigger input pin for the A/D converter. Set the corresponding Port Direction Register to input if this function is used. |
| 36 to 39 | 38 to 41 | P60 to P63 | E | General I/O port. This function is enabled when the analog input enable register specifies a port. |
| | | AN0 to AN3 | | Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D. |
| 41 to 44 | 43 to 46 | P64 to P67 | E | General I/O port. The function is enabled when the analog input enable register specifies a port. |
| | | AN4 to AN7 | | Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D. |
| 45 | 47 | P56 | D | General I/O port. This function is always enabled. |
| | | TIN0 | | Event input pin for the 16-bit reload timers 0. Set the corresponding Port Direction Register to input if this function is used. |

*(Continued)*

*(Continued)*

| Pin No. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP*2 | QFP*1 | | | |
| 72 | 74 | P95 | D | General I/O port. This function is always enabled. |
| | | RX0 | | RX input pin for CAN0 Interface. When the CAN function is used, output from the other functions must be stopped. |
| 73 | 75 | P96 | D | General I/O port. This function is enabled when CAN1 disables the output. |
| | | TX1 | | TX output pin for CAN1. This function is enabled when CAN1 enables the output (only MB90540G series) . |
| 74 | 76 | P97 | D | General I/O port. This function is always enabled. |
| | | RX1 | | RX input pin for CAN1 Interface. When the CAN function is used, output from the other functions must be stopped (only MB90540G series) . |
| 76 | 78 | PA0 | D | General I/O port. This function is always enabled. |
| 32 | 34 | $AV_{CC}$ | Power supply | Power supply pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to $AV_{CC}$ is applied to $V_{CC}$. |
| 35 | 37 | $AV_{SS}$ | Power supply | Power supply pin for the A/D Converter. |
| 33 | 35 | AVRH | Power supply | External reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to $AV_{CC}$. |
| 34 | 36 | AVRL | Power supply | External reference voltage input pin for the A/D Converter. |
| 47, 48 | 49, 50 | MD0, MD1 | C | Input pins for specifying the operating mode. The pins must be directly connected to $V_{CC}$ or $V_{SS}$. |
| 49 | 51 | MD2 | F | Input pin for specifying the operating mode. The pin must be directly connected to $V_{CC}$ or $V_{SS}$. |
| 25 | 27 | C | — | Power supply stabilization capacitor pin. It should be connected externally to an 0.1 µF ceramic capacitor. |
| 21, 82 | 23, 84 | $V_{CC}$ | Power supply | Input pin for power supply (5.0 V) . |
| 9, 40, 79 | 11, 42, 81 | $V_{SS}$ | Power supply | Input pin for power supply (0.0 V) . |

*1 : FPT-100P-M06

*2 : FPT-100P-M20

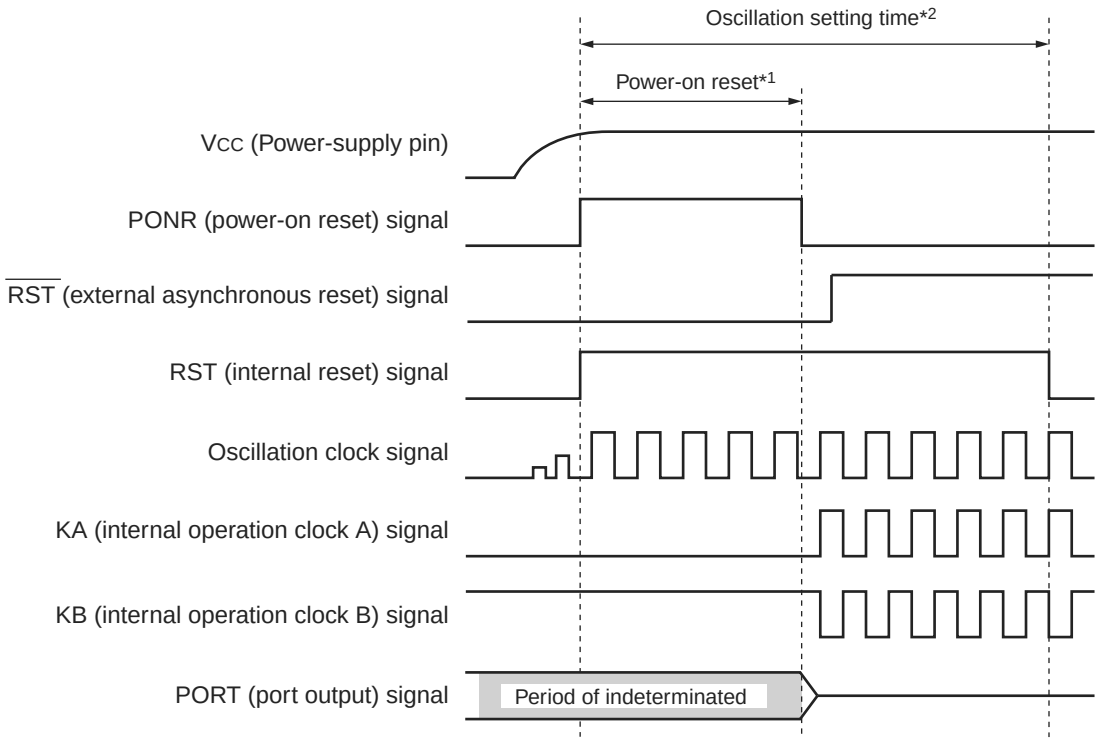
**(12) Indeterminate outputs from ports 0 and 1 (MB90V540G only)**

During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

- If $\overline{RST}$ pin is “H”, the outputs become indeterminate.
- If $\overline{RST}$ pin is “L”, the outputs become high-impedance.

Pay attention to the port output timing shown as follow.

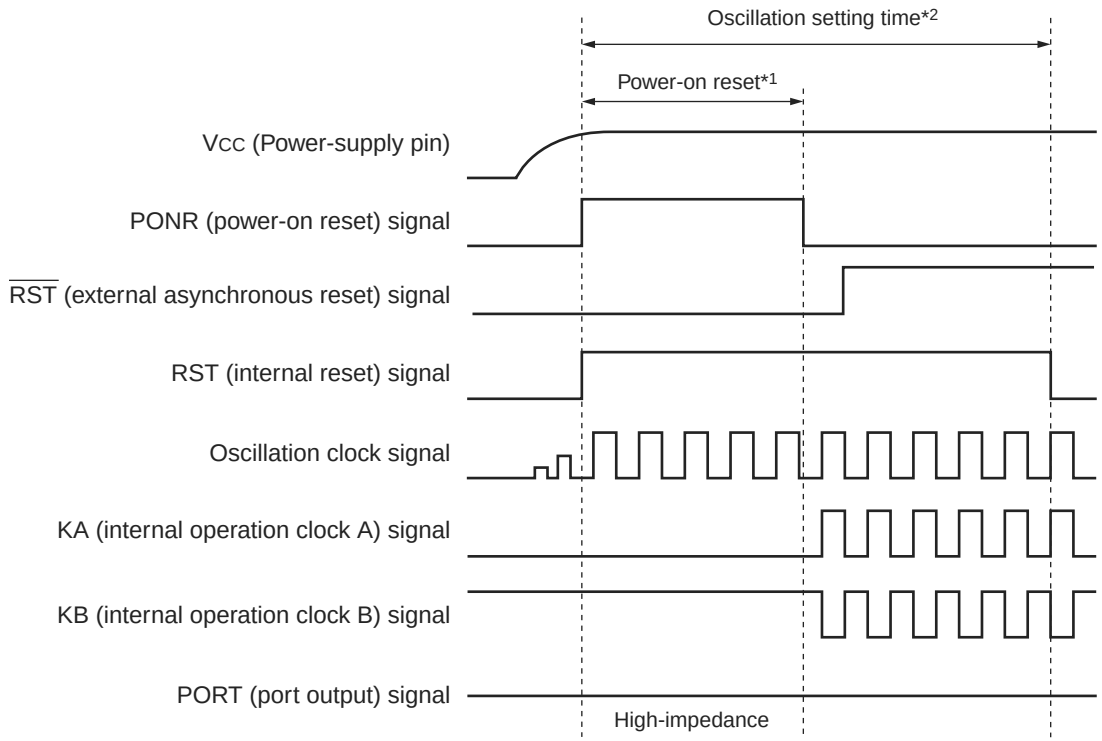
- $\overline{RST}$ pin is “H”




*1 : Power-on reset time : “Period of clock frequency” × $2^{17}$ (Clock frequency of 16 MHz : 8.19 ms)

*2 : Oscillation setting time : “Period of clock frequency” × $2^{18}$ (Clock frequency of 16 MHz : 16.38 ms)

■ $\overline{\text{RST}}$ pin is “L”




*1 : Power-on reset time : “Period of clock frequency” × $2^{17}$ (Clock frequency of 16 MHz : 8.19 ms)

*2 : Oscillation setting time : “Period of clock frequency” × $2^{18}$ (Clock frequency of 16 MHz : 16.38 ms)

**(13) Initialization**

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

**(14) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions**

In the Signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”) , the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “$00_H$”.

If the values of the corresponding bank registers (DTB, ADB, USB, SSB) are set to other than “$00_H$”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

**(15) Using REALOS**

The use of EI²OS is not possible with the REALOS real time operating system.

**(16) Caution on Operations during PLL Clock Mode**

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

## 8. I/O Map

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| $00_H$ | Port 0 data register | PDR0 | R/W | Port 0 | XXXXXXXX$_B$ |
| $01_H$ | Port 1 data register | PDR1 | R/W | Port 1 | XXXXXXXX$_B$ |
| $02_H$ | Port 2 data register | PDR2 | R/W | Port 2 | XXXXXXXX$_B$ |
| $03_H$ | Port 3 data register | PDR3 | R/W | Port 3 | XXXXXXXX$_B$ |
| $04_H$ | Port 4 data register | PDR4 | R/W | Port 4 | XXXXXXXX$_B$ |
| $05_H$ | Port 5 data register | PDR5 | R/W | Port 5 | XXXXXXXX$_B$ |
| $06_H$ | Port 6 data register | PDR6 | R/W | Port 6 | XXXXXXXX$_B$ |
| $07_H$ | Port 7 data register | PDR7 | R/W | Port 7 | XXXXXXXX$_B$ |
| $08_H$ | Port 8 data register | PDR8 | R/W | Port 8 | XXXXXXXX$_B$ |
| $09_H$ | Port 9 data register | PDR9 | R/W | Port 9 | XXXXXXXX$_B$ |
| $0A_H$ | Port A data register | PDRA | R/W | Port A | _ _ _ _ _ _ _ X$_B$ |
| $0B_H$ to $0F_H$ | Reserved | | | | |
| $10_H$ | Port 0 direction register | DDR0 | R/W | Port 0 | 0 0 0 0 0 0 0 0$_B$ |
| $11_H$ | Port 1 direction register | DDR1 | R/W | Port 1 | 0 0 0 0 0 0 0 0$_B$ |
| $12_H$ | Port 2 direction register | DDR2 | R/W | Port 2 | 0 0 0 0 0 0 0 0$_B$ |
| $13_H$ | Port 3 direction register | DDR3 | R/W | Port 3 | 0 0 0 0 0 0 0 0$_B$ |
| $14_H$ | Port 4 direction register | DDR4 | R/W | Port 4 | 0 0 0 0 0 0 0 0$_B$ |
| $15_H$ | Port 5 direction register | DDR5 | R/W | Port 5 | 0 0 0 0 0 0 0 0$_B$ |
| $16_H$ | Port 6 direction register | DDR6 | R/W | Port 6 | 0 0 0 0 0 0 0 0$_B$ |
| $17_H$ | Port 7 direction register | DDR7 | R/W | Port 7 | 0 0 0 0 0 0 0 0$_B$ |
| $18_H$ | Port 8 direction register | DDR8 | R/W | Port 8 | 0 0 0 0 0 0 0 0$_B$ |
| $19_H$ | Port 9 direction register | DDR9 | R/W | Port 9 | 0 0 0 0 0 0 0 0$_B$ |
| $1A_H$ | Port A direction register | DDRA | R/W | Port A | _ _ _ _ _ _ _ 0$_B$ |
| $1B_H$ | Analog Input Enable register | ADER | R/W | Port 6, A/D | 1 1 1 1 1 1 1 1$_B$ |
| $1C_H$ | Port 0 Pullup control register | PUCR0 | R/W | Port 0 | 0 0 0 0 0 0 0 0$_B$ |
| $1D_H$ | Port 1 Pullup control register | PUCR1 | R/W | Port 1 | 0 0 0 0 0 0 0 0$_B$ |
| $1E_H$ | Port 2 Pullup control register | PUCR2 | R/W | Port 2 | 0 0 0 0 0 0 0 0$_B$ |
| $1F_H$ | Port 3 Pullup control register | PUCR3 | R/W | Port 3 | 0 0 0 0 0 0 0 0$_B$ |
| $20_H$ | Serial Mode Control Register 0 | UMC0 | R/W | UART0 | 0 0 0 0 0 1 0 0$_B$ |
| $21_H$ | Serial Status Register 0 | USR0 | R/W | | 0 0 0 1 0 0 0 0$_B$ |
| $22_H$ | Serial input data register 0/ Serial output data register 0 | UIDR0/UODR0 | R/W | | XXXXXXXX$_B$ |
| $23_H$ | Rate and data register 0 | URD0 | R/W | | 0 0 0 0 0 0 0X$_B$ |

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| $A2_H$ to $A4_H$ | Prohibited | | | | |
| $A5_H$ | Automatic ready function select register | ARSR | W | External Memory Access | 0 0 1 1 _ _ 0 $0_B$ |
| $A6_H$ | External address output control register | HACR | W | | 0 0 0 0 0 0 0 $0_B$ |
| $A7_H$ | Bus control signal selection register | ECSR | W | | 0 0 0 0 0 0 0 $_B$ |
| $A8_H$ | Watchdog Timer control register | WDTC | R/W | Watchdog Timer | XXXXX 1 1 $1_B$ |
| $A9_H$ | Time Base Timer Control register | TBTC | R/W | Time Base Timer | 1 - - 0 0 1 0 $0_B$ |
| $AA_H$ | Watch timer control register | WTC | R/W | Watch Timer | 1 X 0 0 0 0 0 $0_B$ |
| $AB_H$ to $AD_H$ | Prohibited | | | | |
| $AE_H$ | Flash memory control status register (Flash only, otherwise reserved) | FMCS | R/W | Flash Memory | 0 0 0 X 0 0 0 $0_B$ |
| $AF_H$ | Prohibited | | | | |
| $B0_H$ | Interrupt control register 00 | ICR00 | R/W | Interrupt controller | 0 0 0 0 0 1 1 $1_B$ |
| $B1_H$ | Interrupt control register 01 | ICR01 | R/W | | 0 0 0 0 0 1 1 $1_B$ |
| $B2_H$ | Interrupt control register 02 | ICR02 | R/W | | 0 0 0 0 0 1 1 $1_B$ |
| $B3_H$ | Interrupt control register 03 | ICR03 | R/W | | 0 0 0 0 0 1 1 $1_B$ |
| $B4_H$ | Interrupt control register 04 | ICR04 | R/W | | 0 0 0 0 0 1 1 $1_B$ |
| $B5_H$ | Interrupt control register 05 | ICR05 | R/W | | 0 0 0 0 0 1 1 $1_B$ |
| $B6_H$ | Interrupt control register 06 | ICR06 | R/W | | 0 0 0 0 0 1 1 $1_B$ |
| $B7_H$ | Interrupt control register 07 | ICR07 | R/W | | 0 0 0 0 0 1 1 $1_B$ |
| $B8_H$ | Interrupt control register 08 | ICR08 | R/W | | 0 0 0 0 0 1 1 $1_B$ |
| $B9_H$ | Interrupt control register 09 | ICR09 | R/W | | 0 0 0 0 0 1 1 $1_B$ |
| $BA_H$ | Interrupt control register 10 | ICR10 | R/W | | 0 0 0 0 0 1 1 $1_B$ |
| $BB_H$ | Interrupt control register 11 | ICR11 | R/W | | 0 0 0 0 0 1 1 $1_B$ |
| $BC_H$ | Interrupt control register 12 | ICR12 | R/W | | 0 0 0 0 0 1 1 $1_B$ |
| $BD_H$ | Interrupt control register 13 | ICR13 | R/W | | 0 0 0 0 0 1 1 $1_B$ |
| $BE_H$ | Interrupt control register 14 | ICR14 | R/W | | 0 0 0 0 0 1 1 $1_B$ |
| $BF_H$ | Interrupt control register 15 | ICR15 | R/W | | 0 0 0 0 0 1 1 $1_B$ |
| $C0_H$ to $FF_H$ | External | | | | |

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| $1FF0_H$ | Program address detection register 0 | PADR0 | R/W | Address Match Detection Function | $XXXXXXXX_B$ |
| $1FF1_H$ | Program address detection register 0 | PADR0 | R/W | | $XXXXXXXX_B$ |
| $1FF2_H$ | Program address detection register 0 | PADR0 | R/W | | $XXXXXXXX_B$ |
| $1FF3_H$ | Program address detection register 1 | PADR1 | R/W | | $XXXXXXXX_B$ |
| $1FF4_H$ | Program address detection register 1 | PADR1 | R/W | | $XXXXXXXX_B$ |
| $1FF5_H$ | Program address detection register 1 | PADR1 | R/W | | $XXXXXXXX_B$ |

*(Continued)*

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 3928H | Output Compare Register 0 | OCCP0 | R/W | Output Compare 0/1 | XXXXXXXXB |
| 3929H | Output Compare Register 0 | OCCP0 | R/W | | XXXXXXXXB |
| 392AH | Output Compare Register 1 | OCCP1 | R/W | | XXXXXXXXB |
| 392BH | Output Compare Register 1 | OCCP1 | R/W | | XXXXXXXXB |
| 392CH | Output Compare Register 2 | OCCP2 | R/W | Output Compare 2/3 | XXXXXXXXB |
| 392DH | Output Compare Register 2 | OCCP2 | R/W | | XXXXXXXXB |
| 392EH | Output Compare Register 3 | OCCP3 | R/W | | XXXXXXXXB |
| 392FH | Output Compare Register 3 | OCCP3 | R/W | | XXXXXXXXB |
| 3930H to 39FFH | Reserved | | | | |
| 3A00H to 3AFFH | Reserved for CAN 0 Interface. | | | | |
| 3B00H to 3BFFH | Reserved for CAN 0 Interface. | | | | |
| 3C00H to 3CFFH | Reserved for CAN 1 Interface. | | | | |
| 3D00H to 3DFFH | Reserved for CAN 1 Interface. | | | | |
| 3E00H to 3FFFH | Reserved | | | | |

- Read/write notation
  - R/W : Reading and writing permitted
  - R : Read-only
  - W : Write-only

- Initial value notation
  - 0 : Initial value is “0”.
  - 1 : Initial value is “1”.
  - X : Initial value is undefined.
  - _ : Initial value is unused.

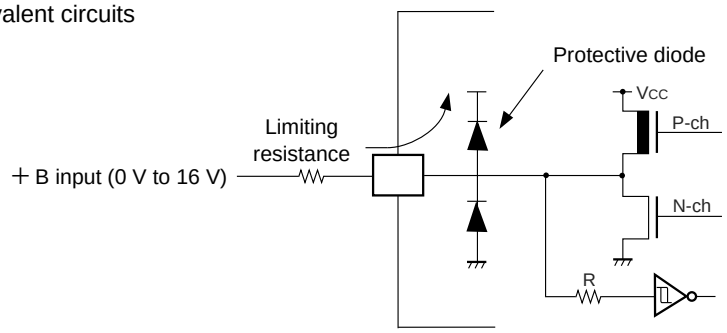
Note: Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

*(Continued)*

| Address | | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|---|
| CAN0 | CAN1 | | | | |
| 003A3C$_H$ | 003C3C$_H$ | ID register 7 | IDR7 | R/W | XXXXXXXX XXXXXXXX$_B$ |
| 003A3D$_H$ | 003C3D$_H$ | | | | |
| 003A3E$_H$ | 003C3E$_H$ | | | | XXXXX--- XXXXXXXX$_B$ |
| 003A3F$_H$ | 003C3F$_H$ | | | | |
| 003A40$_H$ | 003C40$_H$ | ID register 8 | IDR8 | R/W | XXXXXXXX XXXXXXXX$_B$ |
| 003A41$_H$ | 003C41$_H$ | | | | |
| 003A42$_H$ | 003C42$_H$ | | | | XXXXX--- XXXXXXXX$_B$ |
| 003A43$_H$ | 003C43$_H$ | | | | |
| 003A44$_H$ | 003C44$_H$ | ID register 9 | IDR9 | R/W | XXXXXXXX XXXXXXXX$_B$ |
| 003A45$_H$ | 003C45$_H$ | | | | |
| 003A46$_H$ | 003C46$_H$ | | | | XXXXX--- XXXXXXXX$_B$ |
| 003A47$_H$ | 003C47$_H$ | | | | |
| 003A48$_H$ | 003C48$_H$ | ID register 10 | IDR10 | R/W | XXXXXXXX XXXXXXXX$_B$ |
| 003A49$_H$ | 003C49$_H$ | | | | |
| 003A4A$_H$ | 003C4A$_H$ | | | | XXXXX--- XXXXXXXX$_B$ |
| 003A4B$_H$ | 003C4B$_H$ | | | | |
| 003A4C$_H$ | 003C4C$_H$ | ID register 11 | IDR11 | R/W | XXXXXXXX XXXXXXXX$_B$ |
| 003A4D$_H$ | 003C4D$_H$ | | | | |
| 003A4E$_H$ | 003C4E$_H$ | | | | XXXXX--- XXXXXXXX$_B$ |
| 003A4F$_H$ | 003C4F$_H$ | | | | |
| 003A50$_H$ | 003C50$_H$ | ID register 12 | IDR12 | R/W | XXXXXXXX XXXXXXXX$_B$ |
| 003A51$_H$ | 003C51$_H$ | | | | |
| 003A52$_H$ | 003C52$_H$ | | | | XXXXX--- XXXXXXXX$_B$ |
| 003A53$_H$ | 003C53$_H$ | | | | |
| 003A54$_H$ | 003C54$_H$ | ID register 13 | IDR13 | R/W | XXXXXXXX XXXXXXXX$_B$ |
| 003A55$_H$ | 003C55$_H$ | | | | |
| 003A56$_H$ | 003C56$_H$ | | | | XXXXX--- XXXXXXXX$_B$ |
| 003A57$_H$ | 003C57$_H$ | | | | |
| 003A58$_H$ | 003C58$_H$ | ID register 14 | IDR14 | R/W | XXXXXXXX XXXXXXXX$_B$ |
| 003A59$_H$ | 003C59$_H$ | | | | |
| 003A5A$_H$ | 003C5A$_H$ | | | | XXXXX--- XXXXXXXX$_B$ |
| 003A5B$_H$ | 003C5B$_H$ | | | | |
| 003A5C$_H$ | 003C5C$_H$ | ID register 15 | IDR15 | R/W | XXXXXXXX XXXXXXXX$_B$ |
| 003A5D$_H$ | 003C5D$_H$ | | | | |
| 003A5E$_H$ | 003C5E$_H$ | | | | XXXXX--- XXXXXXXX$_B$ |
| 003A5F$_H$ | 003C5F$_H$ | | | | |

- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept + B signal input.
- Sample recommended circuits :

■ Input/Output Equivalent circuits




WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

*(Continued)*

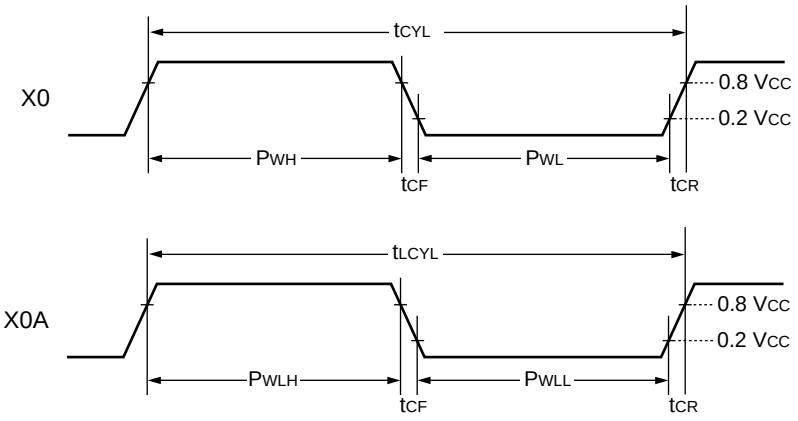
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC}$ = 3.5 V to 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = −40 °C to +105 °C)

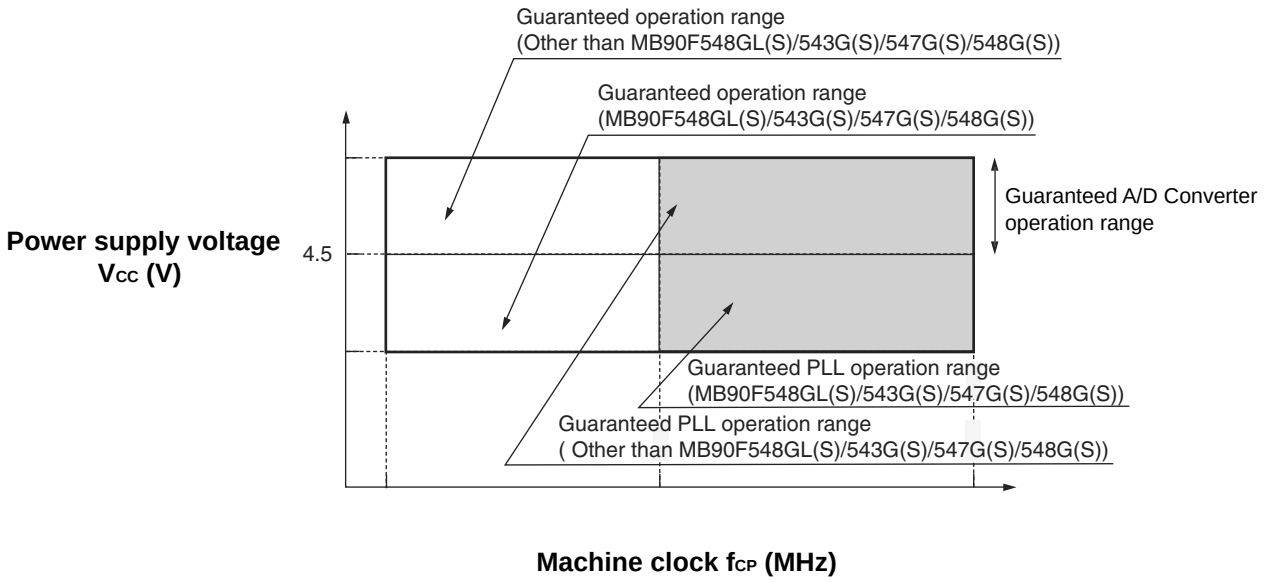
| Parameter | Symbol | Pin name | Condition | Value | | | Units | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current* | $I_{CC}$ | $V_{CC}$ | Internal frequency : 16 MHz, At normal operating | − | 40 | 55 | mA | |
| | | | Internal frequency : 16 MHz, At Flash programming/erasing | − | 50 | 70 | mA | Flash device |
| | $I_{CCS}$ | | Internal frequency : 16 MHz, At sleep mode | − | 12 | 20 | mA | |
| | $I_{CTS}$ | | $V_{CC}$ = 5.0 V ± 10%, Internal frequency : 2 MHz, At pseudo timer mode | − | 300 | 600 | µA | |
| | | | | − | 600 | 1100 | µA | MB90F548GL (S) only |
| | | | | − | 200 | 400 | µA | MB90543G(S)/547G(S)/548(S) only |
| | $I_{CCL}$ | | Internal frequency : 8 kHz, At sub operation, $T_A$ = 25 °C | − | 400 | 750 | µA | MB90F548GL only |
| | | | | − | 50 | 100 | µA | MASK ROM |
| | | | | − | 150 | 300 | µA | Flash device |
| | $I_{CCLS}$ | | Internal frequency : 8 kHz, At sub sleep, $T_A$ = 25 °C | − | 15 | 40 | µA | |
| | $I_{CCT}$ | | Internal frequency : 8 kHz, At timer mode, $T_A$ = 25 °C | − | 7 | 25 | µA | |
| | $I_{CCH1}$ | | At stop, $T_A$ = 25 °C | − | 5 | 20 | µA | |
| | $I_{CCH2}$ | | At hardware standby mode, $T_A$ = 25 °C | − | 50 | 100 | µA | |
| Input capacity | $C_{IN}$ | Other than $AV_{CC}$, $AV_{SS}$, AVRH, AVRL, C, $V_{CC}$, $V_{SS}$ | − | − | 5 | 15 | pF | |

* : The power supply current testing conditions are when using the external clock.

■ **Clock Timing**




■ **Guaranteed PLL operation range**



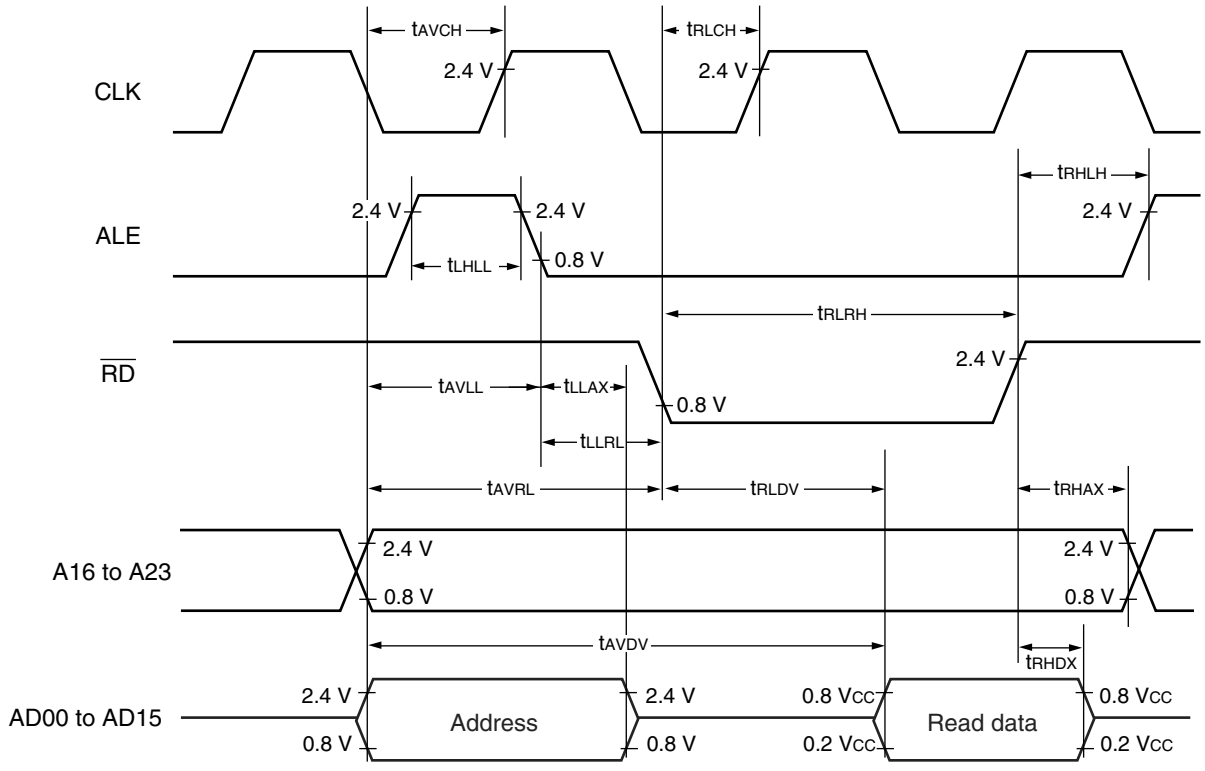
### 11.4.5 Bus Timing (Read)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC}$ = 3.5 V to 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = − 40 °C to + 105 °C)

| Parameter | Symbol | Pin name | Condition | Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| ALE pulse width | $t_{LHLL}$ | ALE | | $t_{CP}/2 - 20$ | − | ns | |
| Valid address → ALE↓ time | $t_{AVLL}$ | ALE, A16 to A23, AD00 to AD15 | | $t_{CP}/2 - 20$ | − | ns | |
| ALE↓ → Address valid time | $t_{LLAX}$ | ALE, AD00 to AD15 | | $t_{CP}/2 - 15$ | − | ns | |
| Valid address → $\overline{RD}$↓ time | $t_{AVRL}$ | A16 toA23, AD00 to AD15, $\overline{RD}$ | | $t_{CP} - 15$ | − | ns | |
| Valid address → Valid data input | $t_{AVDV}$ | A16 to A23, AD00 to AD15 | | − | $5\ t_{CP}/2 - 60$ | ns | |
| $\overline{RD}$ pulse width | $t_{RLRH}$ | RD | − | $3\ t_{CP}/2 - 20$ | − | ns | |
| $\overline{RD}$↓ → Valid data input | $t_{RLDV}$ | $\overline{RD}$, AD00 to AD15 | | − | $3\ t_{CP}/2 - 60$ | ns | |
| $\overline{RD}$↑ → Data hold time | $t_{RHDX}$ | $\overline{RD}$, AD00 to AD15 | | 0 | − | ns | |
| $\overline{RD}$↑ → ALE↑ time | $t_{RHLH}$ | $\overline{RD}$, ALE | | $t_{CP}/2 - 15$ | − | ns | |
| $\overline{RD}$↑ → Address valid time | $t_{RHAX}$ | $\overline{RD}$, A16 to A23 | | $t_{CP}/2 - 10$ | − | ns | |
| Valid address → CLK↑ time | $t_{AVCH}$ | A16 to A23, AD00 to AD15, CLK | | $t_{CP}/2 - 20$ | − | ns | |
| $\overline{RD}$↓ → CLK↑ time | $t_{RLCH}$ | $\overline{RD}$, CLK | | $t_{CP}/2 - 20$ | − | ns | |
| ALE↓ → $\overline{RD}$↓ time | $t_{LLRL}$ | ALE, $\overline{RD}$ | | $t_{CP}/2 - 15$ | − | ns | |

■ **Bus Timing (Read)**



## 11.5 A/D Converter

### 11.5.1 Electrical Characteristics

($V_{CC} = AV_{CC} = 5.0\ V \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\ V$, $3.0\ V \leq AVRH - AVRL$, $T_A = -40\ °C$ to $+105\ °C$)

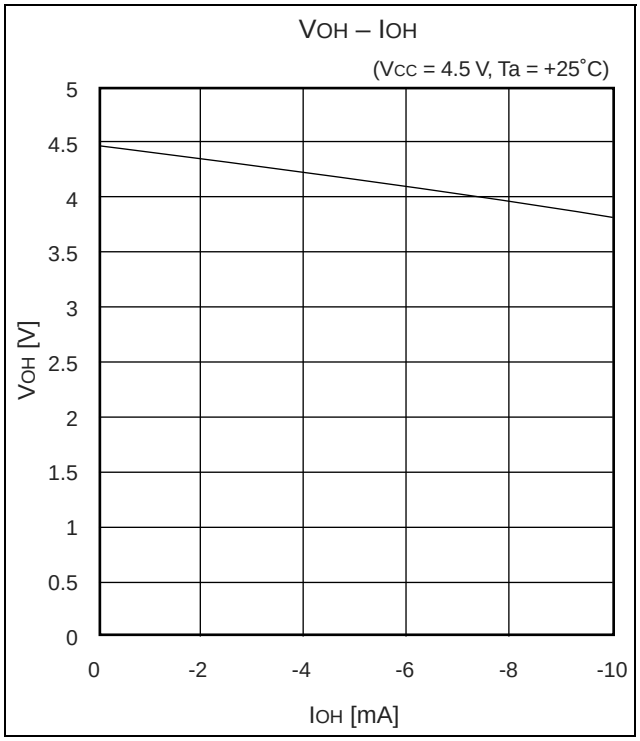
| Parameter | Symbol | Pin name | Value | | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | — | 10 | bit | |
| Conversion error | — | — | — | — | ±5.0 | LSB | |
| Nonlinearity error | — | — | — | — | ±2.5 | LSB | |
| Differential nonlinearity error | — | — | — | — | ±1.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | AN0 to AN7 | AVRL − 3.5 LSB | AVRL + 0.5 LSB | AVRL + 4.5 LSB | V | |
| Full scale transition voltage | $V_{FST}$ | AN0 to AN7 | AVRH − 6.5 LSB | AVRH − 1.5 LSB | AVRH + 1.5 LSB | V | |
| Compare time | — | — | 352 $t_{CP}$ | — | — | ns | Internal frequency : 16 MHz |
| Sampling time | — | — | 64 $t_{CP}$ | — | — | ns | Internal frequency : 16 MHz |
| Analog port input current | $I_{AIN}$ | AN0 to AN7 | −1 | — | 1 | µA | $V_{CC} = AV_{CC} = 5.0\ V \pm 1\%$ |
| Analog input voltage range | $V_{AIN}$ | AN0 to AN7 | AVRL | — | AVRH | V | |
| Reference voltage range | — | AVRH | AVRL + 2.7 | — | $AV_{CC}$ | V | |
| | — | AVRL | 0 | — | AVRH − 2.7 | V | |
| Power supply current | $I_A$ | $AV_{CC}$ | — | 5 | — | mA | |
| | $I_{AH}$ | $AV_{CC}$ | — | — | 5 | µA | * |
| Reference voltage supply current | $I_R$ | AVRH | — | 400 | 600 | µA | Flash device |
| | | | — | 140 | 260 | µA | MASK ROM |
| | $I_{RH}$ | AVRH | — | — | 5 | µA | * |
| Offset between input channels | — | AN0 to AN7 | — | — | 4 | LSB | |

* : When not using an A/D converter, this is the current ($V_{CC} = AV_{CC} = AVRH = 5.0\ V$) when the CPU is stopped.

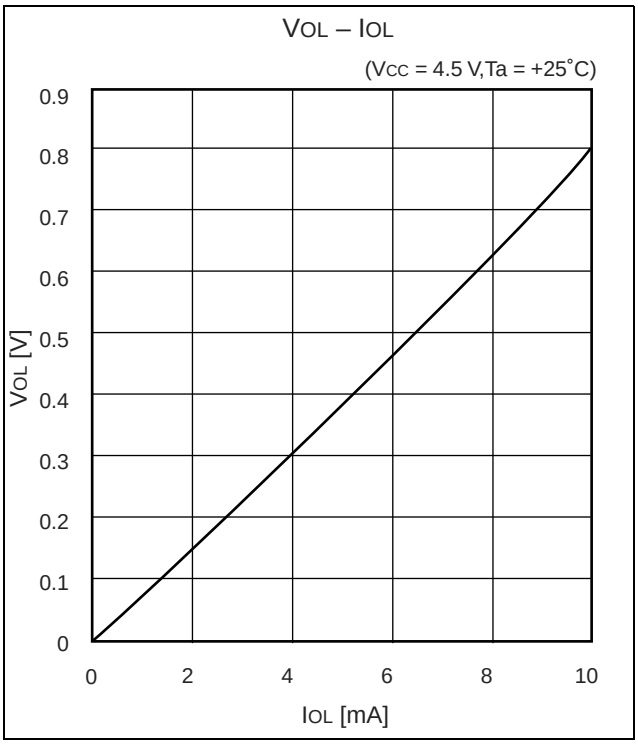
Note: The functionality of the A/D converter is only guaranteed for VCC = 5.0 V ± 10 % (also for MB90543G(S)/547G(S)/548G(S)/F548G(S)/F548GL(S)).

## 12. Example Characteristics

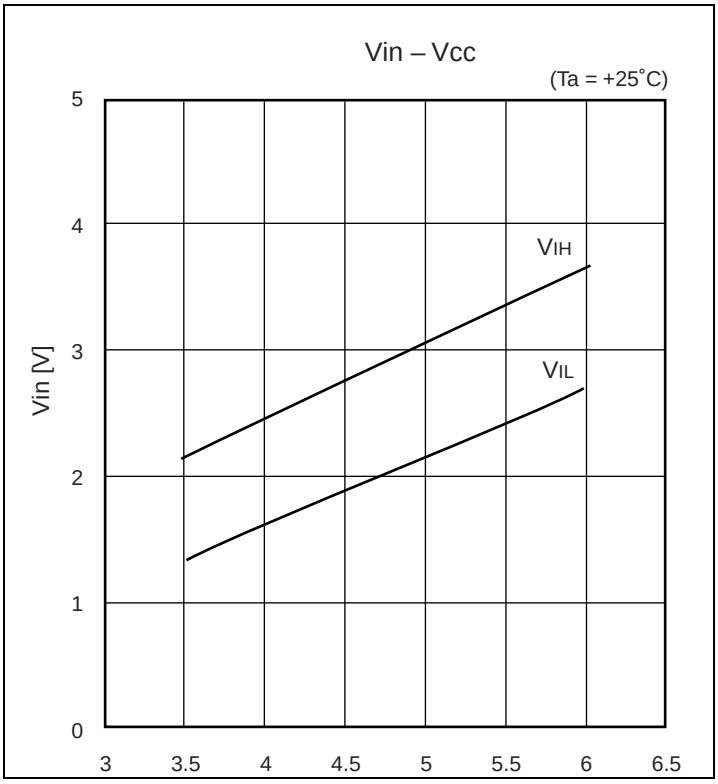
- "H" level output voltage

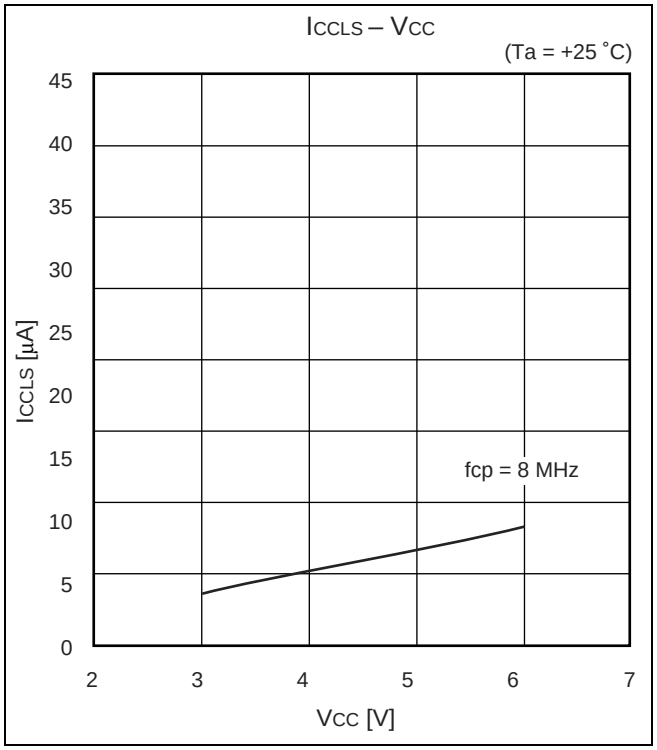


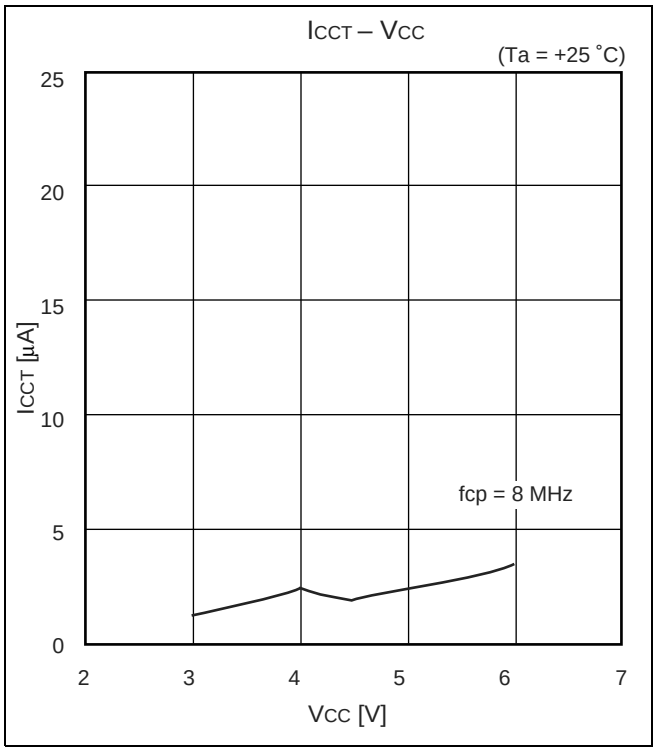

- "L" level output voltage

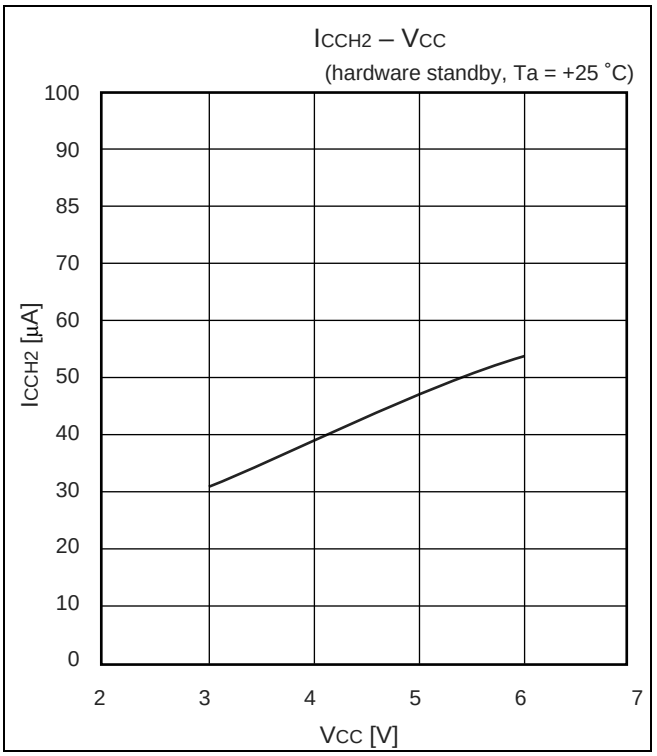


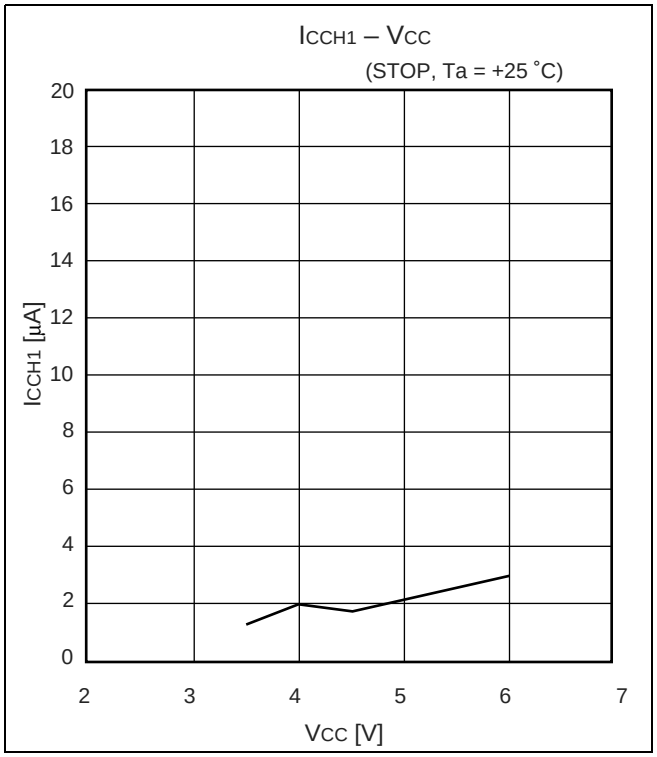

- "H" level input voltage/ "L" level input voltage (Hysterisis inpiut)



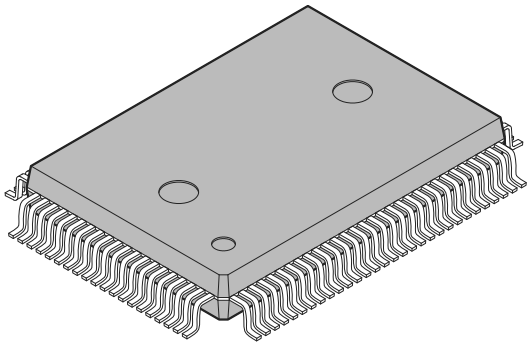

ICCLS – VCC
(Ta = +25 ˚C)
ICCLS [µA]
45
40
35
30
25
20
15
10
5
0
fcp = 8 MHz
2
3
4
5
6
7
VCC [V]


ICCT – VCC
(Ta = +25 ˚C)
ICCT [µA]
25
20
15
10
5
0
fcp = 8 MHz
2
3
4
5
6
7
VCC [V]


ICCH2 – VCC
(hardware standby, Ta = +25 ˚C)
ICCH2 [µA]
100
90
85
70
60
50
40
30
20
10
0
2
3
4
5
6
7
VCC [V]


ICCH1 – VCC
(STOP, Ta = +25 ˚C)
ICCH1 [µA]
20
18
16
14
12
10
8
6
4
2
0
2
3
4
5
6
7
VCC [V]

## 14. Package Dimensions

| | | |
|---|---|---|
|  | | |
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| | | |
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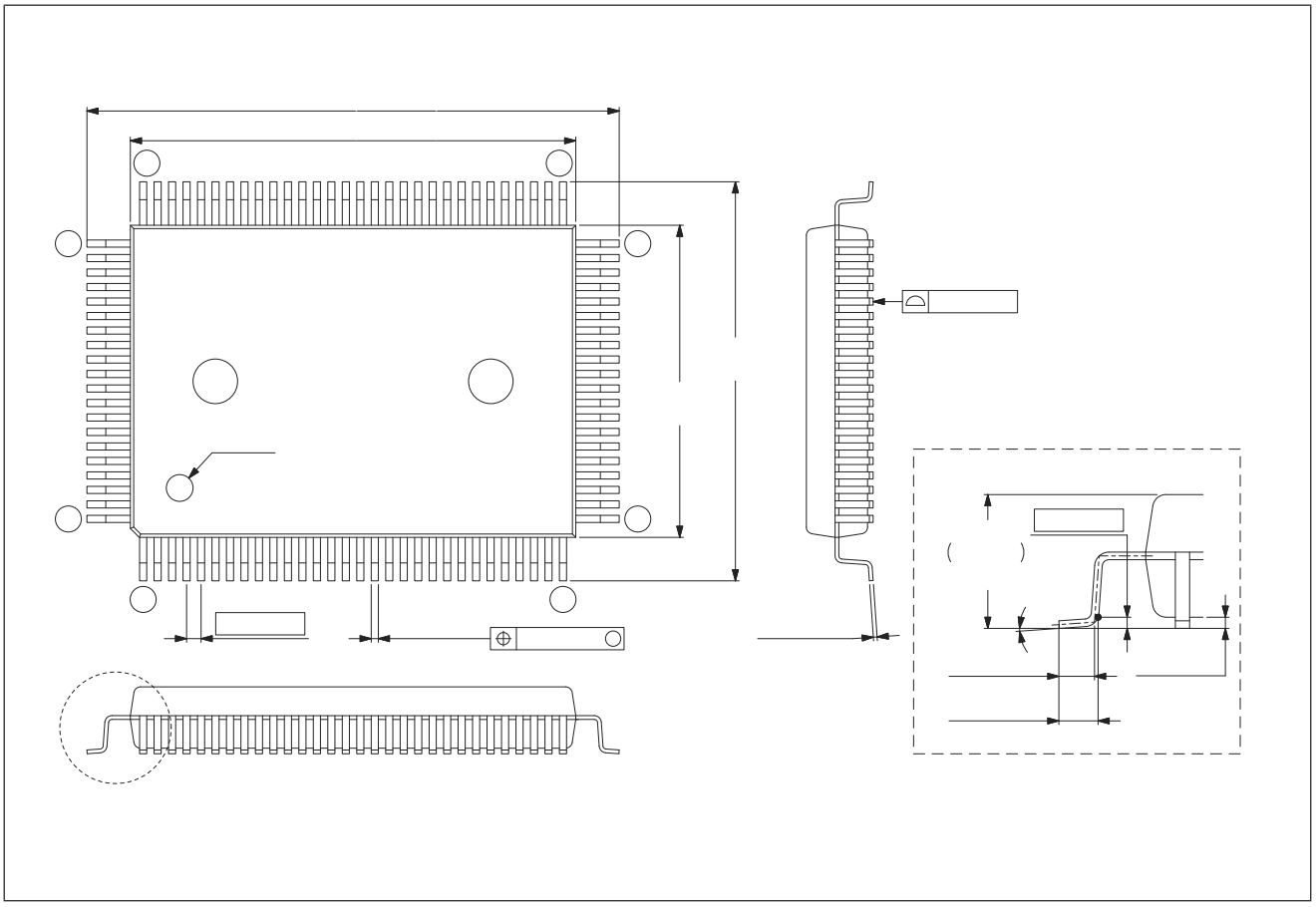
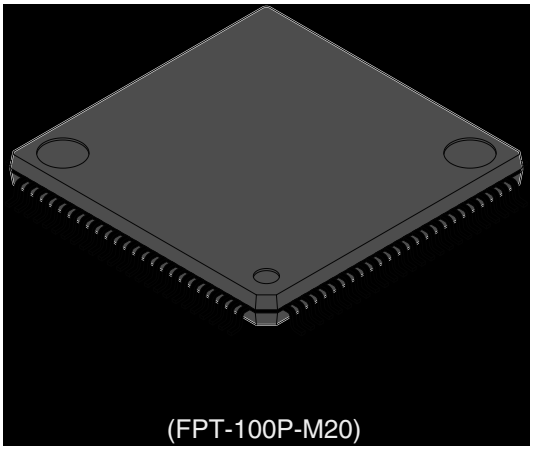
| | | |
| | | |
| | | |

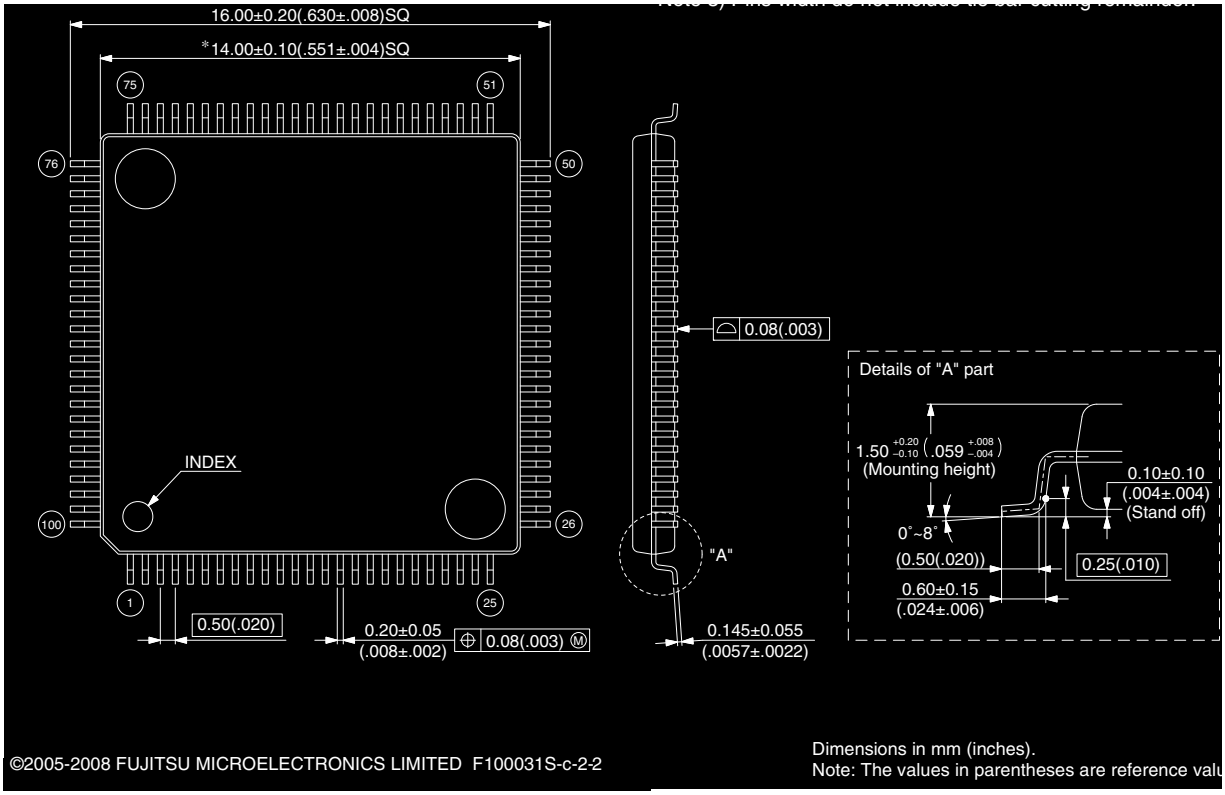


*(Continued)*

*(Continued)*



(FPT-100P-M20)



## 15. Major Changes

Spansion Publication Number: DS07-13703-7E

| Section | Change Results |
|---|---|
| ■ PRODUCT LINEUP | Changed the name in peripheral resource.<br>16-bit I/O Timer → 16-bit Free-run Timer |
| ■ I/O CIRCUIT TYPE | Changed the name of input typ.<br>Hysteresis → CMOS Hysteresis<br>HYS → CMOS Hysteresis |
| ■ BLOCK DIAGRAM | Changed the arrow direction of SOT1 signal at UART1(SCI).<br>"← →" (input/output) → "←" (output) |
| ■ I/O MAP | Changed the text of "Note". |
| ■ INTERRUPT MAP | Changed the name of peripheral resource of the pin number: #19.<br>I/O Timer → 16-bit Free-run Timer |
| ■ ELECTRICAL CHARACTERISTICS<br>2. Recommended Conditions | Changed the remarks of "parameter: Power supply voltage". |
| 3. DC Characteristics | Changed the maximum value of symbol : VILM of parameter: Input voltage.<br>$V_{CC}$ + 0.3 → $V_{SS}$ + 0.3 |
| | Added the following remarks for parameter : Pull-down resistance.<br>Except Flash device |
| 4. AC Characteristics<br>(1) Clock Timing | Added the value when using an external clock in Oscillation frequency and Clock cycle time on (1) Clock Timing for parameter. |
| | Added the item of A/D converter operation range in figure of "■ Guaranteed PLL operation range" |
| (3) Reset and Hardware Standby Input Timing | Changed the following item.<br>(3) Reset and Hardware Standby Input Timing Remarks:<br>In sub-clock mode, sub-sleep mode, timer mode<br>$2t_{CP}$ → $2t_{LCP}$ |
| (4) Power On Reset | Changed as follows;<br>Due to repetitive operation → Waiting time until power-on |
| 5. A/D Converter | Changed the unit of Zero transition voltage and Full scale transition voltage.<br>mV → V |
| ■ ORDERING INFORMATION | Added the MB90F548GLPMC in Part Numbers. |

**NOTE: Please see "Document History" about later revised information.**

## Document History

**Document Title: MB90F543G(S)/546G(S)/548G(S)/549G(S)/549G(S)/V540G/MB90543G(S)/547G(S)/548G(S)/F548GL(S) CMOS F2MC-16LX MB90540G/545G Series 16-bit Proprietary Microcontroller**
**Document Number: 002-07696**

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | — | AKIH | 11/13/2008 | Migrated to Cypress and assigned document number 002-07696.<br>No change to document contents or format. |
| *A | 5537115 | AKIH | 11/30/2016 | Updated to Cypress template |