



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f548gspf-g

Contents

Features.....	1
Product Lineup	4
Pin Assignment	7
Pin Description	9
I/O Circuit Type	14
Handling Devices.....	17
Block Diagram	21
Memory Map.....	22
I/O Map.....	23
CAN Controller.....	29

Interrupt Map.....	35
Electrical Characteristics.....	37
Example Characteristics.....	61
Ordering Information.....	66
Package Dimensions.....	67
Major Changes.....	69
Document History.....	69
Sales, Solutions, and Legal Information	70

Features	MB90F543G (S) /F548G (S) MB90F549G (S) /F546G (S) MB90F548GL(S)	MB90543G (S) MB90547G (S) MB90548G (S) MB90549G (S)	MB90V540G
16-bit Reload Timer (2 channels)	Operation clock frequency : $f_{sys}/2^1$, $f_{sys}/2^3$, $f_{sys}/2^5$ (f_{sys} = System clock frequency) Supports External Event Count function Signals an interrupt when overflow		
16-bit Free-run Timer	Supports Timer Clear when a match with Output Compare (Channel 0) Operation clock freq. : $f_{sys}/2^2$, $f_{sys}/2^4$, $f_{sys}/2^6$, $f_{sys}/2^8$ (f_{sys} = System clock freq.)		
16-bit Output Compare (4 channels)	Signals an interrupt when a match with 16-bit Free-run Timer Four 16-bit compare registers A pair of compare registers can be used to generate an output signal		
16-bit Input Capture (8 channels)	Rising edge, falling edge or rising & falling edge sensitive Four 16-bit Capture registers Signals an interrupt upon external event		
8/16-bit Programmable Pulse Generator (4 channels)	Supports 8-bit and 16-bit operation modes Eight 8-bit reload counters Eight 8-bit reload registers for L pulse width Eight 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter 4 output pins Operation clock freq. : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$ or $128 \mu s @ f_{osc} = 4 \text{ MHz}$ (f_{sys} = System clock frequency, f_{osc} = Oscillation clock frequency)		
CAN Interface MB90540G series : 2 channels MB90545G series : 1 channel	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's supports multiple messages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps		
32 kHz Sub-clock	Sub-clock for low power operation		
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive		
External bus interface	External access using the selectable 8-bit or 16-bit bus is enabled (external bus mode.)		
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs and schmitt trigger inputs Bit-wise programmable as input/output or peripheral signal Sub-clock for 32 kHz Sub clock low power operation		
Flash Memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Erase-Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block Block protection by externally programmed voltage		

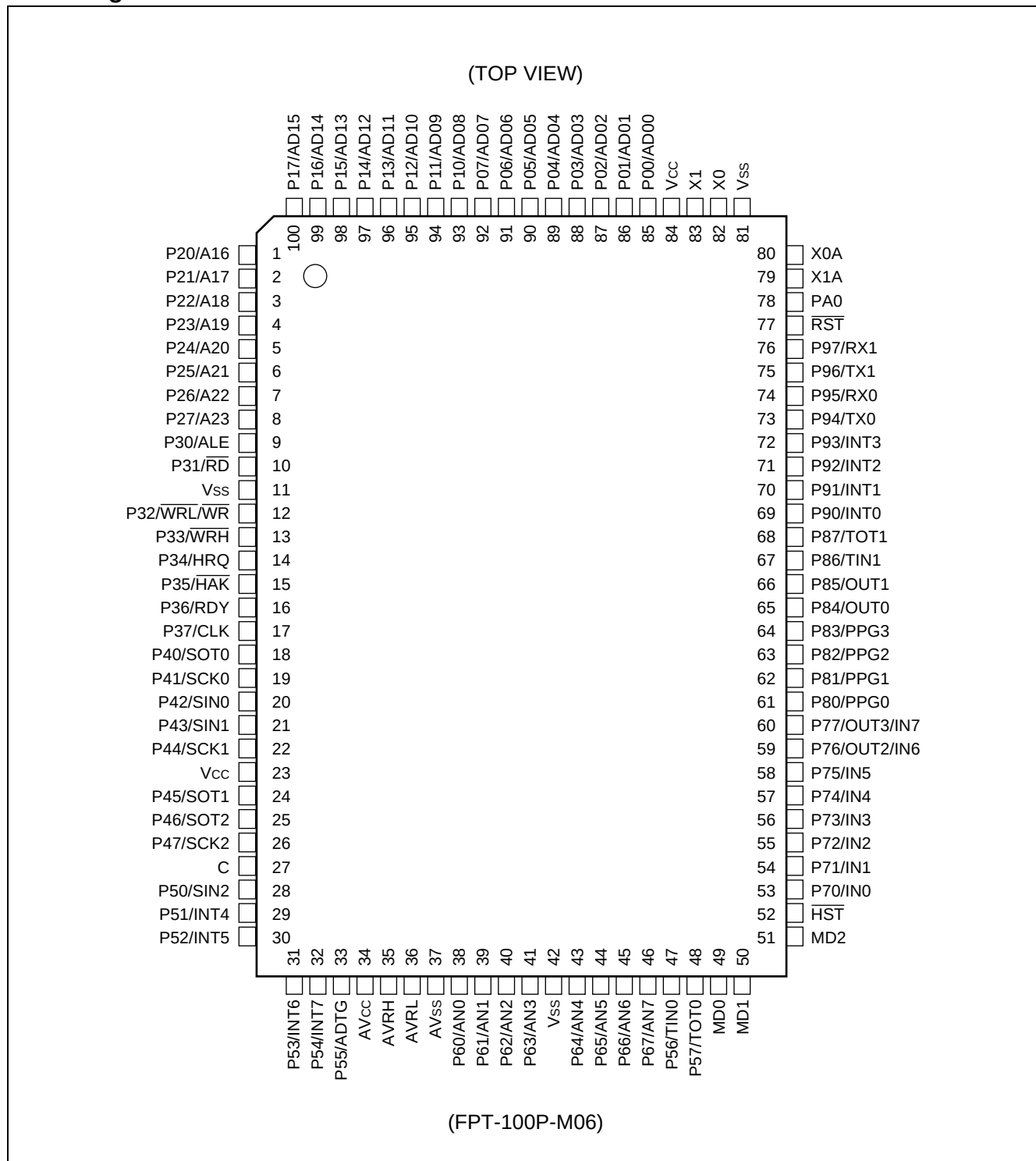
*1 : If the one clock system is used, equip X0A and X1A with clocks from the tool side.

*2 : It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used. Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*3 : Operating Voltage Range

Products	Operation guarantee range
MB90F543G(S)/F546G(S)/F548G(S)/ MB90549G(S)/F549G(S)/V540/V540G	4.5 V to 5.5 V
MB90F548GL(S)/543G(S)/547G(S)/548G(S)	3.5 V to 5.5 V

2. Pin Assignment



3. Pin Description

Pin No.		Pin name	Circuit type	Function
LQFP ²	QFP ¹			
80 81	82 83	X0 X1	A (Oscillation)	High speed crystal oscillator input pins
78	80	X0A	A (Oscillation)	Low speed crystal oscillator input pins. For the one clock system parts, perform external pull-down processing.
77	79	X1A		Low speed crystal oscillator input pins. For the one clock system parts, leave it open.
75	77	$\overline{\text{RST}}$	B	External reset request input pin
50	52	$\overline{\text{HST}}$	C	Hardware standby input pin
83 to 90	85 to 92	P00 to P07	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
91 to 98	93 to 100	P10 to P17	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		AD08 to AD15		I/O pins for 8 higher bits of the external address/data bus. This function is enabled when the external bus is enabled.
99 to 6	1 to 8	P20 to P27	I	General I/O port with programmable pullup. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to "1".
		A16 to A23		8-bit I/O pins for A16 to A23 at the external address/data bus. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to "0".
7	9	P30	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
8	10	P31	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		$\overline{\text{RD}}$		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.
10	12	P32	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the $\overline{\text{WR}}/\overline{\text{WRL}}$ pin output is disabled.
		$\overline{\text{WRL}}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{\text{WR}}/\overline{\text{WRL}}$ pin output are enabled. $\overline{\text{WRL}}$ is write-strobe output pin for the lower 8 bits of the data bus in 16-bit access.
		$\overline{\text{WR}}$		$\overline{\text{WR}}$ is write-strobe output pin for the 8 bits of the data bus in 8-bit access.

(Continued)

Pin No.		Pin name	Circuit type	Function
LQFP ²	QFP ¹			
46	48	P57	D	General I/O port. This function is enabled when the 16-bit reload timers 0 disables the output.
		TOT0		Output pin for the 16-bit reload timers 0. This function is enabled when the 16-bit reload timers 0 enables the output.
51 to 56	53 to 58	P70 to P75	D	General I/O ports. This function is always enabled.
		IN0 to IN5		Trigger input pins for input captures ICU0 to ICU5. Set the corresponding Port Direction Register to input if this function is used.
57 , 58	59 , 60	P76 , P77	D	General I/O ports. This function is enabled when the OCU disables the waveform output.
		OUT2 , OUT3		Event output pins for output compares OCU2 and OCU3. This function is enabled when the OCU enables the waveform output.
		IN6 , IN7		Trigger input pins for input captures ICU6 and ICU7. Set the corresponding Port Direction Register to input and disable the OCU waveform output if this function is used.
59 to 62	61 to 64	P80 to P83	D	General I/O ports. This function is enabled when 8/16-bit PPG disables the waveform output.
		PPG0 to PPG3		Output pins for 8/16-bit PPGs. This function is enabled when 8/16-bit PPG enables the waveform output.
63 , 64	65 , 66	P84 , P85	D	General I/O ports. This function is enabled when the OCU disables the waveform output.
		OUT0 , OUT1		Waveform output pins for output compares OCU0 and OCU1. This function is enabled when the OCU enables the waveform output.
65	67	P86	D	General I/O port. This function is always enabled.
		TIN1		Input pin for the 16-bit reload timers 1. Set the corresponding Port Direction Register to input if this function is used.
66	68	P87	D	General I/O port. This function is enabled when the 16-bit reload timers 1 disables the output.
		TOT1		Output pin for the 16-bit reload timers 1. This function is enabled when the 16-bit reload timers 1 enables the output.
67 to 70	69 to 72	P90 to P93	D	General I/O port. This function is always enabled.
		INT0 to INT3		External interrupt request input pins for INT0 to INT3. Set the corresponding Port Direction Register to input if this function is used.
71	73	P94	D	General I/O port. This function is enabled when CAN0 disables the output.
		TX0		TX output pin for CAN0. This function is enabled when CAN0 enables the output.

(Continued)

(Continued)

Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
72	74	P95	D	General I/O port. This function is always enabled.
		RX0		RX input pin for CAN0 Interface. When the CAN function is used, output from the other functions must be stopped.
73	75	P96	D	General I/O port. This function is enabled when CAN1 disables the output.
		TX1		TX output pin for CAN1. This function is enabled when CAN1 enables the output (only MB90540G series) .
74	76	P97	D	General I/O port. This function is always enabled.
		RX1		RX input pin for CAN1 Interface. When the CAN function is used, output from the other functions must be stopped (only MB90540G series) .
76	78	PA0	D	General I/O port. This function is always enabled.
32	34	AV _{CC}	Power supply	Power supply pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AV _{CC} is applied to V _{CC} .
35	37	AV _{SS}	Power supply	Power supply pin for the A/D Converter.
33	35	AVRH	Power supply	External reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV _{CC} .
34	36	AVRL	Power supply	External reference voltage input pin for the A/D Converter.
47, 48	49, 50	MD0, MD1	C	Input pins for specifying the operating mode. The pins must be directly connected to V _{CC} or V _{SS} .
49	51	MD2	F	Input pin for specifying the operating mode. The pin must be directly connected to V _{CC} or V _{SS} .
25	27	C	—	Power supply stabilization capacitor pin. It should be connected externally to an 0.1 μF ceramic capacitor.
21, 82	23, 84	V _{CC}	Power supply	Input pin for power supply (5.0 V) .
9, 40, 79	11, 42, 81	V _{SS}	Power supply	Input pin for power supply (0.0 V) .

*1 : FPT-100P-M06

*2 : FPT-100P-M20

5. Handling Devices

(1) Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} .
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, care must also be taken in not allowing the analog power-supply voltage (AV_{CC} , $AVRH$) to exceed the digital power-supply voltage.

(2) Handling unused pins

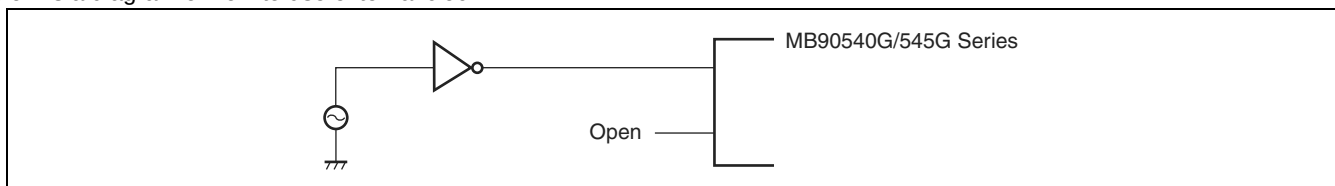
Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 k Ω .

Unused bi-directional pins should be set to the output state and can be left open, or the input state with the above described connection.

(3) Using external clock

To use external clock, drive X0 pin only and leave X1 pin unconnected.

Below is a diagram of how to use external clock.



(4) Use of the sub-clock

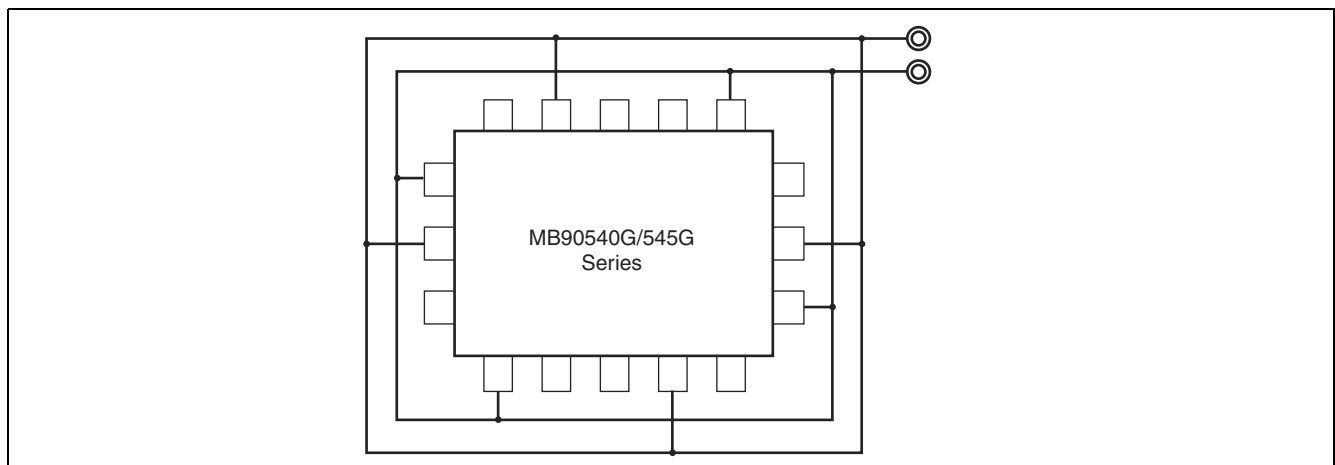
Use one clock system parts when the sub-clock is not used. In that case, pull-down the pin X0A and leave the pin X1A open. When using two clock system parts, a 32 kHz oscillator has to be connected to the X0A and X1A pins.

(5) Power supply pins (V_{CC}/V_{SS})

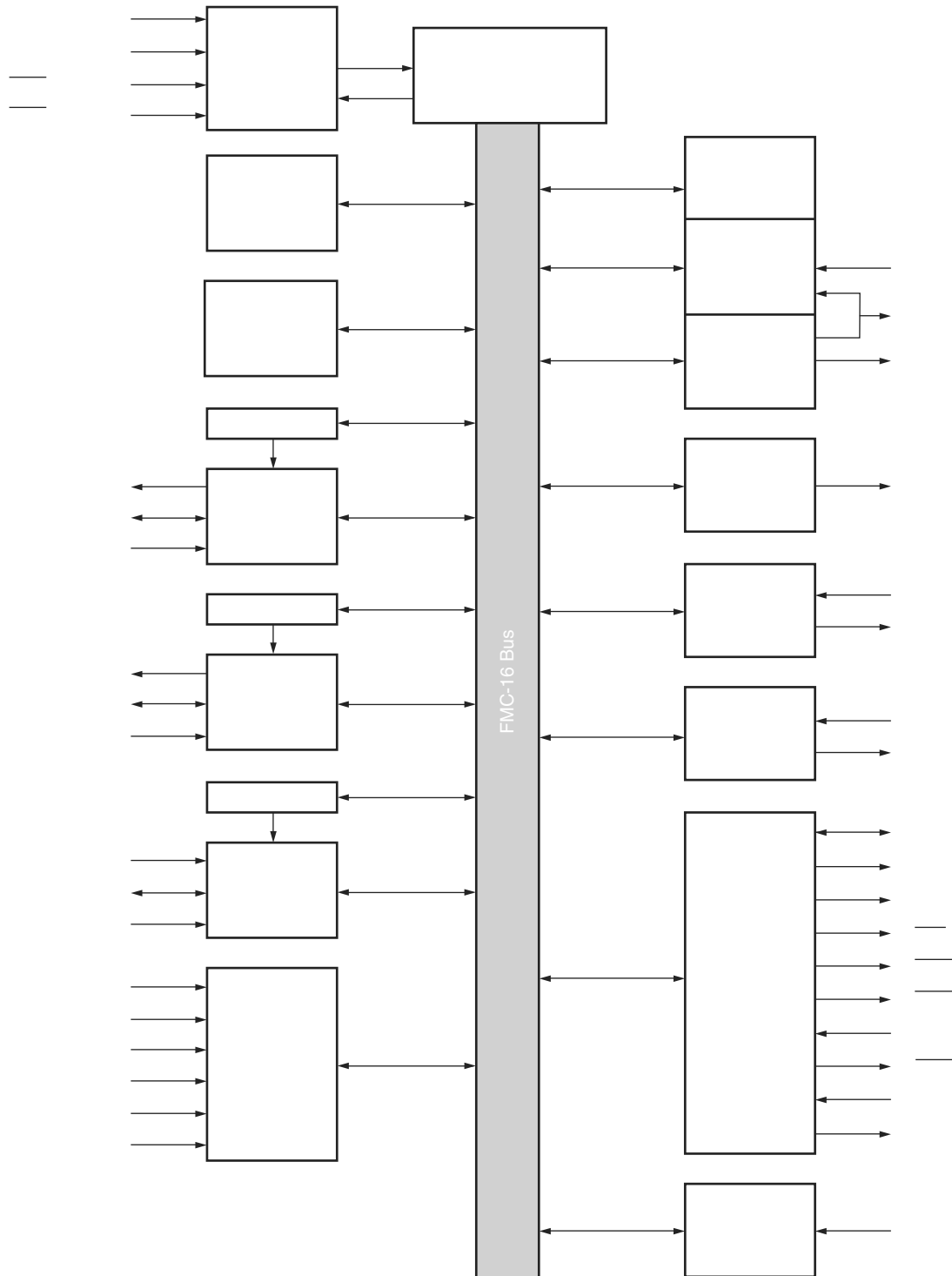
In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to an external power and a ground line to lower the electromagnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect V_{CC} and V_{SS} pins via the lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 μF between V_{CC} and V_{SS} pins near the device.



6. Block Diagram



* : Only the MB90540G series has two channels

Address	Register	Abbreviation	Access	Resource name	Initial value
24 _H	Serial mode register 1	SMR1	R/W	UART1	0 0 0 0 0 0 0 0 _B
25 _H	Serial control register 1	SCR1	R/W		0 0 0 0 0 1 0 0 _B
26 _H	Serial input data register 1/ Serial output data register 1	SIDR1/SODR1	R/W		XXXXXXXX _B
27 _H	Serial status register 1	SSR1	R/W		0 0 0 0 1 _ 0 0 _B
28 _H	UART1 prescaler control register	CDCR	R/W		0 _ _ 1 1 1 1 _B
29 _H	Serial Edge select register	SES1	R/W		_ _ _ _ _ 0 _B
2A _H	Prohibited				
2B _H	Serial I/O prescaler	SCDCR	R/W	Extended I/O Serial Interface	0 _ _ 1 1 1 1 _B
2C _H	Serial mode control register	SMCS	R/W		_ _ _ 0 0 0 0 _B
2D _H	Serial mode control register	SMCS	R/W		0 0 0 0 0 1 0 _B
2E _H	Serial data register	SDR	R/W		XXXXXXXX _B
2F _H	Serial Edge select register	SES2	R/W		_ _ _ _ _ 0 _B
30 _H	External interrupt enable register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0 _B
31 _H	External interrupt request register	EIRR	R/W		XXXXXXXX _B
32 _H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0 _B
33 _H	External interrupt level register	ELVR	R/W		0 0 0 0 0 0 0 0 _B
34 _H	A/D control status register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0 _B
35 _H	A/D control status register 1	ADCS1	R/W		0 0 0 0 0 0 0 0 _B
36 _H	A/D data register 0	ADCR0	R		XXXXXXXX _B
37 _H	A/D data register 1	ADCR1	R/W		0 0 0 0 1 _ XX _B
38 _H	PPG0 operation mode control register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 _ _ 1 _B
39 _H	PPG1 operation mode control register	PPGC1	R/W		0 _ 0 0 0 0 1 _B
3A _H	PPG0/1 clock selection register	PPG01	R/W		0 0 0 0 0 _ _ _B
3B _H	Prohibited				
3C _H	PPG2 operation mode control register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 _ _ 1 _B
3D _H	PPG3 operation mode control register	PPGC3	R/W		0 _ 0 0 0 0 1 _B
3E _H	PPG2/3 Clock Selection Register	PPG23	R/W		0 0 0 0 0 _ _ _B
3F _H	Prohibited				
40 _H	PPG4 operation mode control register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 _ _ 1 _B
41 _H	PPG5 operation mode control register	PPGC5	R/W		0 _ 0 0 0 0 1 _B
42 _H	PPG4/5 clock selection register	PPG45	R/W		0 0 0 0 0 _ _ _B
43 _H	Prohibited				
44 _H	PPG6 operation mode control register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 _ _ 1 _B
45 _H	PPG7 operation mode control register	PPGC7	R/W		0 _ 0 0 0 0 1 _B
46 _H	PPG6/7 clock selection register	PPG67	R/W		0 0 0 0 0 _ _ _B

(Continued)

(Continued)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A88 _H to 003A8F _H	003C88 _H to 003C8F _H	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
003A90 _H to 003A97 _H	003C90 _H to 003C97 _H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
003A98 _H to 003A9F _H	003C98 _H to 003C9F _H	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
003AA0 _H to 003AA7 _H	003CA0 _H to 003CA7 _H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
003AA8 _H to 003AAF _H	003CA8 _H to 003CAF _H	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
003AB0 _H to 003AB7 _H	003CB0 _H to 003CB7 _H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
003AB8 _H to 003ABF _H	003CB8 _H to 003CBF _H	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
003AC0 _H to 003AC7 _H	003CC0 _H to 003CC7 _H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
003AC8 _H to 003ACF _H	003CC8 _H to 003CCF _H	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
003AD0 _H to 003AD7 _H	003CD0 _H to 003CD7 _H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
003AD8 _H to 003ADF _H	003CD8 _H to 003CDF _H	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
003AE0 _H to 003AE7 _H	003CE0 _H to 003CE7 _H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
003AE8 _H to 003AEF _H	003CE8 _H to 003CEF _H	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B
003AF0 _H to 003AF7 _H	003CF0 _H to 003CF7 _H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
003AF8 _H to 003AFF _H	003CF8 _H to 003CFF _H	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

11.3 DC Characteristics

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Input H voltage	V_{IHS}	CMOS hysteresis input pin	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IH}	TTL input pin	—	2.0	—	—	V	
	V_{IHM}	MD input pin	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	
Input L voltage	V_{ILS}	CMOS hysteresis input pin	—	$V_{CC} - 0.3$	—	$0.2 V_{CC}$	V	
	V_{IL}	TTL input pin	—	—	—	0.8	V	
	V_{ILM}	MD input pin	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	
Output H voltage	V_{OH}	All output pins	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -4.0 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	V_{OL}	All output pins	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 4.0 \text{ mA}$	—	—	0.4	V	
Input leak current	I_{IL}	—	$V_{CC} = 5.5 \text{ V}$, $V_{SS} < V_I < V_{CC}$	—5	—	5	μA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, RST	—	25	50	100	$k\Omega$	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	$k\Omega$	Except Flash devices

(Continued)

(Continued)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

Parameter	Sym- bol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Power supply current*	I _{CC}	V _{CC}	Internal frequency : 16 MHz, At normal operating	—	40	55	mA	
			Internal frequency : 16 MHz, At Flash programming/erasing	—	50	70	mA	Flash device
	I _{CCS}		Internal frequency : 16 MHz, At sleep mode	—	12	20	mA	
	I _{CTS}		V _{CC} = 5.0 V ± 10%, Internal frequency : 2 MHz, At pseudo timer mode	—	300	600	μA	
				—	600	1100	μA	MB90F548GL (S) only
				—	200	400	μA	MB90543G(S)/547G(S)/548(S) only
	I _{CCL}		Internal frequency : 8 kHz, At sub operation, T _A = 25 °C	—	400	750	μA	MB90F548GL only
				—	50	100	μA	MASK ROM
				—	150	300	μA	Flash device
	I _{CCLS}		Internal frequency : 8 kHz, At sub sleep, T _A = 25 °C	—	15	40	μA	
	I _{CCT}		Internal frequency : 8 kHz, At timer mode, T _A = 25 °C	—	7	25	μA	
I _{CCH1}	At stop, T _A = 25 °C	—	5	20	μA			
I _{CCH2}	At hardware standby mode, T _A = 25 °C	—	50	100	μA			
Input capacity	C _{IN}	Other than AV _{CC} , AV _{SS} , AVRH, AVRL, C, V _{CC} , V _{SS}	—	5	15	pF		

* : The power supply current testing conditions are when using the external clock.

11.4 AC Characteristics

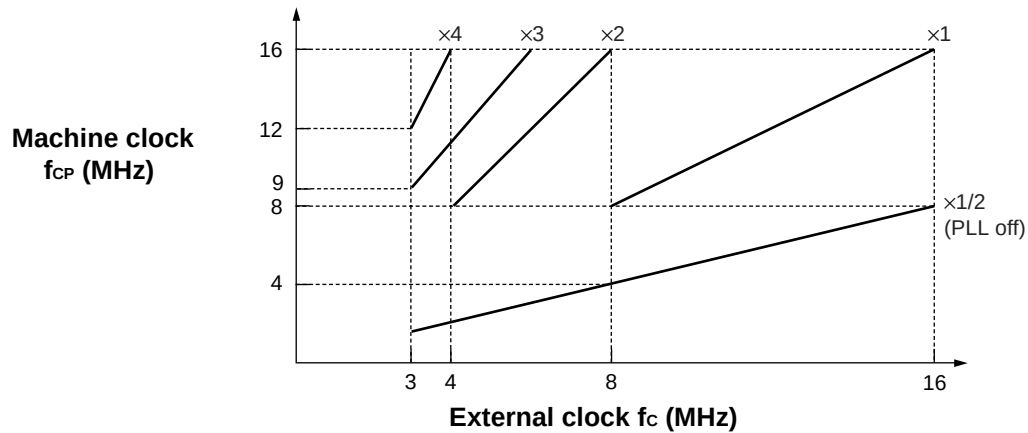
11.4.1 Clock Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Oscillation frequency	f_c	X0, X1	3	—	16	MHz	No multiplier When using an oscillator circuit $V_{CC} = 5.0 \text{ V} \pm 10\%$
			8	—	16	MHz	PLL multiplied by 1 When using an oscillator circuit $V_{CC} = 5.0 \text{ V} \pm 10\%$
			4	—	8	MHz	PLL multiplied by 2 When using an oscillator circuit $V_{CC} = 5.0 \text{ V} \pm 10\%$
			3	—	5.33	MHz	PLL multiplied by 3 When using an oscillator circuit $V_{CC} = 5.0 \text{ V} \pm 10\%$
			3	—	4	MHz	PLL multiplied by 4 When using an oscillator circuit $V_{CC} = 5.0 \text{ V} \pm 10\%$
			3	—	5	MHz	When using an oscillator circuit $V_{CC} < 4.5 \text{ V}$ (MB90F548GL(S)/543G(S)/ 547G(S)/548G(S))
			3	—	16	MHz	No multiplier When using an external clock
			8	—	16	MHz	PLL multiplied by 1 When using an external clock
			4	—	8	MHz	PLL multiplied by 2 When using an external clock
			3	—	5.33	MHz	PLL multiplied by 3 When using an external clock
			3	—	4	MHz	PLL multiplied by 4 When using an external clock
	f_{CL}	X0A, X1A	—	32.768	—	kHz	

(Continued)

■ External clock frequency and Machine clock frequency


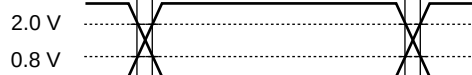
AC characteristics are set to the measured reference voltage values below.

■ Input signal waveform

Hysteresis Input Pin



TTL Input Pin


■ Output signal waveform

Output Pin

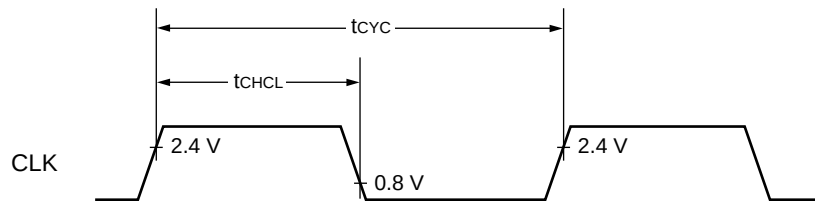


11.4.2 Clock Output Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	$V_{CC} = 5\text{ V} \pm 10\%$	62.5	—	ns	
CLK $\uparrow$ → CLK $\downarrow$	t_{CHCL}			20	—	ns	



11.4.3 Reset and Hardware Standby Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

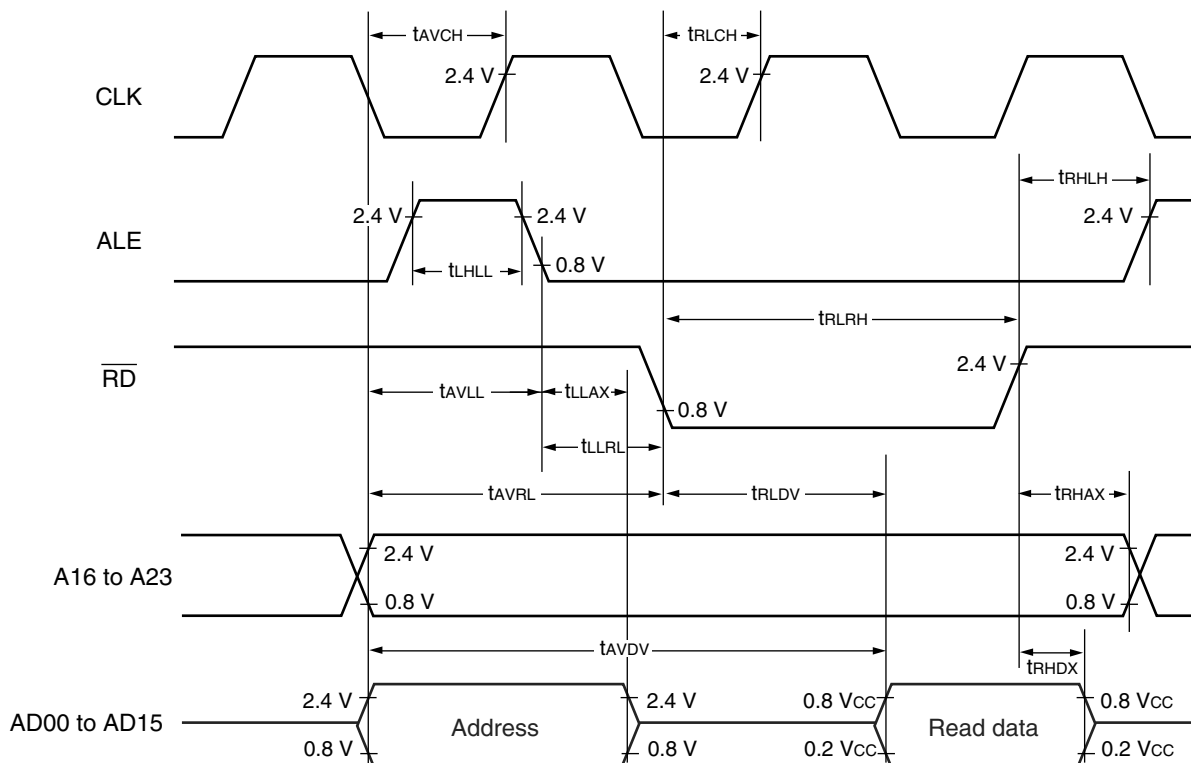
(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value		Units	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	$4\ t_{CP}$	—	ns	Under normal operation
			Oscillation time of oscillator + $4\ t_{CP}$	—	ms	In stop mode
			100	—	μs	In pseudo timer mode (MB90543G (S) /547G (S) /548G (S))
			$4\ t_{CP}$	—	ns	In pseudo timer mode (Other than MB90543G (S) /547G (S) /548G (S))
			$2\ t_{LCP}$	—	μs	In sub-clock mode, sub-sleep mode, timer mode
Hardware standby input time	t_{HSTL}	HST	$4\ t_{CP}$	—	ns	Under normal operation

Note : " t_{cp} " represents one cycle time of the machine clock.

Oscillation time of oscillator is time that amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ns.

Any reset can not fully initialize the Flash Memory if it is performing the automatic algorithm.

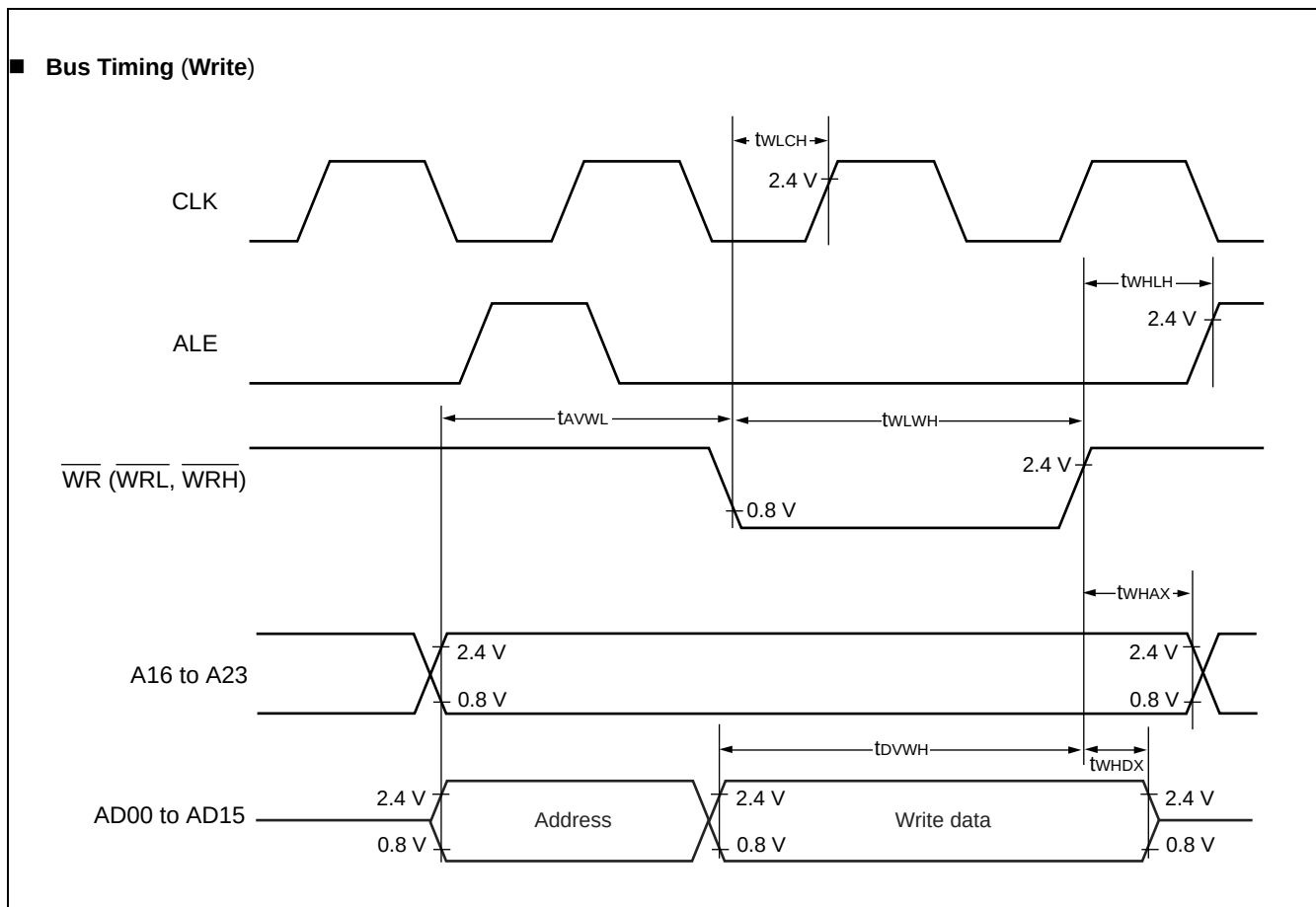
■ Bus Timing (Read)


11.4.6 Bus Timing (Write)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Valid address $\rightarrow \overline{WR}\downarrow$ time	t_{AVWL}	A16 to A23 AD00 to AD15, $\overline{WR}$	—	$t_{CP} - 15$	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	WR		$3 t_{CP}/2 - 20$	—	ns	
Valid data output $\rightarrow \overline{WR}\uparrow$ time	t_{DVWH}	AD00 to AD15, $\overline{WR}$		$3 t_{CP}/2 - 20$	—	ns	
$\overline{WR}\uparrow \rightarrow$ Data hold time	t_{WHDX}	AD00 to AD15, $\overline{WR}$		20	—	ns	
$\overline{WR}\uparrow \rightarrow$ Address valid time	t_{WHAX}	A16 to A23, $\overline{WR}$		$t_{CP}/2 - 10$	—	ns	
$\overline{WR}\uparrow \rightarrow$ ALE $\uparrow$ time	t_{WHLH}	WR, ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{WR}\uparrow \rightarrow$ CLK $\uparrow$ time	t_{WLCH}	WR, CLK		$t_{CP}/2 - 20$	—	ns	

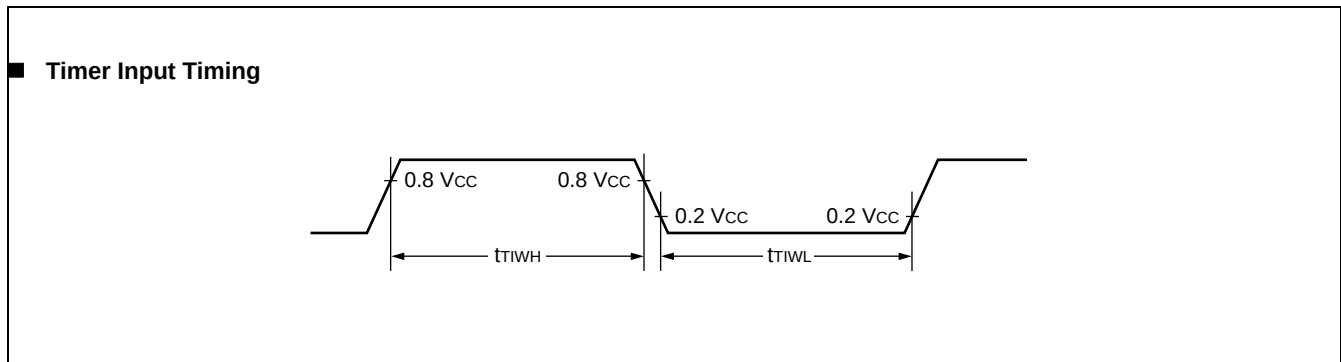


11.4.10 Timer Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	$4\ t_{CP}$	—	ns	
	t_{TIWL}	IN0 to IN7					

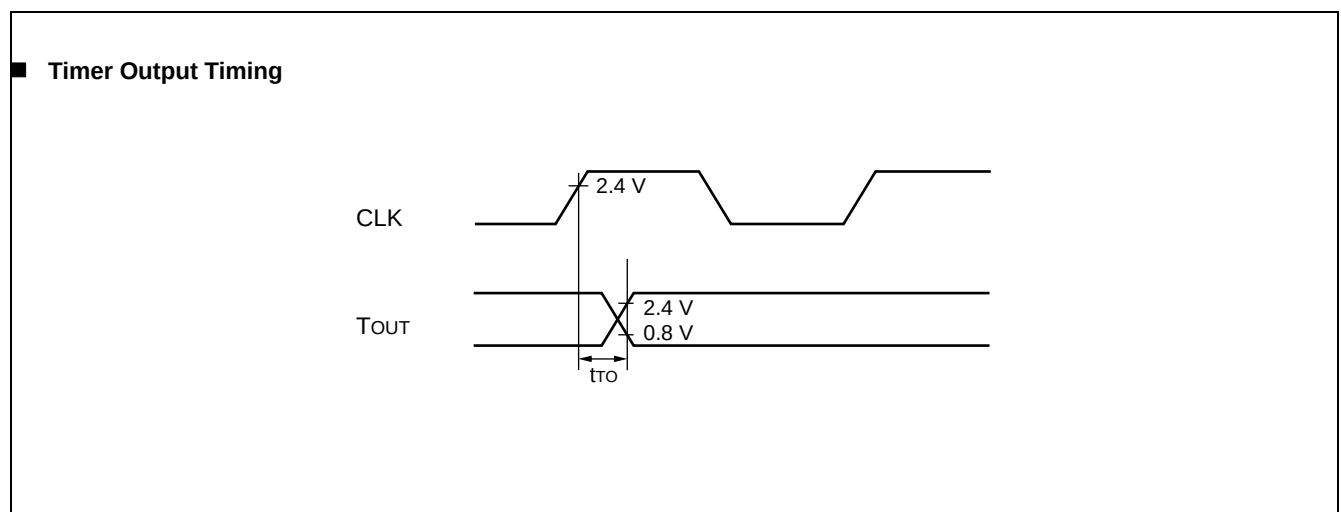


11.4.11 Timer Output Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
CLK $\uparrow$ $\rightarrow$ T _{OUT} change time	t_{TO}	TOT0, TOT1, PPG0 to PPG3	—	30	—	ns	



11.5 A/D Converter

11.5.1 Electrical Characteristics

($V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $3.0 \text{ V} \leq AVR_H - AVR_L$, $T_A = -40 \text{ }^\circ\text{C}$ to $+105 \text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Conversion error	—	—	—	—	± 5.0	LSB	
Nonlinearity error	—	—	—	—	± 2.5	LSB	
Differential nonlinearity error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	$AVRL - 3.5 \text{ LSB}$	$AVRL + 0.5 \text{ LSB}$	$AVRL + 4.5 \text{ LSB}$	V	
Full scale transition voltage	V_{FST}	AN0 to AN7	$AVRH - 6.5 \text{ LSB}$	$AVRH - 1.5 \text{ LSB}$	$AVRH + 1.5 \text{ LSB}$	V	
Compare time	—	—	$352 t_{CP}$	—	—	ns	Internal frequency : 16 MHz
Sampling time	—	—	$64 t_{CP}$	—	—	ns	Internal frequency : 16 MHz
Analog port input current	I_{AIN}	AN0 to AN7	-1	—	1	μA	$V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 1\%$
Analog input voltage range	V_{AIN}	AN0 to AN7	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	$AVRL + 2.7$	—	AV_{CC}	V	
	—	AVRL	0	—	$AVRH - 2.7$	V	
Power supply current	I_A	AV_{CC}	—	5	—	mA	
	I_{AH}	AV_{CC}	—	—	5	μA	*
Reference voltage supply current	I_R	AVRH	—	400	600	μA	Flash device
			—	140	260	μA	MASK ROM
	I_{RH}	AVRH	—	—	5	μA	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

* : When not using an A/D converter, this is the current ($V_{CC} = AV_{CC} = AVR_H = 5.0 \text{ V}$) when the CPU is stopped.

Note: The functionality of the A/D converter is only guaranteed for $V_{CC} = 5.0 \text{ V} \pm 10\%$ (also for MB90543G(S)/547G(S)/548G(S)/F548G(S)/F548GL(S)).