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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f548gspmc-g

Starting by an external trigger input.
Conversion time : 26.3 μs

- FULL-CAN interfaces
  MB90540G series : 2 channels
  MB90545G series : 1 channel
  Conforming to Version 2.0 Part A and Part B
  Flexible message buffering (mailbox and FIFO buffering can be mixed)
- External bus interface : Maximum address space 16 Mbytes
- Package: QFP-100, LQFP-100

1. Product Lineup

Features	MB90F543G (S) /F548G (S) MB90F549G (S) /F546G (S) MB90F548GL(S)	MB90543G (S) MB90547G (S) MB90548G (S) MB90549G (S)	MB90V540G
CPU	F²MC-16LX CPU		
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, 1/2 when PLL stop) Minimum instruction exection time : 62.5 ns (machine clock 16MHz, 4MHz osc. four times multiplied by PLL)		
ROM	Flash memory MB90F543G(S)/F548G(S) / F548GL(S) : 128 Kbytes MB90F549G(S)/F546G(S) : 256 Kbytes	MASK ROM : MB90547G(S): 64 Kbytes MB90543G(S)/548G(S): 128 Kbytes MB90549G(S): 256 Kbytes	External
RAM	MB90F548G(S)/F548GL(S): 4 Kbytes MB90F543G (S) /F549G(S) : 6 Kbytes MB90F546G(S) : 8 Kbytes	MB90547G(S): 2 Kbytes MB90548G(S): 4 Kbytes MB90543G(S)/549G(S): 6 Kbytes	8 Kbytes
Clocks	MB90F543G/F548G/F549G/F546G/F548GL : Two clocks system MB90F543GS/F548GS/F549GS/F546GS/F548GLS : One clock system	MB90543G/547G/548G/549G : Two clocks system MB90543GS/547GS/548GS/549GS : One clock system	Two clocks system*1
Operating voltage range	*3		
Temperature range	−40 °C to 105 °C		
Package	QFP100, LQFP100		PGA-256
Emulator-specify power supply*2	—		None
UART0	Full duplex double buffer Support asynchronous/synchronous (with start/stop bit) transfer Baud rate : 4808/5208/9615/10417/19230/38460/62500/500000 bps (asynchronous) 500 K/1 M/2 Mbps (synchronous) at System clock = 16 MHz		
UART1 (SCI)	Full duplex double buffer Asynchronous (start-stop synchronized) and CLK-synchronous communication Baud rate : 1202/2404/4808/9615/19230/31250/38460/62500 bps (asynchronous) 62.5 K/125 K/250 K/500 K/1 M/2 Mbps (synchronous) at 6, 8, 10, 12, 16 MHz		
Serial I/O	Transfer can be started from MSB or LSB Supports internal clock synchronized transfer and external clock synchronized transfer Supports positive-edge and nagative-edge clock synchronization Baud rate : 31.25 K/62.5 K/125 K/500 K/1 Mbps at System clock = 16 MHz		
A/D Converter	10-bit or 8-bit resolution 8 input channels Conversion time : 26.3 µs (per one channel)		

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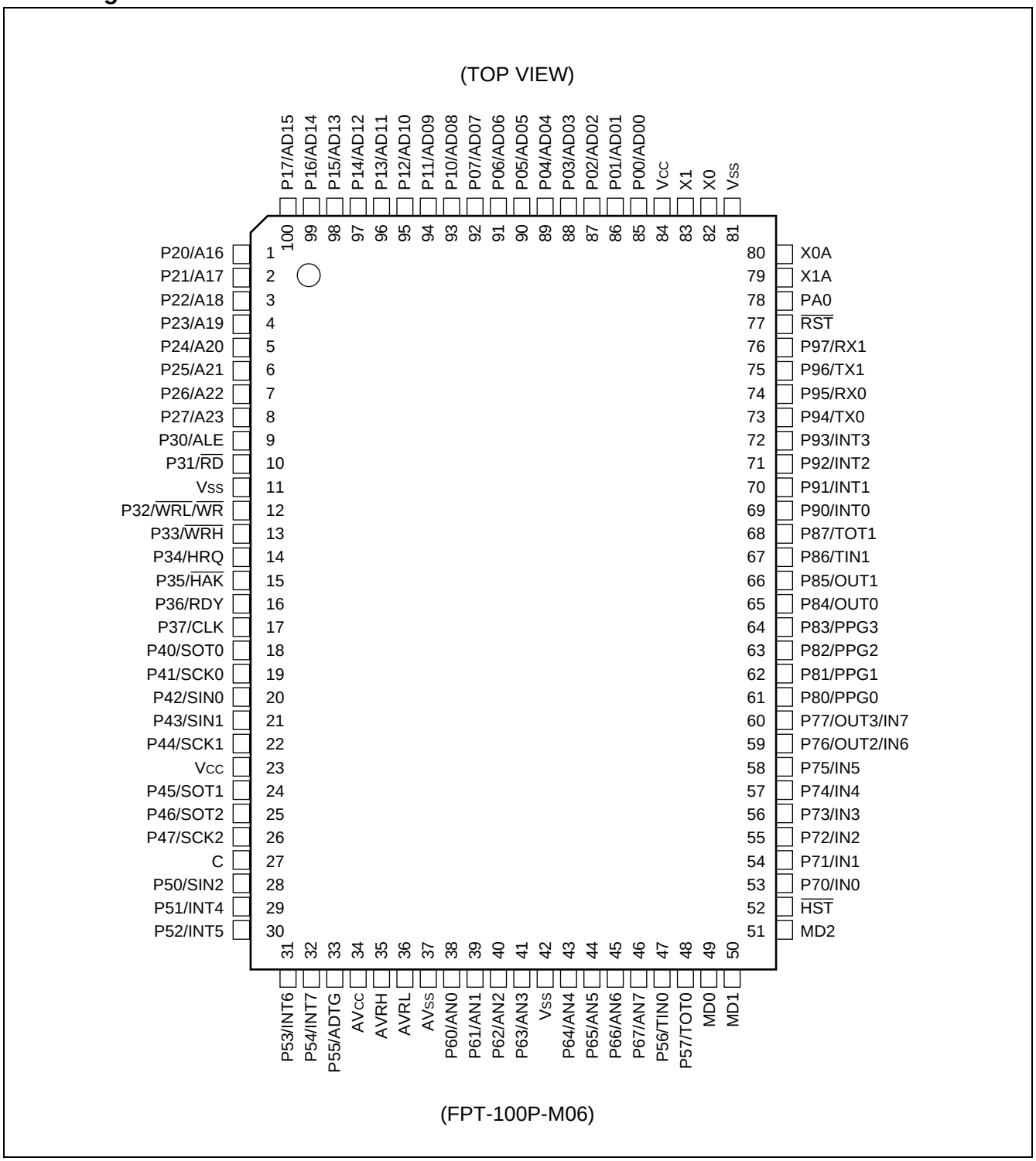
2. Pin Assignment



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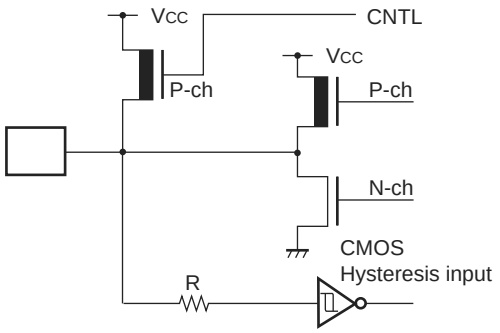
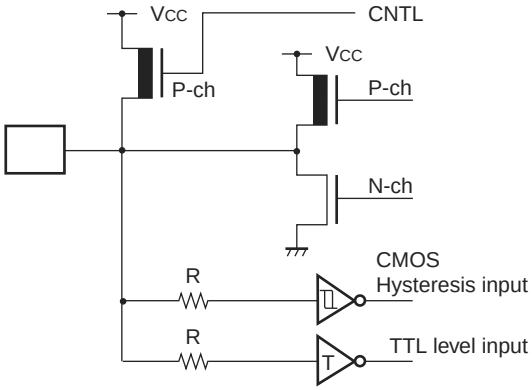
Circuit type	Diagram	Remarks
H		■ CMOS level output ■ CMOS Hysteresis input ■ Programmable pull-up resistor : 50 kΩ approx.
I		■ CMOS level output ■ CMOS Hysteresis input ■ TTL level input (Flash devices in Flash writer mode only) ■ Programmable pullup resistor : 50 kΩ approx.

8. I/O Map

Address	Register	Abbreviation	Access	Resource name	Initial value
00_H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX$_B$
01_H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX$_B$
02_H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX$_B$
03_H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX$_B$
04_H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX$_B$
05_H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX$_B$
06_H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX$_B$
07_H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXX$_B$
08_H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX$_B$
09_H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX$_B$
$0A_H$	Port A data register	PDRA	R/W	Port A	_ _ _ _ _ _ _X$_B$
$0B_H$ to $0F_H$	Reserved				
10_H	Port 0 direction register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0$_B$
11_H	Port 1 direction register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0$_B$
12_H	Port 2 direction register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0$_B$
13_H	Port 3 direction register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0$_B$
14_H	Port 4 direction register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0$_B$
15_H	Port 5 direction register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0$_B$
16_H	Port 6 direction register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0$_B$
17_H	Port 7 direction register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0$_B$
18_H	Port 8 direction register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0$_B$
19_H	Port 9 direction register	DDR9	R/W	Port 9	0 0 0 0 0 0 0 0$_B$
$1A_H$	Port A direction register	DDRA	R/W	Port A	_ _ _ _ _ _ _0$_B$
$1B_H$	Analog Input Enable register	ADER	R/W	Port 6, A/D	1 1 1 1 1 1 1 1$_B$
$1C_H$	Port 0 Pullup control register	PUCR0	R/W	Port 0	0 0 0 0 0 0 0 0$_B$
$1D_H$	Port 1 Pullup control register	PUCR1	R/W	Port 1	0 0 0 0 0 0 0 0$_B$
$1E_H$	Port 2 Pullup control register	PUCR2	R/W	Port 2	0 0 0 0 0 0 0 0$_B$
$1F_H$	Port 3 Pullup control register	PUCR3	R/W	Port 3	0 0 0 0 0 0 0 0$_B$
20_H	Serial Mode Control Register 0	UMC0	R/W	UART0	0 0 0 0 0 1 0 0$_B$
21_H	Serial Status Register 0	USR0	R/W		0 0 0 1 0 0 0 0$_B$
22_H	Serial input data register 0/ Serial output data register 0	UIDR0/UODR0	R/W		XXXXXXXX$_B$
23_H	Rate and data register 0	URD0	R/W		0 0 0 0 0 0 0X$_B$

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Address	Register	Abbreviation	Access	Resource name	Initial value
3900H	Reload L	PRLL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXXB
3901H	Reload H	PRLH0	R/W		XXXXXXXXB
3902H	Reload L	PRLL1	R/W		XXXXXXXXB
3903H	Reload H	PRLH1	R/W		XXXXXXXXB
3904H	Reload L	PRLL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXXB
3905H	Reload H	PRLH2	R/W		XXXXXXXXB
3906H	Reload L	PRLL3	R/W		XXXXXXXXB
3907H	Reload H	PRLH3	R/W		XXXXXXXXB
3908H	Reload L	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXXB
3909H	Reload H	PRLH4	R/W		XXXXXXXXB
390AH	Reload L	PRLL5	R/W		XXXXXXXXB
390BH	Reload H	PRLH5	R/W		XXXXXXXXB
390CH	Reload L	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXXB
390DH	Reload H	PRLH6	R/W		XXXXXXXXB
390EH	Reload L	PRLL7	R/W		XXXXXXXXB
390FH	Reload H	PRLH7	R/W		XXXXXXXXB
3910H to 3917H	Reserved				
3918H	Input Capture Register 0	IPCP0	R	Input Capture 0/1	XXXXXXXXB
3919H	Input Capture Register 0	IPCP0	R		XXXXXXXXB
391AH	Input Capture Register 1	IPCP1	R		XXXXXXXXB
391BH	Input Capture Register 1	IPCP1	R		XXXXXXXXB
391CH	Input Capture Register 2	IPCP2	R	Input Capture 2/3	XXXXXXXXB
391DH	Input Capture Register 2	IPCP2	R		XXXXXXXXB
391EH	Input Capture Register 3	IPCP3	R		XXXXXXXXB
391FH	Input Capture Register 3	IPCP3	R		XXXXXXXXB
3920H	Input Capture Register 4	IPCP4	R	Input Capture 4/5	XXXXXXXXB
3921H	Input Capture Register 4	IPCP4	R		XXXXXXXXB
3922H	Input Capture Register 5	IPCP5	R		XXXXXXXXB
3923H	Input Capture Register 5	IPCP5	R		XXXXXXXXB
3924H	Input Capture Register 6	IPCP6	R	Input Capture 6/7	XXXXXXXXB
3925H	Input Capture Register 6	IPCP6	R		XXXXXXXXB
3926H	Input Capture Register 7	IPCP7	R		XXXXXXXXB
3927H	Input Capture Register 7	IPCP7	R		XXXXXXXXB

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Address	Register	Abbreviation	Access	Resource name	Initial value
3928H	Output Compare Register 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
3929H	Output Compare Register 0	OCCP0	R/W		XXXXXXXXB
392AH	Output Compare Register 1	OCCP1	R/W		XXXXXXXXB
392BH	Output Compare Register 1	OCCP1	R/W		XXXXXXXXB
392CH	Output Compare Register 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXXB
392DH	Output Compare Register 2	OCCP2	R/W		XXXXXXXXB
392EH	Output Compare Register 3	OCCP3	R/W		XXXXXXXXB
392FH	Output Compare Register 3	OCCP3	R/W		XXXXXXXXB
3930H to 39FFH	Reserved				
3A00H to 3AFFH	Reserved for CAN 0 Interface.				
3B00H to 3BFFH	Reserved for CAN 0 Interface.				
3C00H to 3CFFH	Reserved for CAN 1 Interface.				
3D00H to 3DFFH	Reserved for CAN 1 Interface.				
3E00H to 3FFFH	Reserved				

- Read/write notation
  - R/W : Reading and writing permitted
  - R : Read-only
  - W : Write-only

- Initial value notation
  - 0 : Initial value is “0”.
  - 1 : Initial value is “1”.
  - X : Initial value is undefined.
  - _ : Initial value is unused.

Note: Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

List of Message Buffers (DLC Registers and Data Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A60H	003C60H	DLC register 0	DLCR0	R/W	----XXXXB
003A61H	003C61H				
003A62H	003C62H	DLC register 1	DLCR1	R/W	----XXXXB
003A63H	003C63H				
003A64H	003C64H	DLC register 2	DLCR2	R/W	----XXXXB
003A65H	003C65H				
003A66H	003C66H	DLC register 3	DLCR3	R/W	----XXXXB
003A67H	003C67H				
003A68H	003C68H	DLC register 4	DLCR4	R/W	----XXXXB
003A69H	003C69H				
003A6AH	003C6AH	DLC register 5	DLCR5	R/W	----XXXXB
003A6BH	003C6BH				
003A6CH	003C6CH	DLC register 6	DLCR6	R/W	----XXXXB
003A6DH	003C6DH				
003A6EH	003C6EH	DLC register 7	DLCR7	R/W	----XXXXB
003A6FH	003C6FH				
003A70H	003C70H	DLC register 8	DLCR8	R/W	----XXXX
003A71H	003C71H				
003A72H	003C72H	DLC register 9	DLCR9	R/W	----XXXXB
003A73H	003C73H				
003A74H	003C74H	DLC register 10	DLCR10	R/W	----XXXXB
003A75H	003C75H				
003A76H	003C76H	DLC register 11	DLCR11	R/W	----XXXXB
003A77H	003C77H				
003A78H	003C78H	DLC register 12	DLCR12	R/W	----XXXXB
003A79H	003C79H				
003A7AH	003C7AH	DLC register 13	DLCR13	R/W	----XXXXB
003A7BH	003C7BH				
003A7CH	003C7CH	DLC register 14	DLCR14	R/W	----XXXXB
003A7DH	003C7DH				
003A7EH	003C7EH	DLC register 15	DLCR15	R/W	----XXXXB
003A7FH	003C7FH				
003A80H to 003A87H	003C80H to 003C87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB

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10. Interrupt Map

Interrupt cause	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC$_H$	—	—
INT9 instruction	N/A	#09	FFFFD8$_H$	—	—
Exception	N/A	#10	FFFFD4$_H$	—	—
CAN 0 RX	N/A	#11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN 0 TX/NS	N/A	#12	FFFFCC$_H$		
CAN 1 RX	N/A	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 1 TX/NS	N/A	#14	FFFFC4$_H$		
External Interrupt INT0/INT1	*1	#15	FFFFC0$_H$	ICR02	0000B2$_H$
Time Base Timer	N/A	#16	FFFFBC$_H$		
16-bit Reload Timer 0	*1	#17	FFFFB8$_H$	ICR03	0000B3$_H$
8/10-bit A/D Converter	*1	#18	FFFFB4$_H$		
16-bit Free-run Timer	N/A	#19	FFFFB0$_H$	ICR04	0000B4$_H$
External Interrupt INT2/INT3	*1	#20	FFFFAC$_H$		
Serial I/O	*1	#21	FFFFA8$_H$	ICR05	0000B5$_H$
8/16-bit PPG 0/1	N/A	#22	FFFFA4$_H$		
Input Capture 0	*1	#23	FFFFA0$_H$	ICR06	0000B6$_H$
External Interrupt INT4/INT5	*1	#24	FFFF9C$_H$		
Input Capture 1	*1	#25	FFFF98$_H$	ICR07	0000B7$_H$
8/16-bit PPG 2/3	N/A	#26	FFFF94$_H$		
External Interrupt INT6/INT7	*1	#27	FFFF90$_H$	ICR08	0000B8$_H$
Watch Timer	N/A	#28	FFFF8C$_H$		
8/16-bit PPG 4/5	N/A	#29	FFFF88$_H$	ICR09	0000B9$_H$
Input Capture 2/3	*1	#30	FFFF84$_H$		
8/16-bit PPG 6/7	N/A	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 0	*1	#32	FFFF7C$_H$		
Output Compare 1	*1	#33	FFFF78$_H$	ICR11	0000BB$_H$
Input Capture 4/5	*1	#34	FFFF74$_H$		
Output Compare 2/3 - Input Capture 6/7	*1	#35	FFFF70$_H$	ICR12	0000BC$_H$
16-bit Reload Timer 1	*1	#36	FFFF6C$_H$		
UART 0 RX	*2	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 0 TX	*1	#38	FFFF64$_H$		
UART 1 RX	*2	#39	FFFF60$_H$	ICR14	0000BE$_H$
UART 1 TX	*1	#40	FFFF5C$_H$		
Flash Memory	N/A	#41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed interrupt	N/A	#42	FFFF54$_H$		

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*1 : The interrupt request flag is cleared by the EI²OS interrupt clear signal.

*2 : The interrupt request flag is cleared by the EI²OS interrupt clear signal. A stop request is available.

Notes :

- N/A : The interrupt request flag is not cleared by the EI²OS interrupt clear signal.
- For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.
- At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by a hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.
- If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

11.2 Recommended Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value			Units	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.5	5.0	5.5	V	Under normal operation : Other than MB90F548GL(S)/543G(S)/547G(S)/548G(S)
						Under normal operation when A/D conveter is used : MB90F548GL(S)/543G(S)/547G(S)/548G(S)
		3.5	5.0	5.5	V	Under normal operation when A/D conveter is not used : MB90F548GL(S)/543G(S)/547G(S)/548G(S)
		3.0	−	5.5	V	Maintain RAM data in stop mode
Smooth capacitor	C_S	0.022	0.1	1.0	µF	*
Operating temperature	T_A	−40	−	+105	°C	

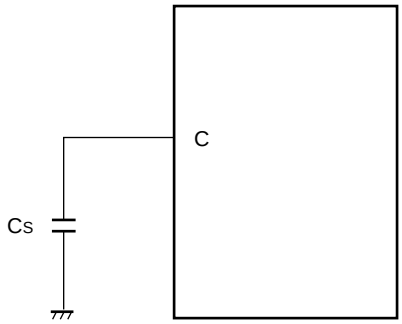
*: Use a ceramic capacitor or a capacitor of better 4. AC characteristics. The bypass capacitor should be greater than this capacitor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ **C Pin Connection Diagram**



11.3 DC Characteristics

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Input H voltage	V_{IHS}	CMOS hysteresis input pin	−	0.8 V_{CC}	−	V_{CC} + 0.3	V	
	V_{IH}	TTL input pin	−	2.0	−	−	V	
	V_{IHM}	MD input pin	−	V_{CC} − 0.3	−	V_{CC} + 0.3	V	
Input L voltage	V_{ILS}	CMOS hysteresis input pin	−	V_{CC} − 0.3	−	0.2 V_{CC}	V	
	V_{IL}	TTL input pin	−	−	−	0.8	V	
	V_{ILM}	MD input pin	−	V_{SS} − 0.3	−	V_{SS} + 0.3	V	
Output H voltage	V_{OH}	All output pins	V_{CC} = 4.5 V, I_{OH} = −4.0 mA	V_{CC} − 0.5	−	−	V	
Output L voltage	V_{OL}	All output pins	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	−	−	0.4	V	
Input leak current	I_{IL}	−	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	−5	−	5	µA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, RST	−	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	−	25	50	100	kΩ	Except Flash devices

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(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Power supply current*	I_{CC}	V_{CC}	Internal frequency : 16 MHz, At normal operating	—	40	55	mA	
			Internal frequency : 16 MHz, At Flash programming/erasing	—	50	70	mA	Flash device
	I_{CCS}		Internal frequency : 16 MHz, At sleep mode	—	12	20	mA	
	I_{CTS}		V_{CC} = 5.0 V ± 10%, Internal frequency : 2 MHz, At pseudo timer mode	—	300	600	µA	
				—	600	1100	µA	MB90F548GL (S) only
				—	200	400	µA	MB90543G(S)/547G(S)/548(S) only
	I_{CCL}		Internal frequency : 8 kHz, At sub operation, T_A = 25 °C	—	400	750	µA	MB90F548GL only
				—	50	100	µA	MASK ROM
				—	150	300	µA	Flash device
	I_{CCLS}		Internal frequency : 8 kHz, At sub sleep, T_A = 25 °C	—	15	40	µA	
	I_{CCT}		Internal frequency : 8 kHz, At timer mode, T_A = 25 °C	—	7	25	µA	
	I_{CCH1}		At stop, T_A = 25 °C	—	5	20	µA	
	I_{CCH2}		At hardware standby mode, T_A = 25 °C	—	50	100	µA	
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVRH, AVRL, C, V_{CC}, V_{SS}	—	—	5	15	pF	

* : The power supply current testing conditions are when using the external clock.

(Continued)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

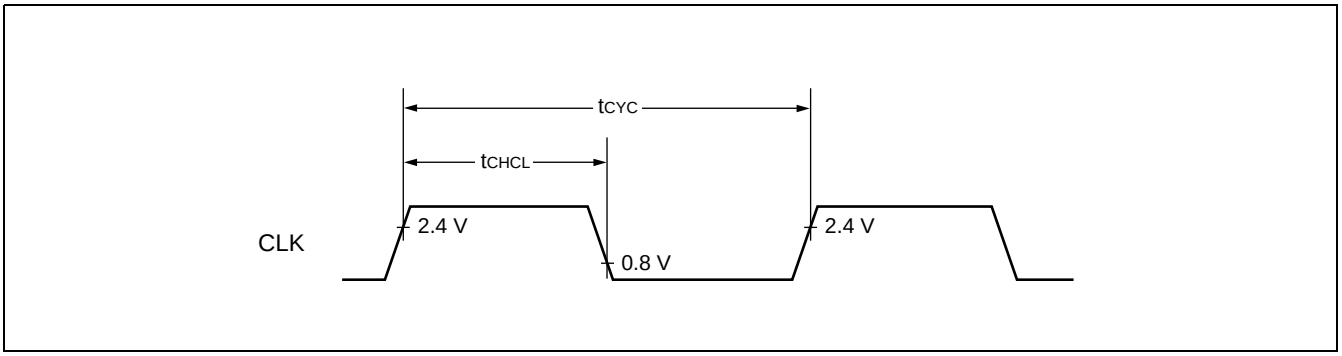
Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	No multiplier When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			62.5	—	125	ns	PLL multiplied by 1 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			125	—	250	ns	PLL multiplied by 2 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			187.5	—	333	ns	PLL multiplied by 3 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			250	—	333	ns	PLL multiplied by 4 When using an oscillator circuit V_{CC} = 5.0 V ± 10%
			200	—	333	ns	When using an oscillator circuit V_{CC} < 4.5 V(MB90F548GL(S)/543G(S)/547G(S)/548G(S))
			62.5	—	333	ns	No multiplier When using an external clock
			62.5	—	125	ns	PLL multiplied by 1 When using an external clock
			125	—	250	ns	PLL multiplied by 2 When using an external clock
			187.5	—	333	ns	PLL multiplied by 3 When using an external clock
			250	—	333	ns	PLL multiplied by 4 When using an external clock
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WLH}, P_{WLL}	X0A	—	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using an external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	When using main clock
	f_{LCP}	—	—	8.192	—	kHz	When using sub-clock
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	When using main clock
	t_{LCP}	—	—	122.1	—	µs	When using sub-clock

11.4.2 Clock Output Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	V_{CC} = 5 V ± 10%	62.5	—	ns	
CLK↑ → CLK↓	t_{CHCL}			20	—	ns	



11.4.3 Reset and Hardware Standby Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Value		Units	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	4 t_{CP}	—	ns	Under normal operation
			Oscillation time of oscillator + 4 t_{CP}	—	ms	In stop mode
			100	—	µs	In pseudo timer mode (MB90543G (S) /547G (S) /548G (S))
			4 t_{CP}	—	ns	In pseudo timer mode (Other than MB90543G (S) /547G (S) /548G (S))
			2 t_{LCP}	—	µs	In sub-clock mode, sub-sleep mode, timer mode
Hardware standby input time	t_{HSTL}	$\overline{HST}$	4 t_{CP}	—	ns	Under normal operation

Note : "t_{cp}" represents one cycle time of the machine clock.

Oscillation time of oscillator is time that amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between handreds of µs to several ms. In the external clock, the oscillation time is 0 ns.

Any reset can not fully initialize the Flash Memory if it is performing the automatic algorithm.

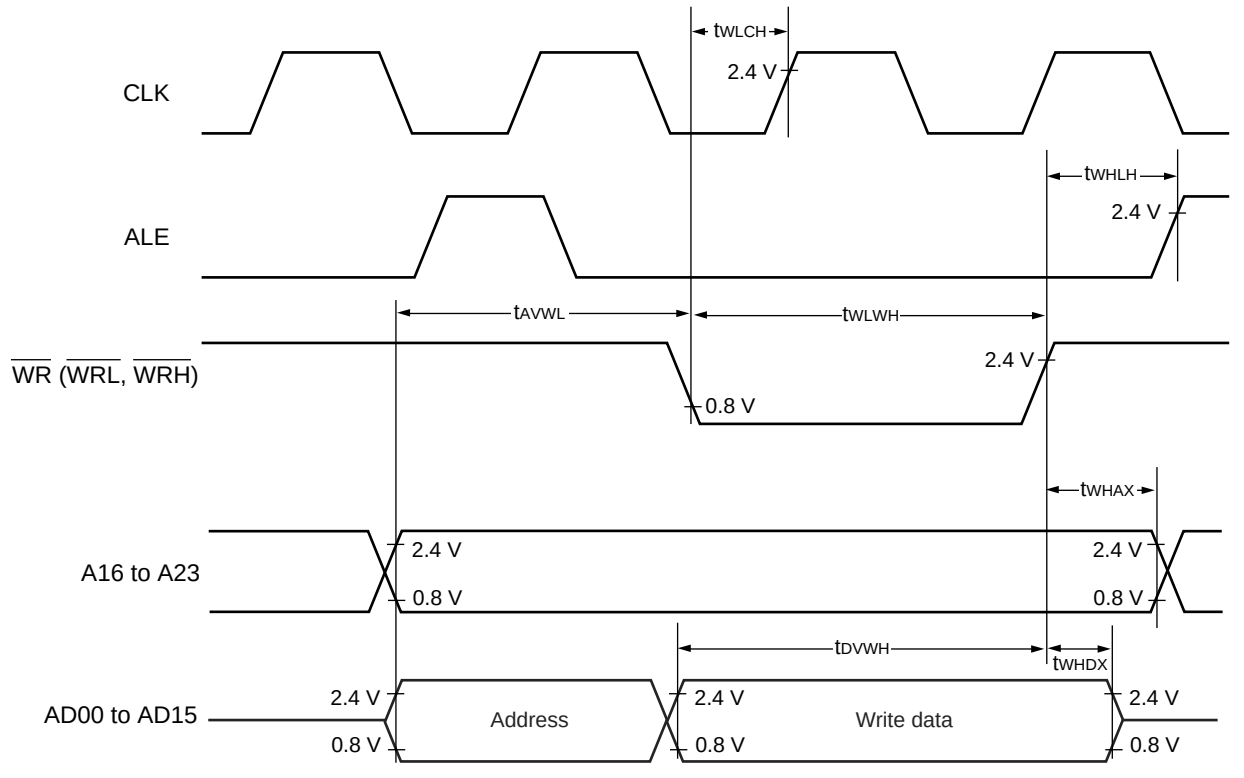
11.4.6 Bus Timing (Write)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Valid address → $\overline{WR}$↓ time	t_{AVWL}	A16 to A23 AD00 to AD15, $\overline{WR}$	—	t_{CP} − 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	WR		3 t_{CP}/2 − 20	—	ns	
Valid data output → $\overline{WR}$↑ time	t_{DVWH}	AD00 to AD15, $\overline{WR}$		3 t_{CP}/2 − 20	—	ns	
$\overline{WR}$↑ → Data hold time	t_{WHDX}	AD00 to AD15, $\overline{WR}$		20	—	ns	
$\overline{WR}$↑ → Address valid time	t_{WHAX}	A16 to A23, $\overline{WR}$		t_{CP}/2 − 10	—	ns	
$\overline{WR}$↑ → ALE↑ time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 − 15	—	ns	
$\overline{WR}$↑ → CLK↑ time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 − 20	—	ns	

■ **Bus Timing** (**Write**)



11.4.7 Ready Input Timing

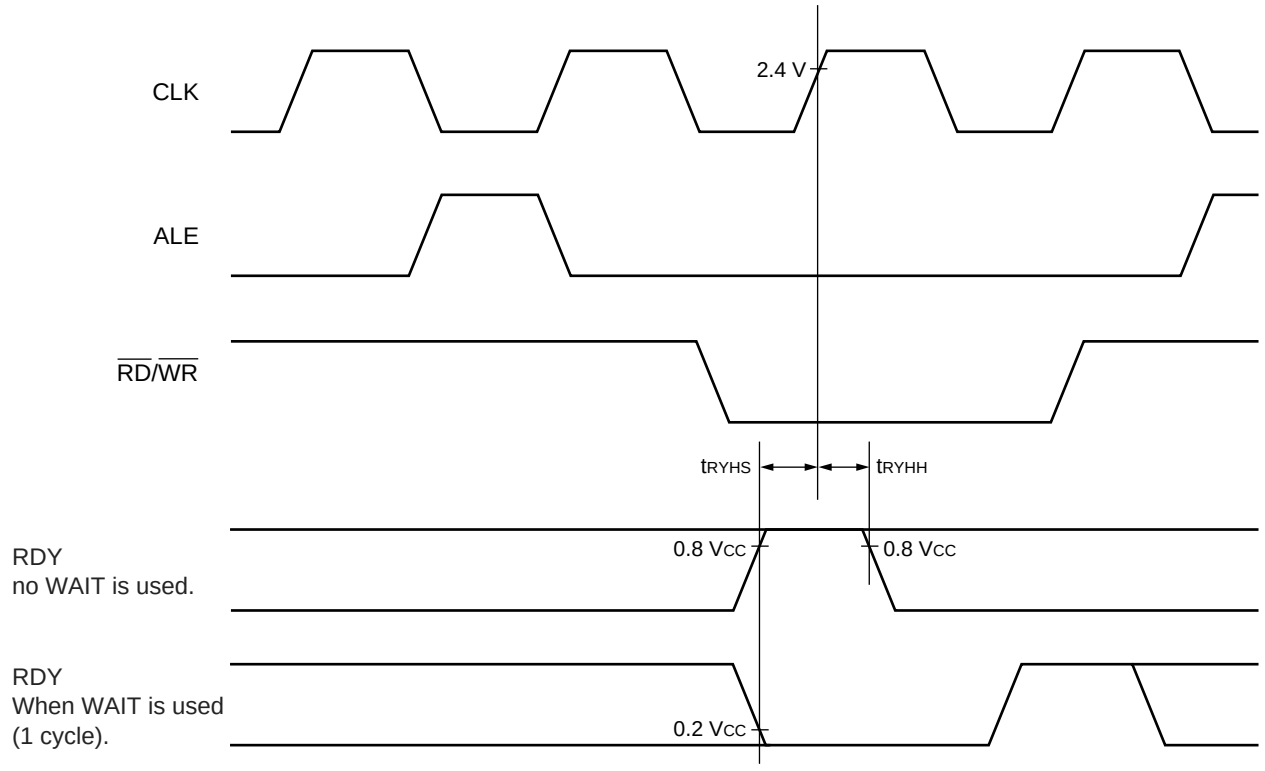
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.

■ **Ready Input Timing**



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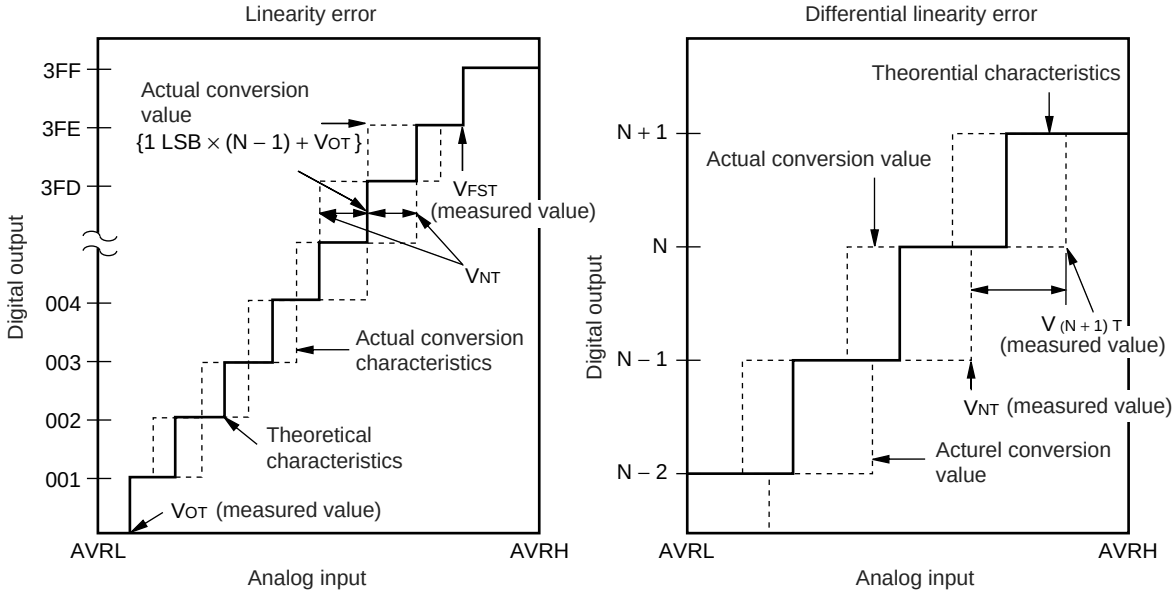


$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage at transition of digital output from "000_H" to "001_H"
V_{FST} : Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

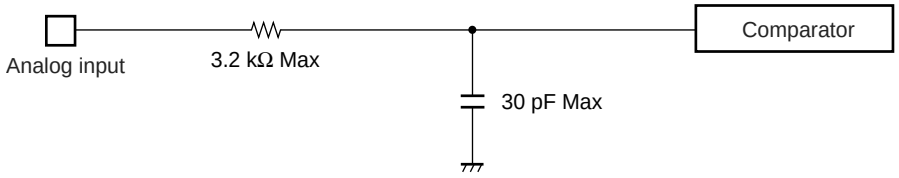
11.5.3 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions, :

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

Note : When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz) .

■ **Equipment of analog input circuit model**



11.5.4 Error

The smaller the | AVRH − AVRL |, the greater the error would become relatively.

11.6 Flash Memory Program/Erase Characteristics

Parameter	Condition	Value			Units	Remarks	
		Min	Typ	Max			
Sector erase time	T_A = + 25 °C V_{CC} = 5.0 V	—	1	15	s	Excludes 00H programming prior erasure	
Chip erase time		—	5	—	s	MB90F543G (S) /F548G (S) /F548GL (S)	Excludes 00H programming prior erasure
			7	—	s	MB90F549G (S) /F546G (S)	
Word (16 bit width) programming time		—	16	3,600	µs	Excludes system-level overhead	
Erase/Program cycle	—	10,000	—	—	cycle		

■ Power supply current (MB90549G)