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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	<u>.</u>
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f548gspmc-gs

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Starting by an external trigger input. Conversion time : 26.3 μ s

FULL-CAN interfaces
 MB90540G series : 2 channels
 MB90545G series : 1 channel
 Conforming to Version 2.0 Part A and Part B

Flexible message buffering (mailbox and FIFO buffering can be mixed)

- External bus interface : Maximum address space 16 Mbytes
- Package: QFP-100, LQFP-100



3. Pin Description

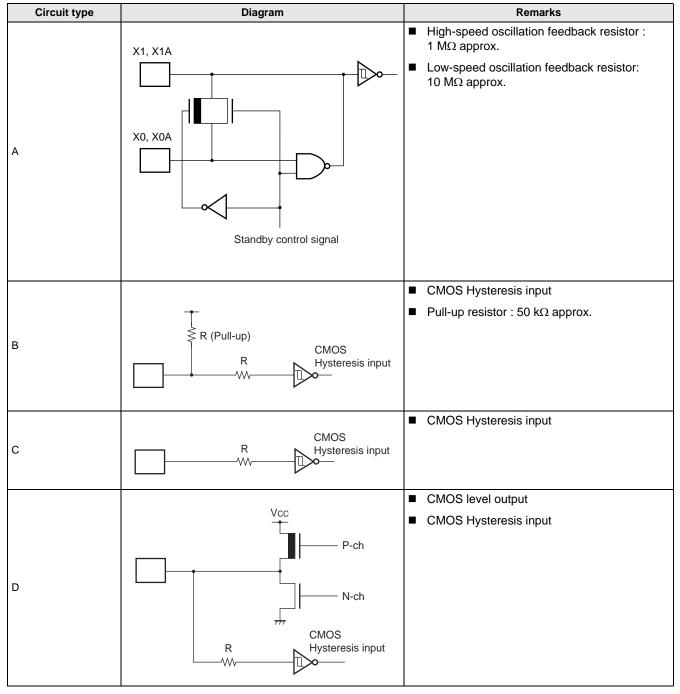
Pin No.		Diaman	0:	Function					
LQFP*2	QFP ^{∗1}	Pin name	Circuit type	Function					
80 81	82 83	X0 X1	A (Oscillation)	High speed crystal oscillator input pins					
78	80	X0A	А	Low speed crystal oscillator input pins. For the one clock system parts, perfom external pull-down processing.					
77	79	X1A	(Oscillation)	Low speed crystal oscillator input pins. For the one clock system parts, leave it open.					
75	77	RST	В	External reset request input pin					
50	52	HST	С	Hardware standby input pin					
00.45.00	05 40 00	P00 to P07		General I/O port with programmable pullup. This function is enabled in the single-chip mode.					
83 to 90	85 to 92	AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.					
	91 to 98 93 to 100 P10 to P17 AD08 to AD15			General I/O port with programmable pullup. This function is enabled in th single-chip mode.					
91 to 98				I/O pins for 8 higher bits of the external address/data bus. This function is enabled when the external bus is enabled.					
00.1-0	4 1 2	P20 to P27		General I/O port with programmable pullup. In external bus mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to "1".					
99 to 6	1 to 8	A16 to A23		8-bit I/O pins for A16 to A23 at the external address/data bus. In external but mode, this function is valid when the corresponding bits in the external address output control resister (HACR) are set to "0".					
7		P30		General I/O port with programmable pullup. This function is enabled in the single-chip mode.					
7	9	ALE		Address latch enable output pin. This function is enabled when the externa bus is enabled.					
0	10	P31		General I/O port with programmable pullup. This function is enabled in the single-chip mode.					
8	10	RD		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.					
		P32		General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the WR/WRL pin output is disabled.					
10	12	WRL WR	1	Write strobe output pin for the data bus. This function is enabled when bot the external bus and the \overline{WR}/WRL pin output are enabled. \overline{WRL} is write-strobe output pin for the lower 8 bits of the data bus in 16-bit access. \overline{WR} write-strobe output pin for the 8 bits of the data bus in 8-bit access.					



Pin	No.	Pin name	Circuit type	Function				
LQFP*2	QFP ^{∗1}	i in name	Circuit type	i unction				
46	48	P57	D	General I/O port. This function is enabled when the 16-bit reload timers 0 disables the output.				
40	40	тото		Output pin for the 16-bit reload timers 0. This function is enabled when the 16-bit reload timers 0 enables the output.				
		P70 to P75		General I/O ports. This function is always enabled.				
51 to 56	53 to 58	IN0 to IN5	D	Trigger input pins for input captures ICU0 to ICU5. Set the corresponding Port Direction Register to input if this function is used.				
		P76 , P77		General I/O ports. This function is enabled when the OCU disables the waveform output.				
57 , 58	59 , 60	OUT2 , OUT3	D	Event output pins for output compares OCU2 and OCU3. This function is enabled when the OCU enables the waveform output.				
		IN6 , IN7		Trigger input pins for input captures ICU6 and ICU7. Set the corresponding Port Direction Register to input and disable the OCU waveform output if this function is used.				
59 to 62	P80 to P83		D	General I/O ports. This function is enabled when 8/16-bit PPG disables the waveform output.				
59 10 62 61 10 64		PPG0 to PPG3		Output pins for 8/16-bit PPGs. This function is enabled when 8/16-bit PPG enables the waveform output.				
63,64	65,66	P84 , P85	D	General I/O ports. This function is enabled when the OCU disables the waveform output.				
03,04	05,00	OUT0 , OUT1		Waveform output pins for output compares OCU0 and OCU1. This function enabled when the OCU enables the waveform output.				
		P86		General I/O port. This function is always enabled.				
65	67	TIN1	D	Input pin for the 16-bit reload timers 1. Set the corresponding Port Direction Register to input if this function is used.				
66	68	P87	D	General I/O port. This function is enabled when the 16-bit reload timers 1 disables the output.				
00	00	TOT1		Output pin for the 16-bit reload timers 1. This function is enabled when the 16- bit reload timers 1 enables the output.				
		P90 to P93		General I/O port. This function is always enabled.				
67 to 70	69 to 72	INT0 to INT3	D	External interrupt request input pins for INT0 to INT3. Set the corresponding Port Direction Register to input if this function is used.				
		P94		General I/O port. This function is enabled when CAN0 disables the output.				
71	73	ТХО	D	TX output pin for CAN0. This function is enabled when CAN0 enables the output.				



4. I/O Circuit Type





(Continued)

Circuit type	Diagram	Remarks
		CMOS level output
		 CMOS Hysteresis input
н	Vcc Vcc P-ch P-ch N-ch m CMOS Hysteresis input	 Programmable pull-up resistor : 50 kΩ approx.
		CMOS level output
		 CMOS Hysteresis input
		 TTL level input (Flash devices in Flash writer mode only)
	P-ch	 Programmable pullup resistor : 50 kΩ approx.
1	N-ch	
	R R Hysteresis input	
	TTL level input	





5. Handling Devices

(1) Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than Vcc or lower than Vss is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between Vcc and Vss.

■ The AVcc power supply is applied before the Vcc voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, care must also be taken in not allowing the analog power-supply voltage (AVcc, AVRH) to exceed the digital power-supply voltage.

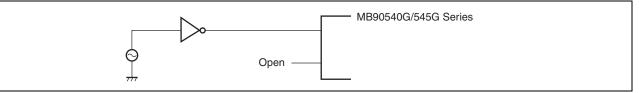
(2) Handling unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefor they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 k Ω .

Unused bi-directional pins should be set to the output state and can be left open, or the input state with the above described connection.

(3) Using external clock

To use external clock, drive X0 pin only and leave X1 pin unconnected. Below is a diagram of how to use external clock.



(4) Use of the sub-clock

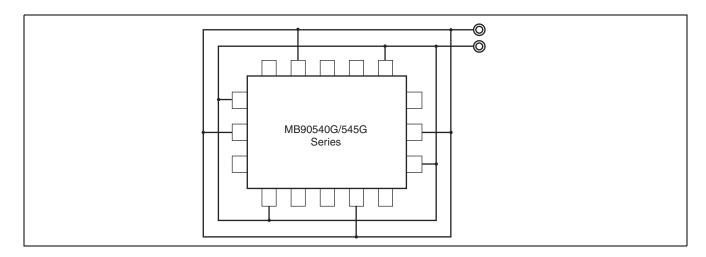
Use one clock system parts when the sub-clock is not used. In that case, pull-down the pin X0A and leave the pin X1A open. When using two clock system parts, a 32 kHz oscillator has to be connected to the X0A and X1A pins.

(5) Power supply pins (Vcc/Vss)

In products with multiple V_{cc} or V_{ss} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to an external power and a ground line to lower the electromagnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect Vcc and Vss pins via the lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 µF between Vcc and Vss pins near the device.



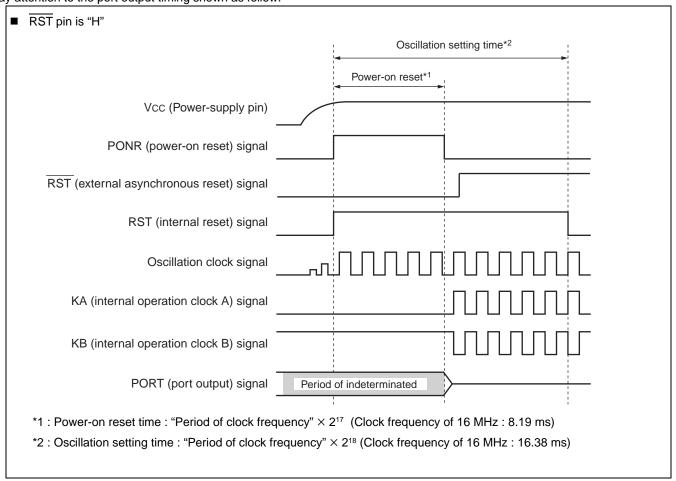


(12) Indeterminate outputs from ports 0 and 1 (MB90V540G only)

During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

■ If RST pin is "H", the outputs become indeterminate.

■ If RST pin is "L", the outputs become high-impedance. Pay attention to the port output timing shown as follow.





9. CAN Controller

The MB90540G series contains two CAN controllers (CAN0 and CAN1), the MB90545G series contains only one (CAN0). The Evaluation Chip MB90V540G also has two CAN controllers.

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
 - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
 - □ 29-bit ID and 8-byte data
 - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
 - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 1 Mbps (when input clock is at 16 MHz)

List of Control Registers

Address		Register	Abbreviation	Access	Initial Value	
CAN0	CAN1	Kegiatei	Abbieviation	ALLESS	initial value	
000070н	000080н	Message buffer valid register	BVALR	R/W	00000000 00000000в	
000071н	000081 н	Nessage builet valid register	DVALK	N/ W	0000000 000000B	
000072н	000082н	Transmit request register	TREOR	R/W	0000000 0000000	
000073н	000083н		IREQR	r//v		
000074н	000084н	Transmit cancel register	TCANR	w	00000000 00000000в	
000075н	000085н		ICANK	vv	0000000 000000B	
000076н	000086н	Transmit complete register	TCR	R/W	0000000 00000000	
000077н	000087н		ICK	r/vv		
000078н	000088н	Receive complete register	RCR	R/W	00000000 00000000в	
000079н	000089н	Receive complete register	RCR	r/vv		
00007Ан	00008Ан	Remote request receiving register	RRTRR	R/W	0000000 0000000в	
00007Bн	00008Bн	Remote request receiving register		N/ W	0000000 000000B	
00007Cн	00008Сн		ROVRR	R/W	00000000 00000000в	
00007Dн	00008Dн	Receive overrun register	ROVER	r/vv		
00007Eн	00008Eн	Receive interrupt enable register	RIER	R/W	00000000 00000000B	
00007Fн	00008Fн	Receive interrupt enable register		IN/ VV	0000000 0000000B	



(Continued)

Address		Desister	Abbroviation	A	Initial Value	
CAN0	CAN1	Register Abbreviation Access		initiai value		
003В00н	003D00н	- Control status register	CSR	R/W, R	00000 00-1в	
003B01н	003D01н		CSK	K/VV, K	00000 00-1в	
003В02н	003D02н	Lest quest indicator register	LEIR	R/W	000-000в	
003В03н	003D03н	Last event indicator register	LEIR	K/ VV	000-000B	
003В04н	003D04н	Receive/transmit error counter register	RTEC	R	0000000 0000000в	
003В05н	003D05н	- Receive/transmit error counter register	RIEC	ĸ		
003В06н	003D06н	Pit timing register	BTR	R/W	-1111111 1111111в	
003В07н	003D07н	Bit timing register	DIK	R/VV	-1111111 11111118	
003В08н	003D08н		IDER	R/W		
003В09н	003D09н	IDE register	IDER	R/W	XXXXXXXX XXXXXXXB	
003В0Ан	003D0AH		register TRTRR R/W		0000000 0000000в	
003В0Вн	003D0BH	 Transmit RTR register 		R/VV	0000000 000000B	
003В0Сн	003D0CH	Demote from a receive weiting register	RFWTR	R/W		
003B0DH	003D0DH	- Remote frame receive waiting register		R/W	XXXXXXXX XXXXXXXXB	
003В0Ен	003D0Eн	Transmit request enable register	TIER	R/W	0000000 0000000в	
003B0Fн	003D0Fн	- Transmit request enable register	HER	K/VV	0000000 000000B	
003B10н	003D10н				XXXXXXXX XXXXXXXxx	
003B11н	003D11н		AMSR	SR R/W	~~~~~~	
003B12н	003D12н	Acceptance mask select register	AWSR		XXXXXXXX XXXXXXXxx	
003B13н	003D13н				^^^^^	
003B14н	003D14н					
003B15н	003D15н	Assentance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXXB	
003B16н	003D16н	Acceptance mask register 0	AWKU	K/VV	XXXXX XXXXXXXXB	
003B17н	003D17н	7			^^^^^	
003B18н	003D18н					
003B19н	003D19⊦	Acceptopop mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXXB	
003В1Ан	003D1Aн	Acceptance mask register 1		17/10	XXXXX XXXXXXXxB	
003B1Bн	003D1BH				~~~~~ ~~~~~	

List of Message Buffers (ID Registers)

Address		Pagistar	Abbreviation	A	Initial Value	
CAN0	CAN1	Register	Appreviation	Access	initial value	
003A00н to 003A1Fн	003C00н to 003C1Fн	General-purpose RAM	_	R/W	XXXXXXXXB to XXXXXXXB	
003А20н	003C20н				XXXXXXXX XXXXXXXxx	
003A21н	003C21н	ID register 0	IDR0	R/W	~~~~~~	
003А22н	003С22н		IDRO	r./ v v	XXXXX XXXXXXXXB	
003А23н	003С23н				~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	



Address		Register	Abbreviation	A	Initial Value	
CAN0	CAN1	Keyistei	Abbreviation Access			
003А24н	003C24 _H				XXXXXXXX XXXXXXXX	
003A25н	003C25н	ID register 1	IDR1	R/W	^^^^^	
003A26н	003C26н			1.1/ 1.1	XXXXX XXXXXXXB	
003A27н	003C27н					
003A28н	003C28н				XXXXXXXX XXXXXXXB	
003A29н	003C29н	ID register 2	IDR2	R/W		
003А2Ан	003C2Ан			1.1/ 1.1	XXXXX XXXXXXXB	
003A2Bн	003C2Bн				~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	
003А2Сн	003С2Сн				XXXXXXXX XXXXXXXB	
003A2Dн	003C2Dн	ID register 3	IDR3	R/W		
003А2Ен	003C2Eн			1.1/ 1.1	XXXXX XXXXXXXB	
003A2Fн	003C2Fн					
003А30н	003C30н				XXXXXXXX XXXXXXXB	
003A31н	003C31н	ID register 4	IDR4	R/W		
003А32н	003С32н				XXXXX XXXXXXXB	
003А33н	003С33н					
003А34н	003C34н				XXXXXXXX XXXXXXXxx	
003А35 н	003C35н	ID register 5	IDR5	R/W		
003А36н	003C36н			1.7, 4.4	XXXXX XXXXXXXXB	
003А37н	003C37н					
003А38н	003C38н				XXXXXXXX XXXXXXXXB	
003А39н	003С39н	ID register 6	IDR6	R/W		
003АЗАн	003С3Ан			11/11	XXXXX XXXXXXXXB	
003А3Вн	003C3BH					





(Continued)

*1 : The interrupt request flag is cleared by the EI2OS interrupt clear signal.

*2 : The interrupt request flag is cleared by the El²OS interrupt clear signal. A stop request is available.

Notes :

- N/A : The interrupt request flag is not cleared by the EI²OS interrupt clear signal.
- For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the El²OS interrupt clear signal.
- At the end of El²OS, the El²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the El²OS and in the meantime another interrupt flag is set by a hardware event, the later event is lost because the flag is cleared by the El²OS clear signal caused by the first event. So it is recommended not to use the El²OS for this interrupt number.
- If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.





11. Electrical Characteristics

11.1 Absolute Maximum Ratings

 $(V_{SS} = AV_{SS} = 0.0 V)$

Parameter	Symbol	Value		Units	Remarks
Farameter	Symbol	Min	Max	Units	Remarks
	Vcc	Vss - 0.3	Vss + 6.0	V	
Power supply voltage	AVcc	Vss - 0.3	Vss + 6.0	V	Vcc = AVcc *1
	AVRH, AVRL	V _{SS} - 0.3	Vss + 6.0	V	AVcc≥AVRH/AVRL, AVRH≥ AVRL *1
Input voltage	Vi	$V_{SS} - 0.3$	Vss + 6.0	V	*2
Output voltage	Vo	$V_{SS} = 0.3$	Vss + 6.0	V	*2
Maximum clamp current		- 2.0	+ 2.0	mA	*6
Total maximum clamp current	Σ Iclamp	-	20	mA	*6
"L" level max output current	lol	-	15	mA	*3
"L" level avg. output current	OLAV	-	4	mA	*4
"L" level max overall output current	ΣΙοι	-	100	mA	
"L" level avg. overall output current	Σ Iolav	-	50	mA	*5
"H" level max output current	Іон	-	-15	mA	*3
"H" level avg. output current	Іонач	-	-4	mA	*4
"H" level max overall output current	ΣІон	-	-100	mA	
"H" level avg. overall output current	ΣΙοήαν	-	-50	mA	*5
Dower concurration	Pp	-	500	mW	Flash device
Power consumption	ΓD	—	400	mW	MASK ROM
Operating temperature	TA	-40	+105	°C	
Storage temperature	Тѕтс	-55	+150	°C	

*1 : AVcc, AVRH, AVRL should not exceed Vcc. Also, AVRH, AVRL should not exceed AVcc, and AVRL does not exceed AVRH.

- *2 : VI and Vo should not exceed Vcc + 0.3 V. However if the maximum current to/from an input is limited by some means with external components, the IcLAMP rating supercedes the VI rating.
- *3 : The maximum output current is a peak value for a corresponding pin.
- *4 : Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5 : Total average current is an average current value observed for a 100 ms period for all corresponding pins.

*6 :

- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0
- Use within recommended operating conditions.
- □ Use at DC voltage (current) .
- □ The + B signal should always be applied with a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the + B input potential may pass through the protective diode and increase the potential at the Vcc pin, and this may affect other devices.
- Note that if a + B signal is input when the microcontroller current is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- □ Care must be taken not to leave the + B input pin open.

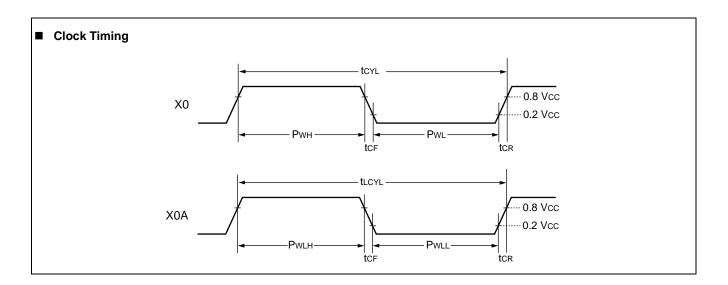


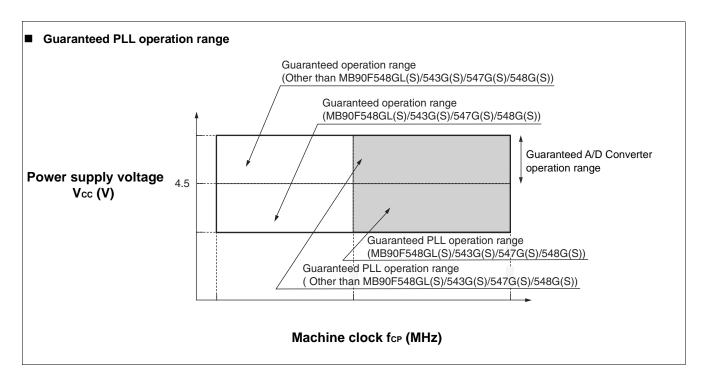
11.3 DC Characteristics

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V \text{ to } 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ }^{\circ}\text{C} \text{ to } +105 \text{ }^{\circ}\text{C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ }^{\circ}\text{C} \text{ to } +105 \text{ }^{\circ}\text{C})

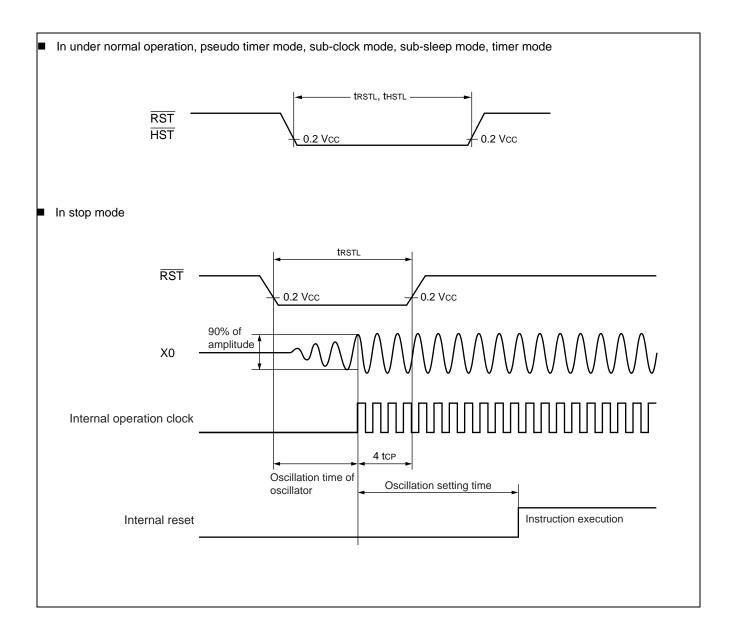
Doromotor	Symbol	Pin name	Condition		Value	Units	Remarks	
Parameter	Symbol	Fin name	Condition	Min	Тур	Max	Units	Remarks
Input H	VIHS	CMOS hysteresis input pin	-	0.8 Vcc	_	Vcc + 0.3	v	
voltage	Vін	TTL input pin	-	2.0	—	—	V	
voltage Input L voltage Output H voltage Output L voltage Input leak current Pull-up resistance	VIHM	MD input pin	-	Vcc - 0.3	—	Vcc + 0.3	V	
Input L	Vils	CMOS hysteresis input pin	-	Vcc - 0.3	_	0.2 Vcc	V	
voltage	VIL	TTL input pin	-	—	—	0.8	V	
	VILM	MD input pin	-	Vss - 0.3	—	Vss + 0.3	V	
	Vон	All output pins	$V_{CC} = 4.5 V,$ $I_{OH} = -4.0 mA$	Vcc - 0.5	_	_	V	
	Vol	All output pins	$V_{CC} = 4.5 V,$ $I_{OL} = 4.0 mA$	-	_	0.4	V	
•	lı∟	-	$V_{CC} = 5.5 V,$ $V_{SS} < V_{I} < V_{CC}$	-5	_	5	μΑ	
	Rup	P00 to P07, P10 to P17, P20 to P27, P30 to P37, RST	_	25	50	100	kΩ	
Pull-down resistance	Rdown	MD2	-	25	50	100	kΩ	Except Flash devices









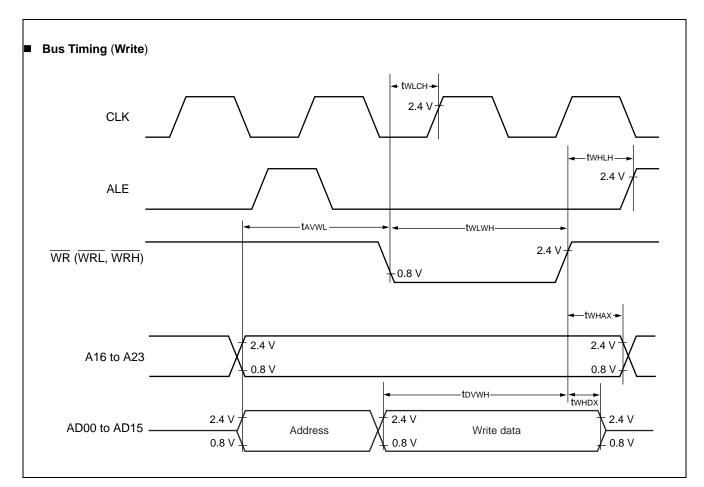




11.4.6 Bus Timing (Write)

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ °C to} + 105 \text{ °C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ °C to} + 105 \text{ °C})

Parameter	Symbol Pin name Condi		Condition	Valu	e	Units	Remarks
Faranieter	Symbol	Fill lidine	Condition	Min	Max	Units	Remarks
Valid address $\rightarrow \overline{\mathrm{WR}} \downarrow$ time	tavwl	A16 to A23 AD00 to AD15, WR		tcp — 15	_	ns	
WR pulse width	twlwh	WR		3 tcp/2 — 20	—	ns	
Valid data output $\rightarrow \overline{WR}^{\uparrow}$ time	tovwн	AD00 to AD15, WR		3 tcp/2 — 20	_	ns	
$\overline{WR} \uparrow \to Data hold time$	twhdx	AD00 to AD15, WR	_	20	_	ns	
$\overline{WR}^{\uparrow} \rightarrow Address$ valid time	t WHAX	A16 to A23, WR		tcp/2 — 10	—	ns	
$\overline{WR}^{\uparrow} \rightarrow ALE^{\uparrow}$ time	twhlh	WR, ALE		tcp/2 — 15	—	ns	
$\overline{WR}^{\uparrow} \rightarrow CLK^{\uparrow}$ time	twlch	WR, CLK		t _{CP} /2 — 20	—	ns	



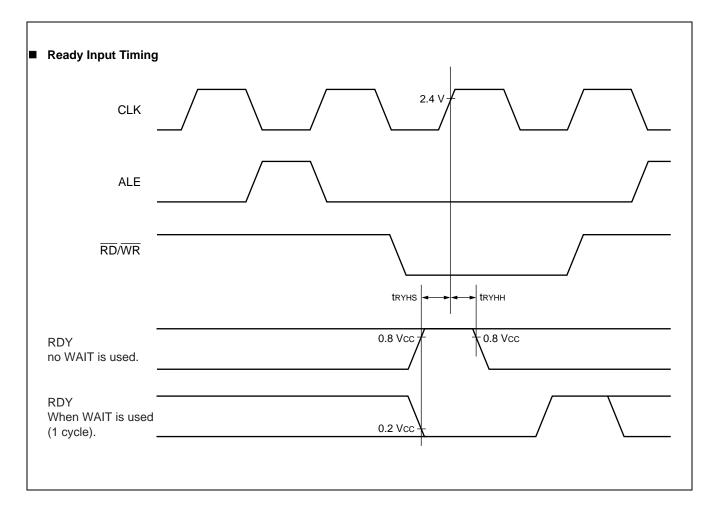


11.4.7 Ready Input Timing

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40 \text{ }^{\circ}\text{C to } + 105 \text{ }^{\circ}\text{C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40 \text{ }^{\circ}\text{C to } + 105 \text{ }^{\circ}\text{C})

Parameter	Symbol	Pin name	Condition	on Value		Units	Remarks
Faranieter	Symbol	Finname	Condition	Min	Min Max	Units	Reliding
RDY setup time	tryhs	RDY		45	_	ns	
RDY hold time	tryнн	RDY	_	0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.



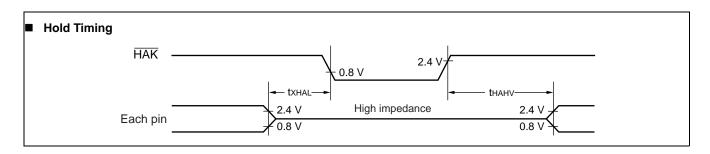


11.4.8 Hold Timing

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V \text{ to } 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ }^{\circ}\text{C} \text{ to } + 105 \text{ }^{\circ}\text{C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10\%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ }^{\circ}\text{C} \text{ to } + 105 \text{ }^{\circ}\text{C})

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
Farameter				Min	Max	Units	Remarks
Pin floating $\rightarrow \overline{\text{HAK}}\downarrow$ time	t xhal	HAK		30	tcp	ns	
\overline{HAK} time \rightarrow Pin valid time	tнанv	HAK	_	tcp	2 tcp	ns	

Note : There is more than 1 cycle from the time HRQ is read to the time the \overline{HAK} is changed.



11.4.9 UART0/1, Serial I/O Timing

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V \text{ to } 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ °C to } + 105 \text{ °C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ °C to } + 105 \text{ °C})

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
Farameter	Farameter Symbol Fin name Condition		Condition	Min	Max	Units	
Serial clock cycle time	tscyc	SCK0 to SCK2		8 tcp	-	ns	
$SCK \downarrow \to SOT$ delay time	tslov	SCK0 to SCK2, SOT0 to SOT2	Internal clock operation	- 80	80	ns	
Valid SIN \rightarrow SCK [↑]	tıvsн	SCK0 to SCK2, SIN0 to SIN2	output pins are C∟ = 80 pF + 1 TTL.	100	_	ns	
$SCK^{\uparrow} \to Valid SIN hold time$	tsнix	SCK0 to SCK2, SIN0 to SIN2		60	_	ns	
Serial clock "H" pulse width	t shsl	SCK0 to SCK2		4 t _{CP}	-	ns	
Serial clock "L" pulse width	tslsh	SCK0 to SCK2		4 tcp	-	ns	
$SCK \downarrow \to SOT$ delay time	tslov	SCK0 to SCK2, SOT0 to SOT2	External clock operation output pins are $C_{L} = 80$	_	150	ns	
Valid SIN \rightarrow SCK \uparrow	tıvsн	SCK0 to SCK2, SIN0 to SIN2	pF + 1 TTL.	60	_	ns	
$SCK^{\uparrow} \to Valid SIN hold time$	tsніх	SCK0 to SCK2, SIN0 to SIN2		60	_	ns	

Notes :

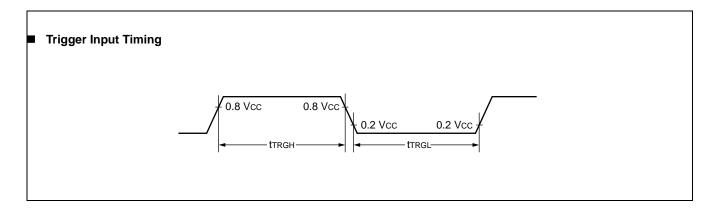
- AC characteristic in CLK synchronized mode.
- C_{L} is load capacity value of pins when testing.
- For tcp (Machine clock cycle time), refer to "(1) Clock Timing".



11.4.12 Trigger Input Timing

 $(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V \text{ to } 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ °C to } + 105 \text{ °C})$ (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 \text{ °C to } + 105 \text{ °C})

Parameter	Symbol	Symbol Pin name	Condition	Value		Units	Remarks	
Falameter	Symbol			Min	Max	Units	Remarks	
Input pulse width	tтrgн	INT0 to INT7,	_	5 tcp	_	ns	Under nomal operation	
	t trgl	ADTG		1		μs	In stop mode	





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