Infineon Technologies - MB90F548GSPMC-GSE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f548gspmc-gse1

Contents

Features	MB90F543G (S) /F548G (S) MB90F549G (S) /F546G (S) MB90F548GL(S)	MB90543G (S) MB90547G (S) MB90548G (S) MB90549G (S)	MB90V540G
16-bit Reload Timer (2 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = System clock frequency) Supports External Event Count function Signals an interrupt when overflow		
16-bit Free-run Timer	Supports Timer Clear when a match with Output Compare (Channel 0) Operation clock freq. : fsys/2^2, fsys/2^4, fsys/2^6, fsys/2^8 (fsys = System clock freq.)		
16-bit Output Compare (4 channels)	Signals an interrupt when a match with 16-bit Free-run Timer Four 16-bit compare registers A pair of compare registers can be used to generate an output signal		
16-bit Input Capture (8 channels)	Rising edge, falling edge or rising & falling edge sensitive Four 16-bit Capture registers Signals an interrupt upon external event		
8/16-bit Programmable Pulse Generator (4 channels)	Supports 8-bit and 16-bit operation modes Eight 8-bit reload counters Eight 8-bit reload registers for L pulse width Eight 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter 4 output pins Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 µs@fosc = 4 MHz (fsys = System clock frequency, fosc = Oscillation clock frequency)		
CAN Interface MB90540G series : 2 channels MB90545G series : 1 channel	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 massage buffers for data and ID's supports multipe massages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps		
32 kHz Sub-clock	Sub-clock for low power operation		
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive		
External bus interface	External access using the selectable 8-bit or 16-bit bus is enabled (external bus mode.)		
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs and schmitt trigger inputs Bit-wise programmable as input/output or peripheral signal Sub-clock for 32 kHz Sub clock low power operation		
Flash Memory	Supports automatic programming, Embeded Algorithm Write/Erase/Erase-Suspend/Erase-Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block Block protection by externally programmed voltage		

*1 : If the one clock system is used, equip X0A and X1A with clocks from the tool side.

*2 : It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*3 : Operating Voltage Range

Products	Operation guarantee range
MB90F543G(S)/F546G(S)/F548G(S)/ MB90549G(S)/F549G(S)/V540/V540G	4.5 V to 5.5 V
MB90F548GL(S)/543G(S)/547G(S)/548G(S)	3.5 V to 5.5 V

Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
11	13	P33	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode, external bus 8-bit mode or when WRH pin output is disabled.
		$\overline{\text{WRH}}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{\text{WRH}}$ output pin is enabled.
12	14	P34	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.
13	15	P35	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.
14	16	P36	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.
		RDY		Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.
15	17	P37	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the CLK output is disabled.
		CLK		CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled.
16	18	P40	G	General I/O port. This function is enabled when UART0 disables the serial data output.
		SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.
17	19	P41	G	General I/O port. This function is enabled when UART0 disables serial clock output.
		SCK0		Serial clock I/O pin for UART0. This function is enabled when UART0 enables the serial clock output.
18	20	P42	G	General I/O port. This function is always enabled.
		SIN0		Serial data input pin for UART0. Set the corresponding Port Direction Register to input if this function is used.
19	21	P43	G	General I/O port. This function is always enabled.
		SIN1		Serial data input pin for UART1. Set the corresponding Port Direction Register to input if this function is used.

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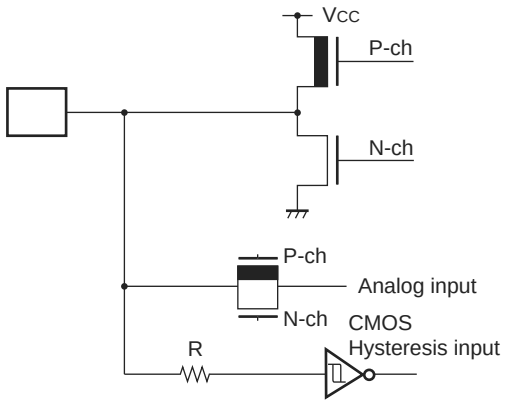
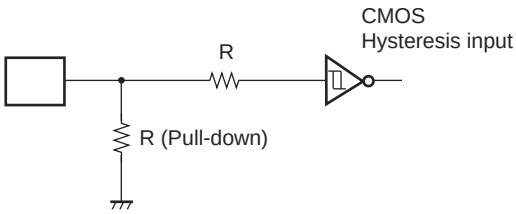
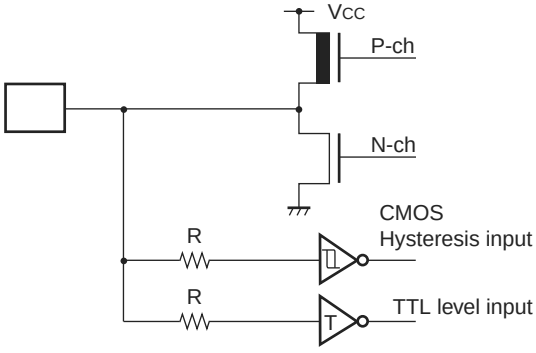
Pin No.		Pin name	Circuit type	Function
LQFP*2	QFP*1			
72	74	P95	D	General I/O port. This function is always enabled.
		RX0		RX input pin for CAN0 Interface. When the CAN function is used, output from the other functions must be stopped.
73	75	P96	D	General I/O port. This function is enabled when CAN1 disables the output.
		TX1		TX output pin for CAN1. This function is enabled when CAN1 enables the output (only MB90540G series) .
74	76	P97	D	General I/O port. This function is always enabled.
		RX1		RX input pin for CAN1 Interface. When the CAN function is used, output from the other functions must be stopped (only MB90540G series) .
76	78	PA0	D	General I/O port. This function is always enabled.
32	34	AV_{CC}	Power supply	Power supply pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AV_{CC} is applied to V_{CC}.
35	37	AV_{SS}	Power supply	Power supply pin for the A/D Converter.
33	35	AVRH	Power supply	External reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV_{CC}.
34	36	AVRL	Power supply	External reference voltage input pin for the A/D Converter.
47, 48	49, 50	MD0, MD1	C	Input pins for specifying the operating mode. The pins must be directly connected to V_{CC} or V_{SS}.
49	51	MD2	F	Input pin for specifying the operating mode. The pin must be directly connected to V_{CC} or V_{SS}.
25	27	C	—	Power supply stabilization capacitor pin. It should be connected externally to an 0.1 µF ceramic capacitor.
21, 82	23, 84	V_{CC}	Power supply	Input pin for power supply (5.0 V) .
9, 40, 79	11, 42, 81	V_{SS}	Power supply	Input pin for power supply (0.0 V) .

*1 : FPT-100P-M06

*2 : FPT-100P-M20

Circuit type	Diagram	Remarks
E		■ CMOS level output ■ CMOS Hysteresis input ■ Analog input
F		■ CMOS Hysteresis input ■ Pull-down Resistor : 50 kΩ approx. (except Flash devices)
G		■ CMOS level output ■ CMOS Hysteresis input ■ TTL level input (Flash devices in Flash writer mode only)

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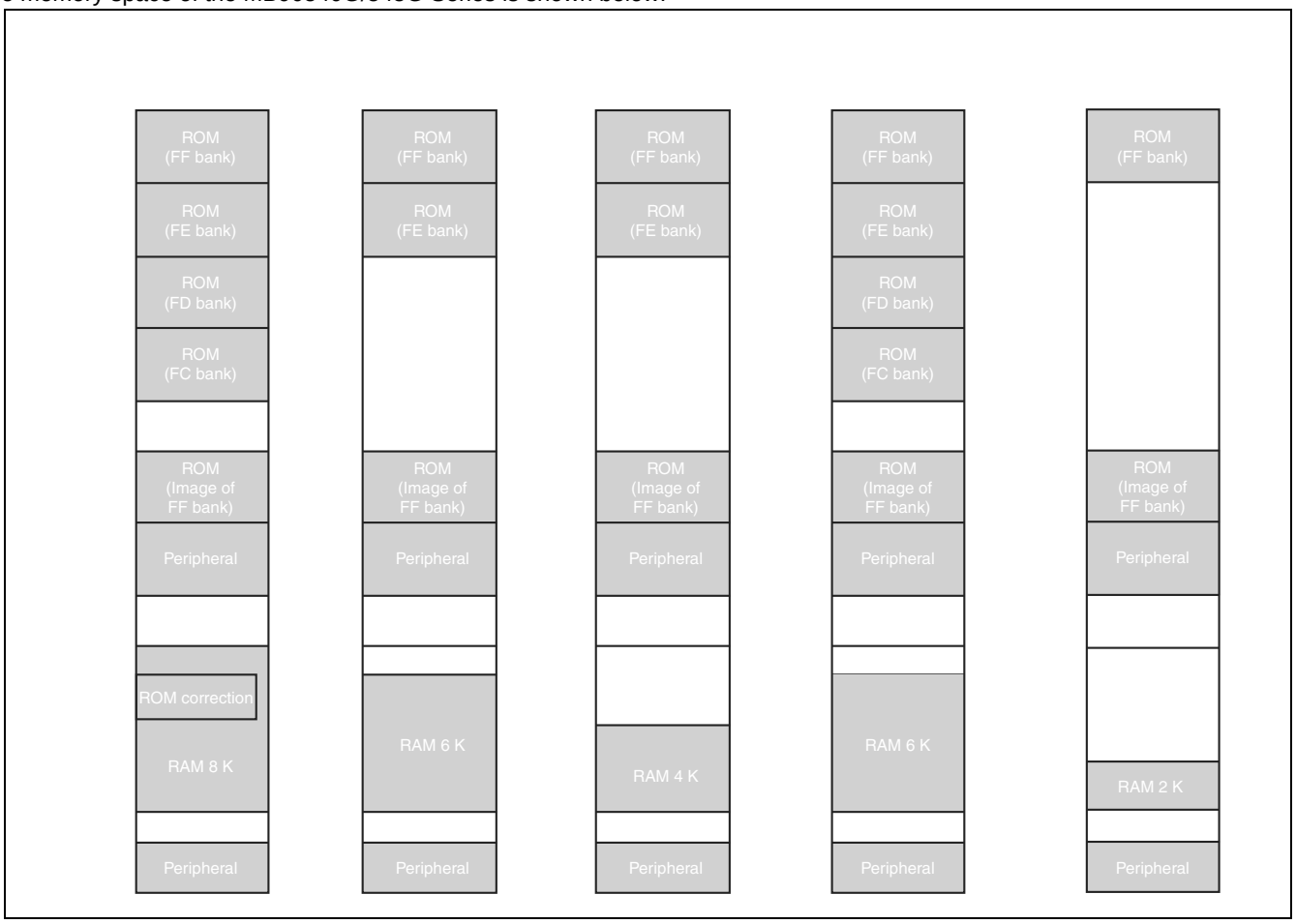
7. Memory Map

The memory space of the MB90540G/545G Series is shown below.



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits address are the same, the table in ROM can be referenced without using the “far” specification in the pointer declaration.
For example, an attempt to access $00C000_H$ accesses the value at $FFC000_H$ in ROM.The ROM area in bank FF exceeds 48 Kbytes, and its entire image cannot be shown in bank 00.The image between $FF4000_H$ and $FFFFFF_H$ is visible in bank 00, while the image between $FF0000_H$ and $FF3FFF_H$ is visible only in bank FF.

Address	Register	Abbreviation	Access	Resource name	Initial value
47_H to $4B_H$	Prohibited				
$4C_H$	Input capture control status register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0_B
$4D_H$	Input capture control status register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0_B
$4E_H$	Input capture control status register 4/5	ICS45	R/W	Input Capture 4/5	0 0 0 0 0 0 0 0_B
$4F_H$	Input capture control status register 6/7	ICS67	R/W	Input Capture 6/7	0 0 0 0 0 0 0 0_B
50_H	Timer control status register 0	TMCSR0	R/W	16-bit Reload Timer 0	0 0 0 0 0 0 0 0_B
51_H	Timer control status register 0	TMCSR0	R/W		_ _ _ _ 0 0 0 0_B
52_H	Timer register 0/reload register 0	TMR0/TMRLR0	R/W		XXXXXXXX_B
53_H	Timer register 0/reload register 0	TMR0/TMRLR0	R/W		XXXXXXXX_B
54_H	Timer control status register 1	TMCSR1	R/W	16-bit Reload Timer 1	0 0 0 0 0 0 0 0_B
55_H	Timer control status register 1	TMCSR1	R/W		_ _ _ _ 0 0 0 0_B
56_H	Timer register 1/reload register 1	TMR1/TMRLR1	R/W		XXXXXXXX_B
57_H	Timer register 1/reload register 1	TMR1/TMRLR1	R/W		XXXXXXXX_B
58_H	Output compare control status register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 _ _ 0 0_B
59_H	Output compare control status register 1	OCS1	R/W		_ _ _ 0 0 0 0 0_B
$5A_H$	Output compare control status register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 _ _ 0 0_B
$5B_H$	Output compare control status register 3	OCS3	R/W		_ _ _ 0 0 0 0 0_B
$5C_H$ to $6B_H$	Prohibited				
$6C_H$	Timer Data register	TCDT	R/W	I/O Timer	0 0 0 0 0 0 0 0_B
$6D_H$	Timer Data register	TCDT	R/W		0 0 0 0 0 0 0 0_B
$6E_H$	Timer Control register	TCCS	R/W		0 0 0 0 0 0 0 0_B
$6F_H$	ROM mirror function selection register	ROMM	R/W	ROM Mirror	_ _ _ _ _ _ _ 1_B
70_H to $7F_H$	Reserved for CAN 0 Interface.				
80_H to $8F_H$	Reserved for CAN 1 Interface.				
90_H to $9D_H$	Prohibited				
$9E_H$	Program address detection control status register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0_B
$9F_H$	Delayed interrupt/release register	DIRR	R/W	Delayed Interrupt	_ _ _ _ _ _ _ 0_B
$A0_H$	Low-power mode control register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0_B
$A1_H$	Clock selection register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0_B

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A24H	003C24H	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXXB
003A25H	003C25H				
003A26H	003C26H				XXXXX--- XXXXXXXXB
003A27H	003C27H				
003A28H	003C28H	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXXB
003A29H	003C29H				
003A2AH	003C2AH				XXXXX--- XXXXXXXXB
003A2BH	003C2BH				
003A2CH	003C2CH	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXXB
003A2DH	003C2DH				
003A2EH	003C2EH				XXXXX--- XXXXXXXXB
003A2FH	003C2FH				
003A30H	003C30H	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXXB
003A31H	003C31H				
003A32H	003C32H				XXXXX--- XXXXXXXXB
003A33H	003C33H				
003A34H	003C34H	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXXB
003A35H	003C35H				
003A36H	003C36H				XXXXX--- XXXXXXXXB
003A37H	003C37H				
003A38H	003C38H	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXXB
003A39H	003C39H				
003A3AH	003C3AH				XXXXX--- XXXXXXXXB
003A3BH	003C3BH				

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A3C$_H$	003C3C$_H$	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX$_B$
003A3D$_H$	003C3D$_H$				
003A3E$_H$	003C3E$_H$				XXXXX--- XXXXXXXX$_B$
003A3F$_H$	003C3F$_H$				
003A40$_H$	003C40$_H$	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXX$_B$
003A41$_H$	003C41$_H$				
003A42$_H$	003C42$_H$				XXXXX--- XXXXXXXX$_B$
003A43$_H$	003C43$_H$				
003A44$_H$	003C44$_H$	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXX$_B$
003A45$_H$	003C45$_H$				
003A46$_H$	003C46$_H$				XXXXX--- XXXXXXXX$_B$
003A47$_H$	003C47$_H$				
003A48$_H$	003C48$_H$	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX$_B$
003A49$_H$	003C49$_H$				
003A4A$_H$	003C4A$_H$				XXXXX--- XXXXXXXX$_B$
003A4B$_H$	003C4B$_H$				
003A4C$_H$	003C4C$_H$	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX$_B$
003A4D$_H$	003C4D$_H$				
003A4E$_H$	003C4E$_H$				XXXXX--- XXXXXXXX$_B$
003A4F$_H$	003C4F$_H$				
003A50$_H$	003C50$_H$	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX$_B$
003A51$_H$	003C51$_H$				
003A52$_H$	003C52$_H$				XXXXX--- XXXXXXXX$_B$
003A53$_H$	003C53$_H$				
003A54$_H$	003C54$_H$	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX$_B$
003A55$_H$	003C55$_H$				
003A56$_H$	003C56$_H$				XXXXX--- XXXXXXXX$_B$
003A57$_H$	003C57$_H$				
003A58$_H$	003C58$_H$	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX$_B$
003A59$_H$	003C59$_H$				
003A5A$_H$	003C5A$_H$				XXXXX--- XXXXXXXX$_B$
003A5B$_H$	003C5B$_H$				
003A5C$_H$	003C5C$_H$	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX$_B$
003A5D$_H$	003C5D$_H$				
003A5E$_H$	003C5E$_H$				XXXXX--- XXXXXXXX$_B$
003A5F$_H$	003C5F$_H$				

(Continued)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A88H to 003A8FH	003C88H to 003C8FH	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXXB to XXXXXXXXB
003A90H to 003A97H	003C90H to 003C97H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXXB to XXXXXXXXB
003A98H to 003A9FH	003C98H to 003C9FH	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXXB to XXXXXXXXB
003AA0H to 003AA7H	003CA0H to 003CA7H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXXB to XXXXXXXXB
003AA8H to 003AAFH	003CA8H to 003CAFH	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXXB to XXXXXXXXB
003AB0H to 003AB7H	003CB0H to 003CB7H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXXB to XXXXXXXXB
003AB8H to 003ABFH	003CB8H to 003CBFH	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXXB to XXXXXXXXB
003AC0H to 003AC7H	003CC0H to 003CC7H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXXB to XXXXXXXXB
003AC8H to 003ACFH	003CC8H to 003CCFH	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXXB to XXXXXXXXB
003AD0H to 003AD7H	003CD0H to 003CD7H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXXB to XXXXXXXXB
003AD8H to 003ADFH	003CD8H to 003CDFH	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXXB to XXXXXXXXB
003AE0H to 003AE7H	003CE0H to 003CE7H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXXB to XXXXXXXXB
003AE8H to 003AEFH	003CE8H to 003CEFH	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXXB to XXXXXXXXB
003AF0H to 003AF7H	003CF0H to 003CF7H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXXB to XXXXXXXXB
003AF8H to 003AFFH	003CF8H to 003CFFH	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXXB to XXXXXXXXB

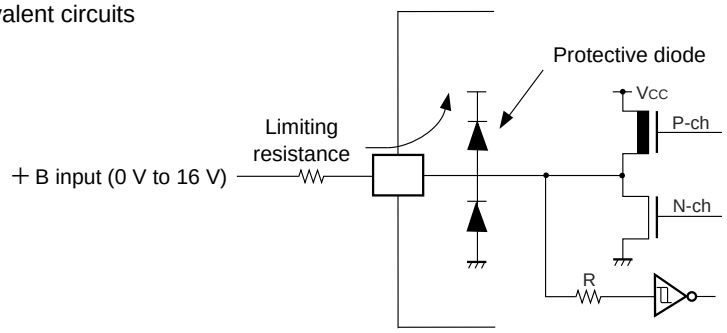
10. Interrupt Map

Interrupt cause	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC$_H$	—	—
INT9 instruction	N/A	#09	FFFFD8$_H$	—	—
Exception	N/A	#10	FFFFD4$_H$	—	—
CAN 0 RX	N/A	#11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN 0 TX/NS	N/A	#12	FFFFCC$_H$		
CAN 1 RX	N/A	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 1 TX/NS	N/A	#14	FFFFC4$_H$		
External Interrupt INT0/INT1	*1	#15	FFFFC0$_H$	ICR02	0000B2$_H$
Time Base Timer	N/A	#16	FFFFBC$_H$		
16-bit Reload Timer 0	*1	#17	FFFFB8$_H$	ICR03	0000B3$_H$
8/10-bit A/D Converter	*1	#18	FFFFB4$_H$		
16-bit Free-run Timer	N/A	#19	FFFFB0$_H$	ICR04	0000B4$_H$
External Interrupt INT2/INT3	*1	#20	FFFFAC$_H$		
Serial I/O	*1	#21	FFFFA8$_H$	ICR05	0000B5$_H$
8/16-bit PPG 0/1	N/A	#22	FFFFA4$_H$		
Input Capture 0	*1	#23	FFFFA0$_H$	ICR06	0000B6$_H$
External Interrupt INT4/INT5	*1	#24	FFFF9C$_H$		
Input Capture 1	*1	#25	FFFF98$_H$	ICR07	0000B7$_H$
8/16-bit PPG 2/3	N/A	#26	FFFF94$_H$		
External Interrupt INT6/INT7	*1	#27	FFFF90$_H$	ICR08	0000B8$_H$
Watch Timer	N/A	#28	FFFF8C$_H$		
8/16-bit PPG 4/5	N/A	#29	FFFF88$_H$	ICR09	0000B9$_H$
Input Capture 2/3	*1	#30	FFFF84$_H$		
8/16-bit PPG 6/7	N/A	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 0	*1	#32	FFFF7C$_H$		
Output Compare 1	*1	#33	FFFF78$_H$	ICR11	0000BB$_H$
Input Capture 4/5	*1	#34	FFFF74$_H$		
Output Compare 2/3 - Input Capture 6/7	*1	#35	FFFF70$_H$	ICR12	0000BC$_H$
16-bit Reload Timer 1	*1	#36	FFFF6C$_H$		
UART 0 RX	*2	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 0 TX	*1	#38	FFFF64$_H$		
UART 1 RX	*2	#39	FFFF60$_H$	ICR14	0000BE$_H$
UART 1 TX	*1	#40	FFFF5C$_H$		
Flash Memory	N/A	#41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed interrupt	N/A	#42	FFFF54$_H$		

(Continued)

- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept + B signal input.
- Sample recommended circuits :

■ Input/Output Equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

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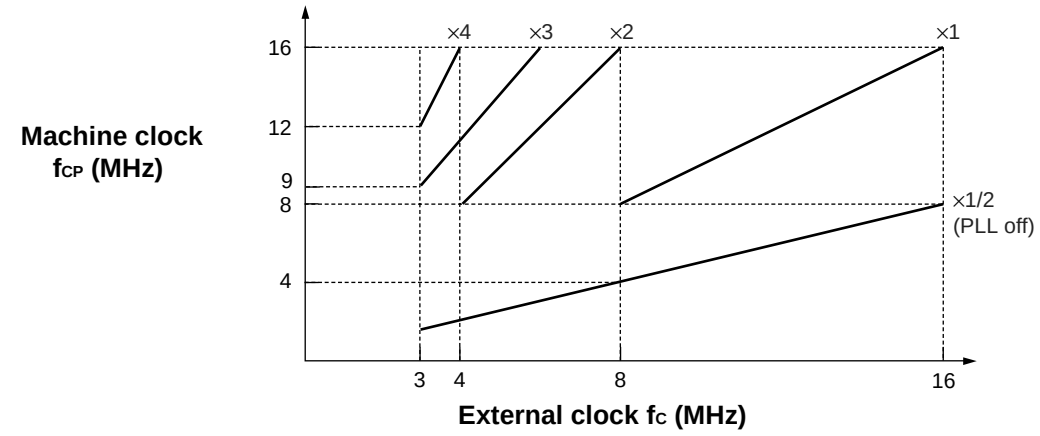
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +105 °C)

Parameter	Symbol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Power supply current*	I_{CC}	V_{CC}	Internal frequency : 16 MHz, At normal operating	—	40	55	mA	
			Internal frequency : 16 MHz, At Flash programming/erasing	—	50	70	mA	Flash device
	I_{CCS}		Internal frequency : 16 MHz, At sleep mode	—	12	20	mA	
	I_{CTS}		V_{CC} = 5.0 V ± 10%, Internal frequency : 2 MHz, At pseudo timer mode	—	300	600	µA	
				—	600	1100	µA	MB90F548GL (S) only
				—	200	400	µA	MB90543G(S)/547G(S)/548(S) only
	I_{CCL}		Internal frequency : 8 kHz, At sub operation, T_A = 25 °C	—	400	750	µA	MB90F548GL only
				—	50	100	µA	MASK ROM
				—	150	300	µA	Flash device
	I_{CCLS}		Internal frequency : 8 kHz, At sub sleep, T_A = 25 °C	—	15	40	µA	
	I_{CCT}		Internal frequency : 8 kHz, At timer mode, T_A = 25 °C	—	7	25	µA	
	I_{CCH1}		At stop, T_A = 25 °C	—	5	20	µA	
	I_{CCH2}		At hardware standby mode, T_A = 25 °C	—	50	100	µA	
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVRH, AVRL, C, V_{CC}, V_{SS}	—	—	5	15	pF	

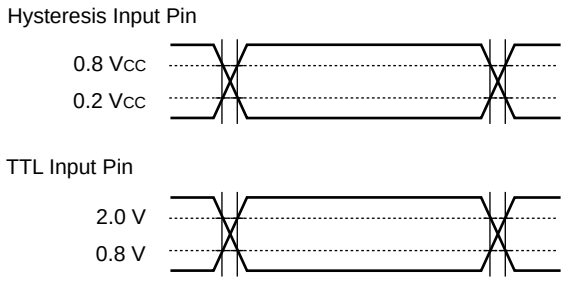
* : The power supply current testing conditions are when using the external clock.

■ **External clock frequency and Machine clock frequency**

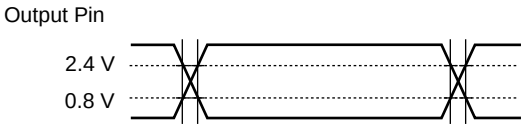


AC characteristics are set to the measured reference voltage values below.

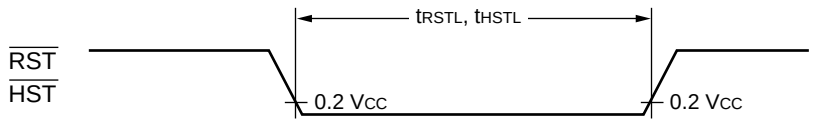
■ **Input signal waveform**



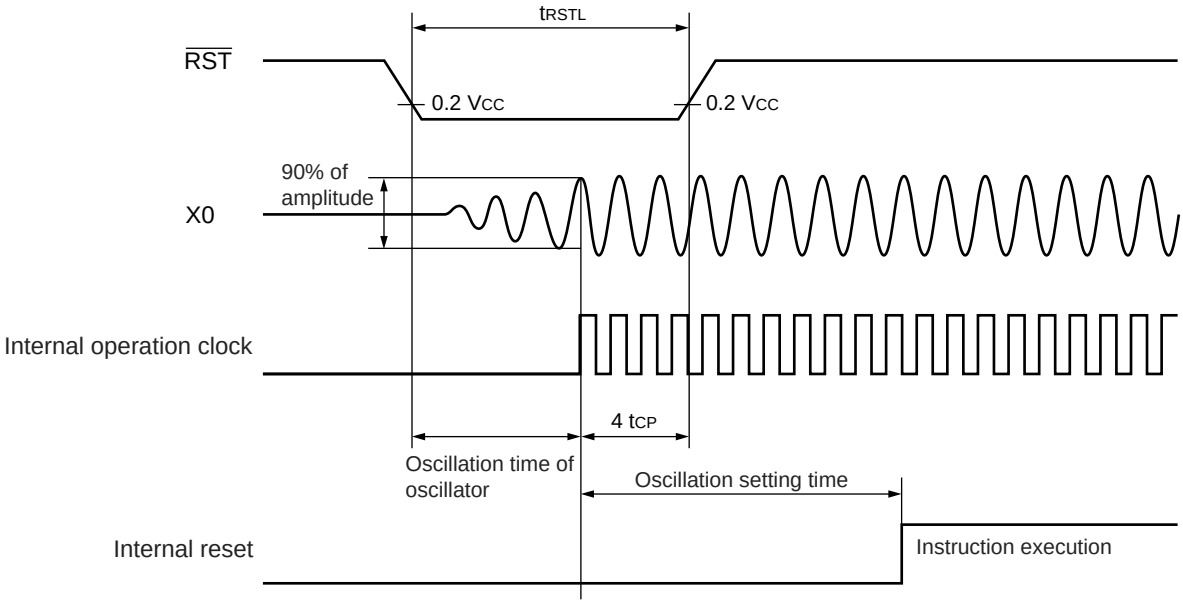
■ **Output signal waveform**



■ In under normal operation, pseudo timer mode, sub-clock mode, sub-sleep mode, timer mode



■ In stop mode



11.4.4 Power On Reset

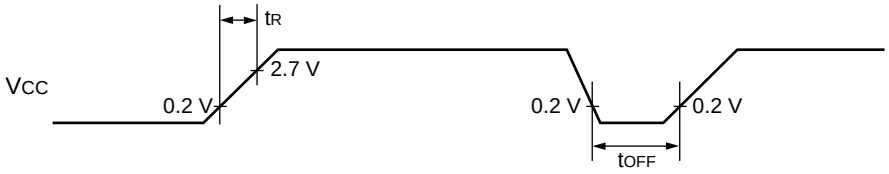
(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

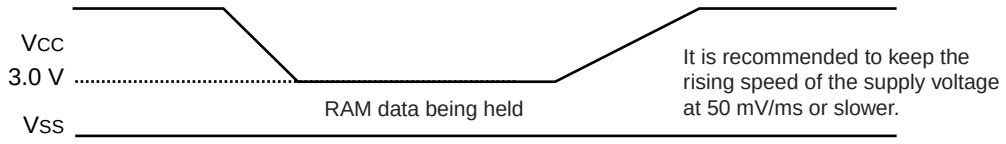
Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	*
Power off time	t_{OFF}	V_{CC}		50	—	ms	Waiting time until power-on

* : V_{CC} must be kept lower than 0.2 V before power-on.

Notes : ■ The above values are used for creating a power-on reset.
■ Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.



11.4.5 Bus Timing (Read)

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE		$t_{CP}/2 - 20$	−	ns	
Valid address → ALE↓ time	t_{AVLL}	ALE, A16 to A23, AD00 to AD15		$t_{CP}/2 - 20$	−	ns	
ALE↓ → Address valid time	t_{LLAX}	ALE, AD00 to AD15		$t_{CP}/2 - 15$	−	ns	
Valid address → $\overline{RD}$↓ time	t_{AVRL}	A16 toA23, AD00 to AD15, $\overline{RD}$		$t_{CP} - 15$	−	ns	
Valid address → Valid data input	t_{AVDV}	A16 to A23, AD00 to AD15		−	$5\ t_{CP}/2 - 60$	ns	
$\overline{RD}$ pulse width	t_{RLRH}	RD	−	$3\ t_{CP}/2 - 20$	−	ns	
$\overline{RD}$↓ → Valid data input	t_{RLDV}	$\overline{RD}$, AD00 to AD15		−	$3\ t_{CP}/2 - 60$	ns	
$\overline{RD}$↑ → Data hold time	t_{RHDX}	$\overline{RD}$, AD00 to AD15		0	−	ns	
$\overline{RD}$↑ → ALE↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	−	ns	
$\overline{RD}$↑ → Address valid time	t_{RHAX}	$\overline{RD}$, A16 to A23		$t_{CP}/2 - 10$	−	ns	
Valid address → CLK↑ time	t_{AVCH}	A16 to A23, AD00 to AD15, CLK		$t_{CP}/2 - 20$	−	ns	
$\overline{RD}$↓ → CLK↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 20$	−	ns	
ALE↓ → $\overline{RD}$↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	−	ns	

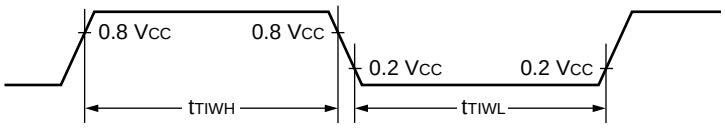
11.4.10 Timer Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	4 t_{CP}	—	ns	
	t_{TIWL}	IN0 to IN7					

■ **Timer Input Timing**



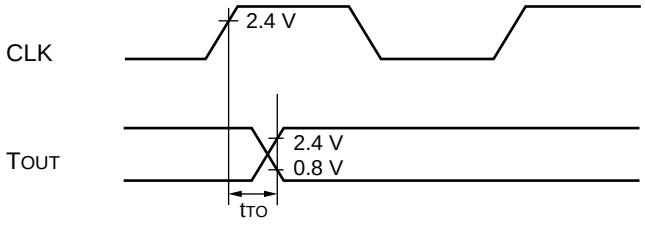
11.4.11 Timer Output Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 3.5 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

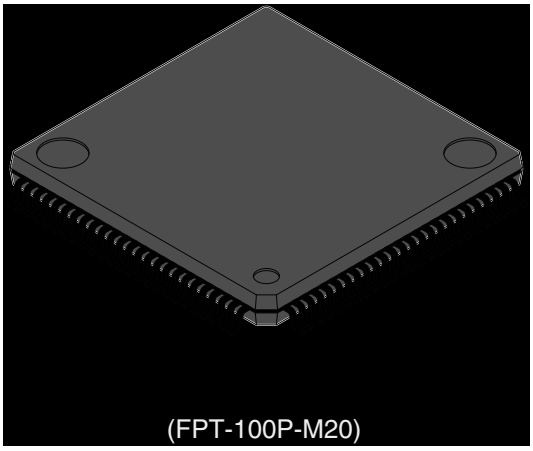
(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): V_{CC} = 5.0 V ± 10%, V_{SS} = AV_{SS} = 0.0 V, T_A = − 40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
CLK↑ → T_{OUT} change time	t_{TO}	TOT0 , TOT1, PPG0 to PPG3	—	30	—	ns	

■ **Timer Output Timing**



(Continued)



(FPT-100P-M20)