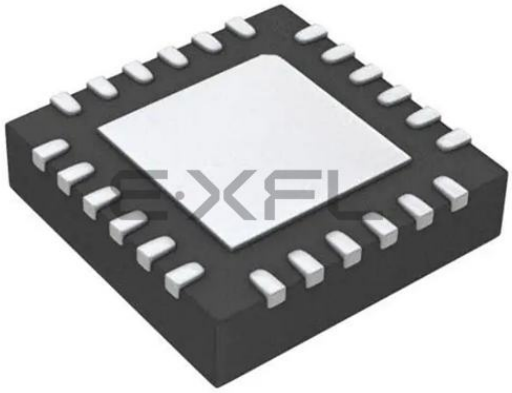

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 18x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f547-im

- ROM, RAM capacities

Flash ROM	Data Flash	RAM	RL78/G1D
128 KB	8 KB	12 KB	R5F11AGG
192 KB	8 KB	16 KB	R5F11AGH
256 KB	8 KB	20 KB[Note]	R5F11AGJ

Note 19 KB when the self-programming function is used.

1.6 Outline of Functions

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		R5F11AGG	R5F11AGH	R5F11AGJ
Code flash memory		128 KB	192 KB	256 KB
Data flash memory		8 KB	8 KB	8 KB
RAM		12 KB	16 KB	20 KB[Note 1]
Address space		1 MB		
System clock (RF side)		32 MHz		
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 3.6 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 3.6 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 3.6 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 3.6 V)		
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 3.6 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 3.6 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 3.6 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 3.6 V)		
Subsystem clock		XT1 (Crystal) oscillation, External main system clock input (EXCLKS) 32.768 kHz		
RF slow clock	External input	External clock input for RF block (EXSLK_RF) 32.768 kHz (TYP.)		
	On-chip Oscillator	32.768 kHz (TYP.)		
Low-speed on-chip oscillator		15 kHz (TYP.)		
General-purpose register		(8-bit register × 8) × 4 banks		
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillation clock: f_{IH} = 32 MHz operation)		
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)		
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)		
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.		
I/O port	Total	32[Note 2]		
	CMOS I/O	20[Note 2]		
	CMOS input	5[Note 2]		
	CMOS output	1[Note 2]		
	N-ch O.D. I/O (withstand voltage: 6 V)	2		
	GPIO (RF block)	4		
2.4 GHz RF transceiver		Supporting Bluetooth v4.1 Specification (Single mode). 2.4 GHz ISM Band, GFSK modulation, TDMA/TDD frequency hopping (Including AES encryption circuit.) Adaptivity (Only in slave operation)		
Timer	16-bit timer	8 channels		
	Watchdog timer	1 channel		
	Real-time clock (RTC)	1 channel		
	12-bit interval timer	1 channel		

(Notes are listed on the next page.)

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}	V_{DD}	–0.5 to +6.5	V
	V_{DDRF1}	V_{DD_RF}	–0.5 to +4.0	V
	V_{DDRF2}	AV_{DD_RF}	–0.5 to +4.0	V
	V_{DDRF3}	DCLIN	–0.5 to +4.0	V
	V_{SSRF}	V_{SS_RF}, AV_{SS_RF}	–0.5 to +0.3	V
Input voltage	V_{I1}	P00, P01, P02, P03, P10, P11, P12, P14, P15, P16, P20, P21, P22, P23, P30, P40, P120, P121, P122, P123, P124, P137, P140, P147, RESET	–0.3 to V_{DD}+0.3 Note 1	V
	V_{I2}	P60, P61	–0.3 to +6.5	V
	V_{IRF1}	GPIO0, GPIO1, GPIO2, GPIO3	–0.3 to V_{DD_RF}+0.3 Note 2	V
	V_{IRF2}	ANT	–0.5 to +1.4	V
Output voltage	V_O	P00, P01, P02, P03, P10, P11, P12, P14, P15, P16, P20, P21, P22, P23, P30, P40, P60, P61, P120, P130, P140, P147	–0.3 to V_{DD}+0.3 Note 1	V
	V_{ORF}	GPIO0, GPIO1, GPIO2, GPIO3, DCLOUT	–0.3 to V_{DD_RF}+0.3 Note 2	V
Analog input voltage	V_{AI}	ANI0, ANI1, ANI2, ANI3, ANI16, ANI17, ANI18, ANI19	–0.3 to V_{DD}+0.3 and –0.3 to $V_{REF(+)}$+0.3 Notes 2, 4	V
REGC pin input voltage	V_{IREGC}	REGC	–0.3 to +2.8 and –0.3 to V_{DD}+0.3 Note 3	V
IC pin input voltage	V_{IIC}	IC0, IC1	–0.5 to +0.3	V

Notes 1. Must be 6.5 V or lower.

2. Must be 4.0 V or lower.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

4. Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. Reference voltage is V_{SS}.

2.3 Oscillator Characteristics

2.3.1 X1, XT1, XRF oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency[Note 1]	Ceramic resonator Crystal resonator	f_X	2.7 V ≤ V_{DD} ≤ 3.6 V	1		20	MHz
			1.8 V ≤ V_{DD} < 2.7 V	1		8	MHz
			1.6 V ≤ V_{DD} ≤ 1.8 V	1		4	MHz
XT1 clock oscillation frequency[Note 1]		f_{XT}		32	32.768	35	kHz
RF base clock oscillation frequency[Note 2]		f_{XRF}			32		MHz
RF base clock oscillation frequency accuracy[Note 2]		f_{XRFP}		-20		+20	ppm

Notes 1. Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time.
Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

2. This Oscillator characteristics is base clock for RF Transceiver.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user.
Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

2.3.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Oscillators	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency[Notes 1, 2]	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy	f_{IHP}	–20 to +85°C	1.8 V ≤ V_{DD} ≤3.6 V	-1.5		+1.5.	%
			1.6 V ≤ V_{DD} <1.8 V	-5.0		+5.0	%
		–40 to –20°C	1.8 V ≤ V_{DD} ≤3.6 V	-2.5		+2.5.	%
			1.6 V ≤ V_{DD} <1.8 V	-5.5		+5.5	%
Low-speed on-chip oscillator clock frequency[Notes 3]	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy	f_{ILP}			–15		+15	%
On-chip oscillator clock frequency for the RF slow clock[Note 3]	f_{ILRF}				32.768		kHz
On-chip oscillator clock frequency accuracy for the RF slow clock	f_{ILRFP}			-0.025		0.025	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to **AC Characteristics** for instruction execution time.

3. This indicates the oscillator characteristics only.

2.4 DC Characteristics

2.4.1 Output current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			–10.0[Note 2]	mA
		P00, P01, P02, P03, P40, P120, P130, P140	Total[Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V			–10.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			–5.0	mA
				1.6 V ≤ V_{DD} < 1.8 V			–2.5	mA
		P10, P11, P12, P13, P14, P15, P16, P30, P147	Total[Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V			–19.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			–10.0	mA
				1.6 V ≤ V_{DD} < 1.8 V			–5.0	mA
		Total of all pins[Note 3]		1.6 V ≤ V_{DD} ≤ 3.6 V			–135.0[Note 4]	mA
	I_{OH2}	P20, P21, P22, P23	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			–0.1[Note 2]	mA
			Total[Note 3]	1.6 V ≤ V_{DD} ≤ 3.6 V			–1.5	mA
	I_{OHRF}	GPIO0, GPIO1, GPIO2, GPIO3	Per pin	1.6 V ≤ V_{DD_RF} ≤ 3.6 V			–2.0	mA
Output current, low[Note 1]	I_{OL1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			20.0[Note 2]	mA
		P60, P61	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			15.0[Note 2]	mA
		P00, P01, P02, P03, P40, P120, P130, P140	Total[Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V			15.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
				1.6 V ≤ V_{DD} < 1.8 V			4.5	mA
		P10, P11, P12, P13, P14, P15, P16, P30, P60, P61, P147	Total[Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V			35.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			20.0	mA
				1.6 V ≤ V_{DD} < 1.8 V			10.0	mA
		Total of all pins[Note 3]		1.6 V ≤ V_{DD} ≤ 3.6 V			150.0	mA
	I_{OL2}	P20, P21, P22, P23	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			0.4[Note 2]	mA
			Total[Note 3]	1.6 V ≤ V_{DD} ≤ 3.6 V			5.0	mA
	I_{OLRF}	GPIO0, GPIO1, GPIO2, GPIO3	Per pin	1.6 V ≤ V_{DD_RF} ≤ 3.6 V			2.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 50% and I_{OH} = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(50 × 0.01) = –14.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. Product for industrial applications (R5F11AGGDNB, R5F11AGHDNB, R5F11AGJDNB) is –100.0 mA.

(**Caution** and **Remark** are listed on the next page.)

Caution P00, P02, P03, and P10 to P15 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.4.2 Input current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	Normal mode (I_{THL} = 1)	0.8V_{DD}		V_{DD}	V
	V_{IH2}	P01, P03, P10, P11, P13, P14, P15, P16	TTL mode 3.3 V ≤ V_{DD} ≤ 3.6 V	2.0		V_{DD}	V
			TTL mode 1.6 V ≤ V_{DD} < 3.3V	1.5		V_{DD}	V
	V_{IH3}	P20, P21, P22, P23		0.7V_{DD}		V_{DD}	V
	V_{IH4}	P60, P61		0.7V_{DD}		6.0	V
	V_{IH5}	P121, P122, P123, P124, P137, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IHRF}	GPIO0, GPIO1, GPIO2, GPIO3		0.85V_{DD_RF}		V_{DD_RF}	V
Input voltage, low	V_{IL1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P140, P147	Normal mode (I_{THL} = 1)	0		0.2V_{DD}	V
	V_{IL2}	P01, P03, P10, P11, P13, P14, P15, P16	TTL mode 3.3 V ≤ V_{DD} ≤ 3.6 V	0		0.5	V
			TTL mode 1.6 V ≤ V_{DD} < 3.3V	0		0.32	V
	V_{IL3}	P20, P21, P22, P23		0		0.3V_{DD}	V
	V_{IL4}	P60, P61		0		0.3V_{DD}	V
	V_{IL5}	P121, P122, P123, P124, P137, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{ILRF}	GPIO0, GPIO1, GPIO2, GPIO3		0		0.1V_{DD_RF}	V

Caution The maximum value of V_{IH} of pins P00, P02, P03, and P10 to P15 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) Standby current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
HALT current Note 1, 2	I_{DD2}	HS (high-speed main) mode Note 7	f_{IH} = 32 MHz Note 4	V_{DD} = 3.0 V		0.62	1.86	mA
			f_{IH} = 24 MHz Note 4	V_{DD} = 3.0 V		0.50	1.45	mA
			f_{IH} = 16 MHz Note 4	V_{DD} = 3.0 V		0.44	1.11	mA
		LS (low-speed main) mode Note 7	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		290	620	μA
				V_{DD} = 2.0 V		290	620	μA
		LV (low-voltage main) mode Note 7	f_{IH} = 4 MHz Note 4	V_{DD} = 3.0 V		440	680	μA
				V_{DD} = 2.0 V		440	680	μA
		HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3	V_{DD} = 3.0 V Note 9		0.31	1.08	mA
						0.48	1.28	mA
			f_{MX} = 10 MHz Note 3	V_{DD} = 3.0 V Note 9		0.21	0.63	mA
						0.28	0.71	mA
		LS (low-speed main) mode Note 7	f_{MX} = 8 MHz Note 3	V_{DD} = 3.0 V Note 9		110	360	μA
						160	420	μA
				V_{DD} = 2.0 V Note 9		110	360	μA
						160	420	μA
		Subsystem clock operation	f_{SUB} = 32.768kHz Note 5	T_A = –40°C Note 9		0.28	0.61	μA
						0.47	0.80	μA
				T_A = +25°C Note 9		0.34	0.61	μA
						0.53	0.80	μA
				T_A = +50°C Note 9		0.41	2.30	μA
						0.60	2.49	μA
				T_A = +70°C Note 9		0.64	4.03	μA
						0.83	4.22	μA
				T_A = +85°C Note 9		1.09	8.04	μA
						1.28	8.23	μA
STOP current Note 6, 8	I_{DD3}	T_A = –40°C				0.19	0.52	μA
		T_A = +25°C				0.25	0.52	μA
		T_A = +50°C				0.32	2.21	μA
		T_A = +70°C				0.55	3.94	μA
		T_A = +85°C				1.00	7.95	μA

(**Notes** and **Remarks** are listed on the next page.)

(3) Current for each peripheral circuit

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
Current when PCLBUZ0 and EXSLK_RF are connected together and MCU supplies RF slow clock to RF	I_{PCEX} Note 1				1.0		μA
RTC operating current	I_{RTC} Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} is 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1				75.0		μA
Thermometer sensor operating current	I_{TMPS} Note 1				75.0		μA
LVD operating current	I_{LVI} Note 1, 7				0.08		μA
Flash self-programming operating current	I_{FSP} Notes 1, 9				2.50	12.20	mA
BGO current	I_{BGO} Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 10		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Notes 1. Current flowing to V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the XT1 oscillator). The value of the current value of the RL78 microcontroller is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. Also, add the value of IFIL in case of selecting low-speed on-chip oscillator. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

4. Current flowing only to the 12 bit interval timer (including the operating current of the low-speed on-chip oscillator). The current value of the MCU is the sum of I_{DD1} or I_{DD2} and I_{IT} when f_{CLK} = f_{SUB} when the watchdog timer operates in STOP mode. When using low-speed on-chip oscillator, add I_{FIL}.

5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the MCU is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.

6. Current flowing only to the A/D converter. The current value of MCU is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

7. Current flowing only to the LVD circuit. The current value of MCU is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit is in operation.

8. Current flowing when operates rewriting to Data flash.

9. Current flowing when operates flash self-programming.

10. Shift time to the SNOOZE mode is referred User's Manual: Hardware.

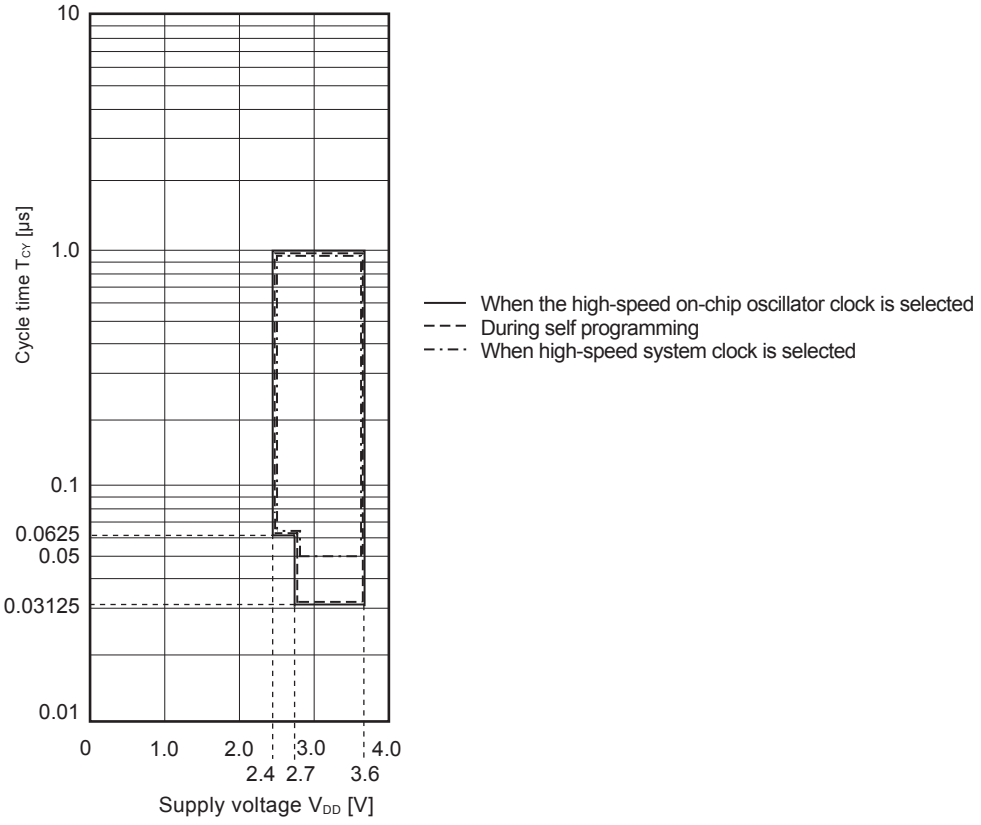
(**Remarks** are listed on the next page.)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) (2/2)

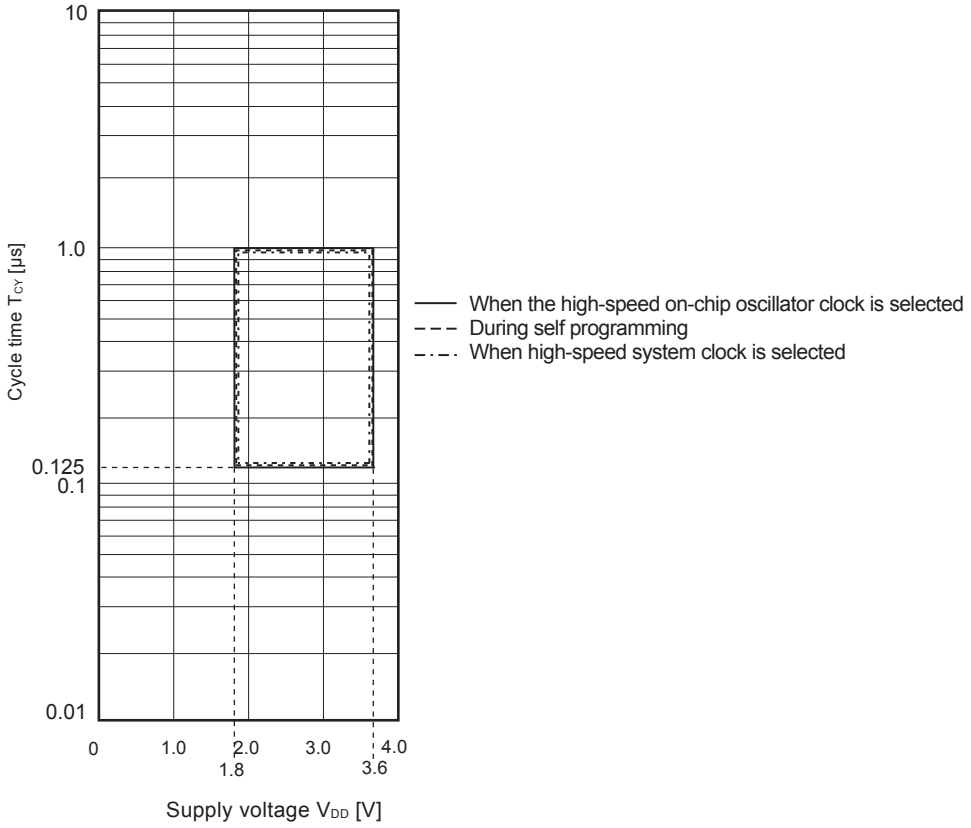
Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0, INTP3, INTP5, INTP6	1			µs
External PA control output High-level width	t_{PAHRF}	TXSELH_RF	283			µs
External PA control output low-level width	t_{PALRF}	TXSELL_RF	283			µs
$\overline{RESET}$ low-level width	t_{RSL}	$\overline{RESET}$	10			µs
$\overline{RESET\_RF}$ internal pin low-level width	t_{RSTLRF}	$\overline{RESET\_RF}$ internal pin	31			µs

Minimum Instruction Execution Time during Main System Clock Operation

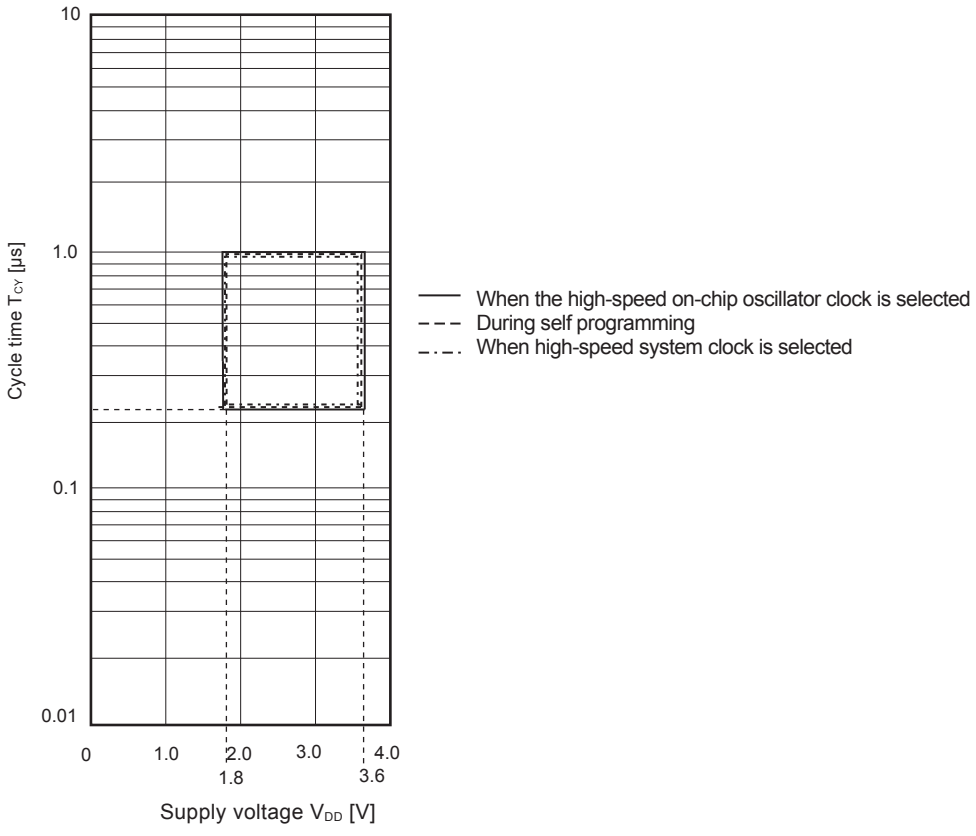
T_{CY} vs V_{DD} (HS (high-speed main) mode)



T_{CY} vs V_{DD} (LS (low-speed main) mode)



T_{CY} vs V_{DD} (LV (low-voltage main) mode)



(3) During communication at same potential (CSI mode) (Internal communication, supporting CSI21 only)

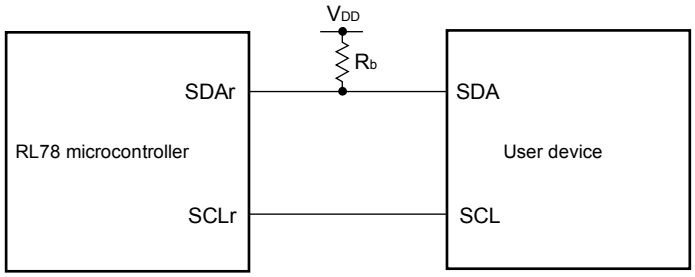
(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ $2/f_{CLK}$ Note	2.4 V ≤ V_{DD} ≤ 3.6 V	250		250		500		ns
			1.8 V ≤ V_{DD} ≤ 3.6 V	–		250		500		ns
			1.6 V ≤ V_{DD} ≤ 3.6 V	–		–		500		ns

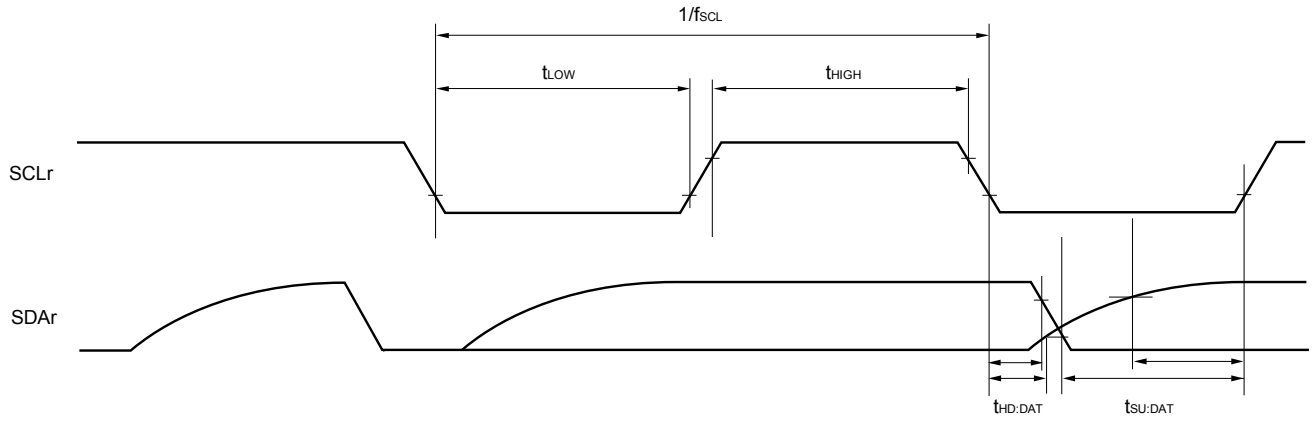
Note Use the f_{CLK} more than 6.5 MHz and lower than 24 MHz.

Remark This specification is for CSI21 only.

Simplified I²C mode mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remarks 1. R_b[Ω]:Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 20), g: PIM number (g =1), h: POM number (h = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clockw to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0), mn = 00, 02)

(7) Communication at different potential (1.8 V, 2.5 V) (UART mode)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode	LS (low-speed main) Mode	LV (low-voltage main) Mode	Unit
				MAX.	MAX.	MAX.	
Transfer rate		Reception	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V	f_{MCK}/6 Note 1	f_{MCK}/6 Note 1	f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3	5.3	1.3	0.6	Mbps
			2.4 V ≤ V_{DD} ≤ 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	f_{MCK}/6 Note 1	f_{MCK}/6 Note 1	f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3	2.6	1.3	0.6	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	–	f_{MCK}/6 Notes 1, 2	f_{MCK}/6 Notes 1, 2	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3	–	1.3	1.3	Mbps
		Transmission	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V	**Note 4**	**Note 4**	**Note 4**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V	1.2 Note 5	1.2 Note 5	1.2 Note 5	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	**Notes 2, 6**	**Notes 2, 6**	**Notes 2, 6**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V	0.43	0.43	0.43	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	–	**Notes 2, 6**	**Notes 2, 6**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V	–	0.43 Notes 7	0.43 Notes 7	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. Use it with $V_{DD} \geq V_b$.

3. Maximum operating frequency of CPU and peripheral hardware clock (f_{CLK}) is following

HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 3.6 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 3.6 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 3.6 V)
LV (low-voltage main) mode: 4 MHz (1.8 V ≤ V_{DD} ≤ 3.6 V)

4. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} ≤ 3.6 V and 2.3 V ≤ Vb ≤ 2.7 V

Maximum transfer rate = 1/{-Cb × Rb × ln (1 - 2.0/Vb)} × 3 [bps]

Baud rate error (theoretical value) =

(1/transfer rate × 2 - {-Cb × Rb × ln (1 - 2.0/Vb)} / (1/transfer rate) × number of transferred bits)

* This value is the theoretical value of the relative difference between the transmission and reception sides.

5. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 4 above to calculate the maximum transfer rate under conditions of the customer.

6. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8V ≤ V_{DD} < 3.3 V and 1.6 V ≤ Vb ≤ 2.0 V

(9) Communication at different potential (1.8 V, 2.5 V) (CSI mode: master mode, SCKp... internal clock output)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) (1/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK} 2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		1150		1150		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		1150		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	–		1150		1150		ns
SCKp high-level width Note 1	t_{KH1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2-170		t_{KCY1}/2-170		t_{KCY1}/2-170		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	t_{KCY1}/2-458		t_{KCY1}/2-458		t_{KCY1}/2-458		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	–		t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		ns
SCKp low-level width Note 1	t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 18		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	–		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
SIp setup time (to SCKp↑) Note 1, 2	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		479		479		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	479		479		479		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	–		479		479		ns
SIp hold time (from SCKp↑) Note 1, 2	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	–		19		19		ns

Notes 1. Supporting CSI00 and CSI20.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

3. Use it with V_{DD} ≥ V_b.

(Caution are listed on the next page.)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 135 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 100 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 100 pF, R_b = 5.5 kΩ	$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 100 pF, R_b = 5.5 kΩ	–		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 50 pF, R_b = 2.7 kΩ	0 Note 4	305	0 Note 4	305	0 Note 4	305	ns
		2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 100 pF, R_b = 2.7 kΩ	0 Note 4	355	0 Note 4	355	0 Note 4	355	ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 100 pF, R_b = 5.5 kΩ	0 Note 4	405	0 Note 4	405	0 Note 4	405	ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 100 pF, R_b = 5.5 kΩ	–	–	0 Note 4	405	0 Note 4	405	ns

Notes 1. The value must also be f_{MCK}/4 or lower.

2. Use it with $V_{DD} \geq V_b$.

3. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(2) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AVREFM/ANI1 (ADREFM = 1), conversion target : ANI16 to ANI19

(T_A = –40 to +85°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V		1.2	±5.0	LSB
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4		1.2	±8.5	LSB
Conversion time	T_{cony}	10-bit resolution	2.7 V ≤ V_{DD} ≤ 3.6 V	3.1875		39	µs
			1.8 V ≤ V_{DD} ≤ 3.6 V	17		39	µs
			1.6 V ≤ AV_{REFP} ≤ 3.6 V	57		95	µs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V			±0.35	%FSR
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4			±0.60	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V			±0.35	%FSR
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V			±3.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4			±6.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V			±2.0	LSB
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4			±2.5	LSB
Analog input voltage	V_{AIN}			0		AV_{REFP} and V_{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} < V_{DD}, MAX. value is following.

Overall error: ±4 LSB is added to the MAX. value of AV_{REFP} = V_{DD}.

Zero-scale error / Full-scale error: ±0.2 %FSR is added to the MAX. value of AV_{REFP} = V_{DD}.

Integral linearity error / Differential linearity error: ±2 LSB is added to the MAX. value n of AV_{REFP} = V_{DD}.

4. When the the conversion time is set to 57 µs (min.) and 95 µs (max.).

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), conversion target : ANI0 to ANI3, ANI16 to ANI19

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (–) = AV_{REFM} Note 4 = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	T_{cony}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V	17		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to 2.**8.2 Temperature sensor and internal reference voltage characteristics.**

4. When reference voltage (-) = V_{SS}, MAX. value is following.

Zero-scale error: ±0.35 %FSR is added to the MAX. value of reference voltage (–) = AV_{REFM}.

Integral linearity error: ±0.5 LSB is added to the MAX. value of reference voltage (–) = AV_{REFM}.

Differential linearity error: ±0.2 LSB is added to the MAX. value of reference voltage (–) = AV_{REFM}.

2.9.2 RF reception characteristics

Unless specified otherwise, the measurement is performed by our evaluation board.

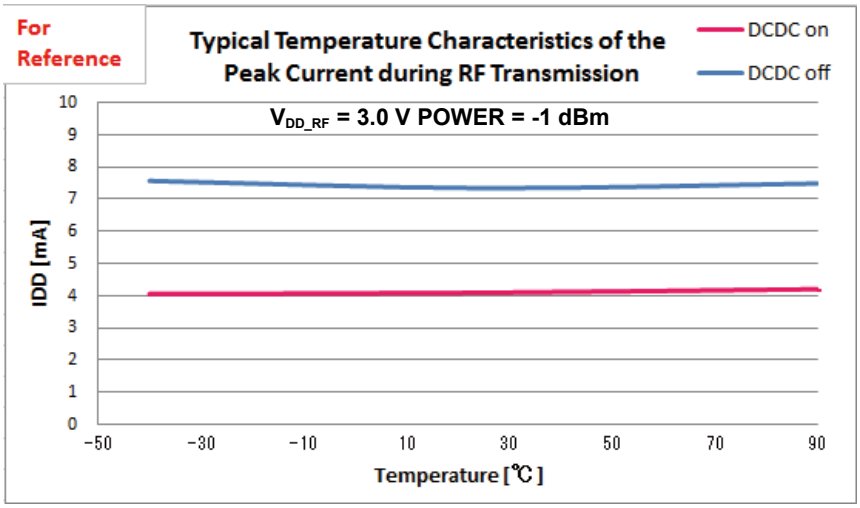
(T_A = +25°C, V_{DD} = V_{DD_RF} = AV_{DD_RF} = 3.0 V, f = 2440 MHz, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

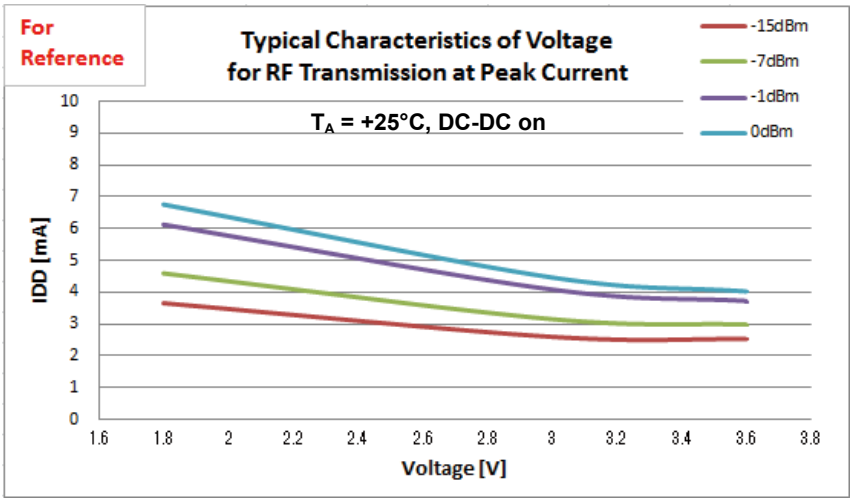
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RF input frequency	RF_{RXFRIN}			2402		2480	MHz
Maximum input level	RF_{LEVL}	PER ≤ 30.8% RF input pin	RF low power mode	-10	0	-	dBm
			RF normal mode	-10	1	-	dBm
			RF high performance mode	-10	1	-	dBm
Receiver sensitivity	RF_{STY}	PER ≤ 30.8%	RF low power mode	-	-60	-50	dBm
			RF normal mode	-	-90	-70	dBm
			RF high performance mode	-	-92	-70	dBm
Secondary radiation	RF_{RXSP}		30 MHz to 1 GHz	-	-72	-57	dBm/ 100 kHz
			1 GHz to 12 GHz	-	-57	-54	dBm/ 100 kHz
Common channel rejection ratio	RF_{CCR}	PER ≤ 30.8%, Prf = –67dBm		-21	-12	-	dB
Adjacent channel rejection ratio	RF_{ADCR}	PER ≤ 30.8% Prf = –67 dBm	±1 MHz	-15	-5	-	dB
			±2 MHz	17	29	-	dB
			±3 MHz	27	34	-	dB
Blocking	RF_{BLK}	PER ≤ 30.8% Prf = –67 dBm	30 MHz - 2000 MHz	-30	-13	-	dB
			2000 MHz to 2399 MHz	-35	-30	-	dBm
			2484 MHz to 3000 MHz	-35	-30	-	dBm
			> 3000 MHz	-30	-17	-	dBm
Frequency tolerance	RF_{RXFERR}	PER ≤ 30.8%		-250		+250	kHz
RSSI accuracy	RF_{RSSIS}	T_A = +25°C, –70 dBm ≤ Prf ≤ –10 dBm		-4	0	4	dB

2.9.3 Performance mapping for typical RF (Reference)

(1) Peak Current during RF Transmission

Unless specified otherwise, the measurement is performed by our evaluation board.
Current consumption is not including MCU unit.





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