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What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11agganb-20

● ROM, RAM capacities

Flash ROM	Data Flash	RAM	RL78/G1D
128 KB	8 KB	12 KB	R5F11AGG
192 KB	8 KB	16 KB	R5F11AGH
256 KB	8 KB	20 KB[Note]	R5F11AGJ

Note 19 KB when the self-programming function is used.

1.5 Block Diagram
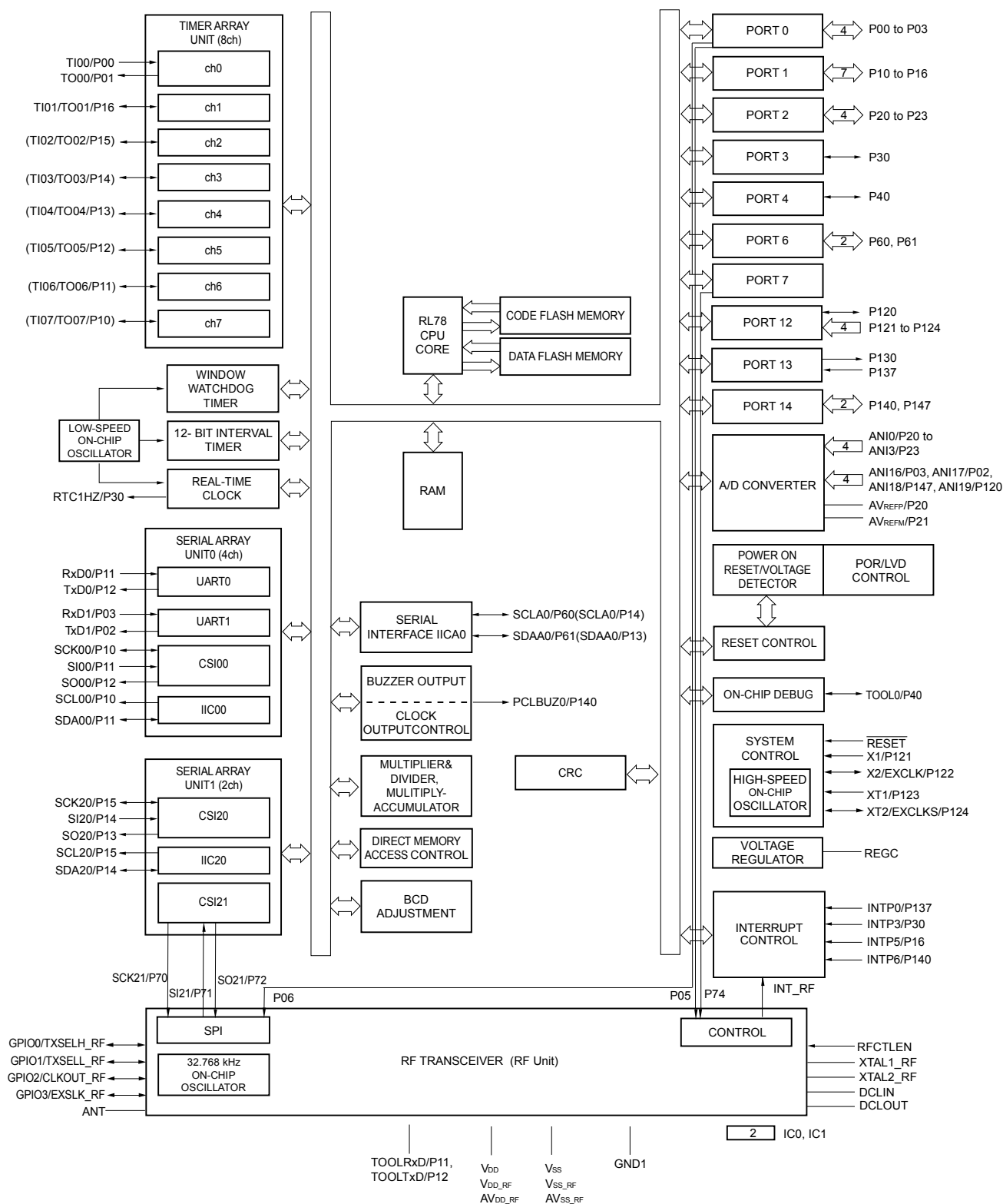
Remark   Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

Caution   **P00, P02, P03, and P10 to P15 do not output high level in N-ch open-drain mode.**

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.4.2 Input current

$(T_A = -40$ to $+85°C$, 1.6 V $\leq V_{DD} = V_{DD\_RF} = AV_{DD\_RF} \leq 3.6$ V, $V_{SS} = V_{SS\_RF} = AV_{SS\_RF} = 0$ V$)$

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	Normal mode ($I_{THL} = 1$)	$0.8V_{DD}$		V_{DD}	V
	V_{IH2}	P01, P03, P10, P11, P13, P14, P15, P16	TTL mode 3.3 V $\leq V_{DD} \leq$ 3.6 V	2.0		V_{DD}	V
			TTL mode 1.6 V $\leq V_{DD} <$ 3.3V	1.5		V_{DD}	V
	V_{IH3}	P20, P21, P22, P23		$0.7V_{DD}$		V_{DD}	V
	V_{IH4}	P60, P61		$0.7V_{DD}$		6.0	V
	V_{IH5}	P121, P122, P123, P124, P137, $\overline{RESET}$		$0.8V_{DD}$		V_{DD}	V
	V_{IHRF}	GPIO0, GPIO1, GPIO2, GPIO3		$0.85V_{DD\_RF}$		V_{DD_RF}	V
Input voltage, low	V_{IL1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P140, P147	Normal mode ($I_{THL} = 1$)	0		$0.2V_{DD}$	V
	V_{IL2}	P01, P03, P10, P11, P13, P14, P15, P16	TTL mode 3.3 V $\leq V_{DD} \leq$ 3.6 V	0		0.5	V
			TTL mode 1.6 V $\leq V_{DD} <$ 3.3V	0		0.32	V
	V_{IL3}	P20, P21, P22, P23		0		$0.3V_{DD}$	V
	V_{IL4}	P60, P61		0		$0.3V_{DD}$	V
	V_{IL5}	P121, P122, P123, P124, P137, $\overline{RESET}$		0		$0.2V_{DD}$	V
	V_{ILRF}	GPIO0, GPIO1, GPIO2, GPIO3		0		$0.1V_{DD\_RF}$	V

Caution   **The maximum value of V_{IH} of pins P00, P02, P03, and P10 to P15 is V_{DD}, even in the N-ch open-drain mode.**

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Notes 1. Current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed system clock and subsystem clock are stopped.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1). Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
   HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz
   2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz
   LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 8 MHz
   LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 4 MHz

6. The upper value is for square-wave input and the lower is with an oscillator connected.

Remarks 1. f_{MX}:   High-speed system clock frequency (External main system clock frequency)

2. f_{IH}:   High-speed on-chip oscillator clock frequency

3. f_{SUB}:   Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

Notes 1. Current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz

2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 8 MHz

LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 4 MHz

8. If operation of the subsystem clock when STOP mode, same as when HALT mode of subsystem clock operation.

9. The upper value is for square-wave input and the lower is with an oscillator connected.

Remarks 1. f_{MX}:   High-speed system clock frequency (External main system clock frequency)

2. f_{IH}:   High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(3) Current for each peripheral circuit

$(T_A = -40$ to $+85°C$, 1.6 V $\leq V_{DD} = V_{DD\_RF} = AV_{DD\_RF} \leq 3.6$ V, $V_{SS} = V_{SS\_RF} = AV_{SS\_RF} = 0$ V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} [Note 1]				0.20		μA
Current when PCLBUZ0 and EXSLK_RF are connected together and MCU supplies RF slow clock to RF	I_{PCEX} [Note 1]				1.0		μA
RTC operating current	I_{RTC} [Notes 1, 2, 3]				0.02		μA
12-bit interval timer operating current	I_{IT} [Notes 1, 2, 4]				0.02		μA
Watchdog timer operating current	I_{WDT} [Notes 1, 2, 5]	f_{IL} is 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} [Notes 1, 6]	When conversion at maximum speed	$AV_{REFP} = V_{DD} = 3.0$ V		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} [Note 1]				75.0		μA
Thermometer sensor operating current	I_{TMPS} [Note 1]				75.0		μA
LVD operating current	I_{LVI} [Note 1, 7]				0.08		μA
Flash self-programming operating current	I_{FSP} [Notes 1, 9]				2.50	12.20	mA
BGO current	I_{BGO} [Notes 1, 8]				2.50	12.20	mA
SNOOZE operating current	I_{SNOZ} [Note 1]	ADC operation	The mode is performed [Note 10]		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, $AV_{REFP} = V_{DD} = 3.0$ V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Notes **1.** Current flowing to V_{DD}.

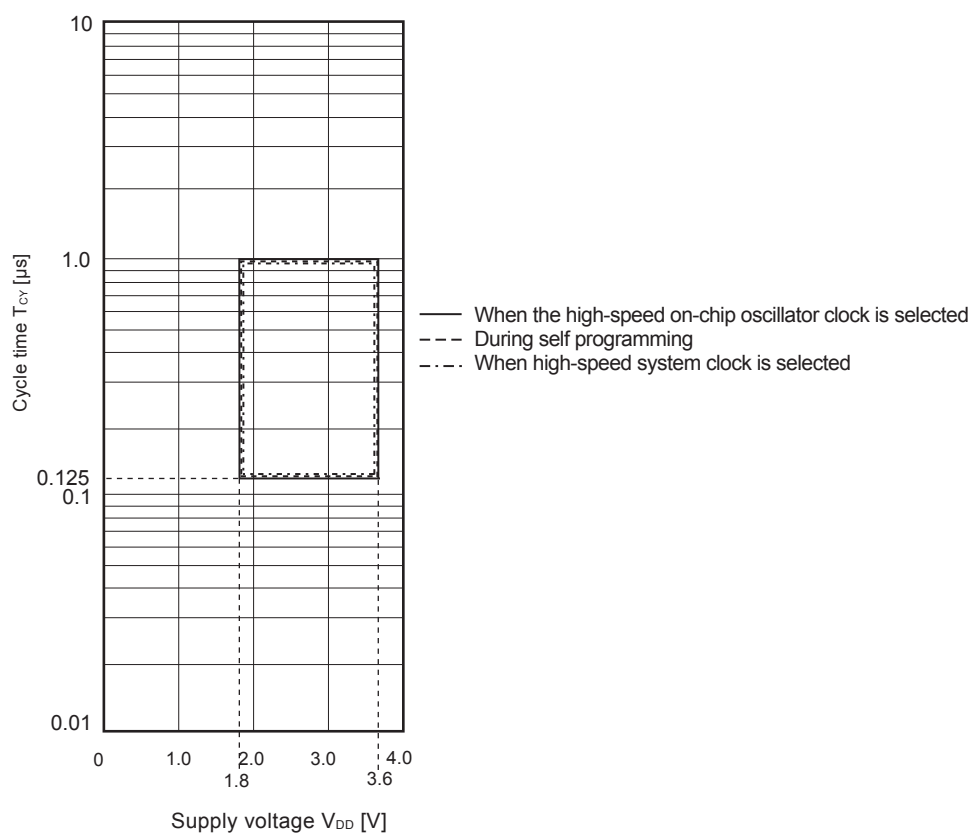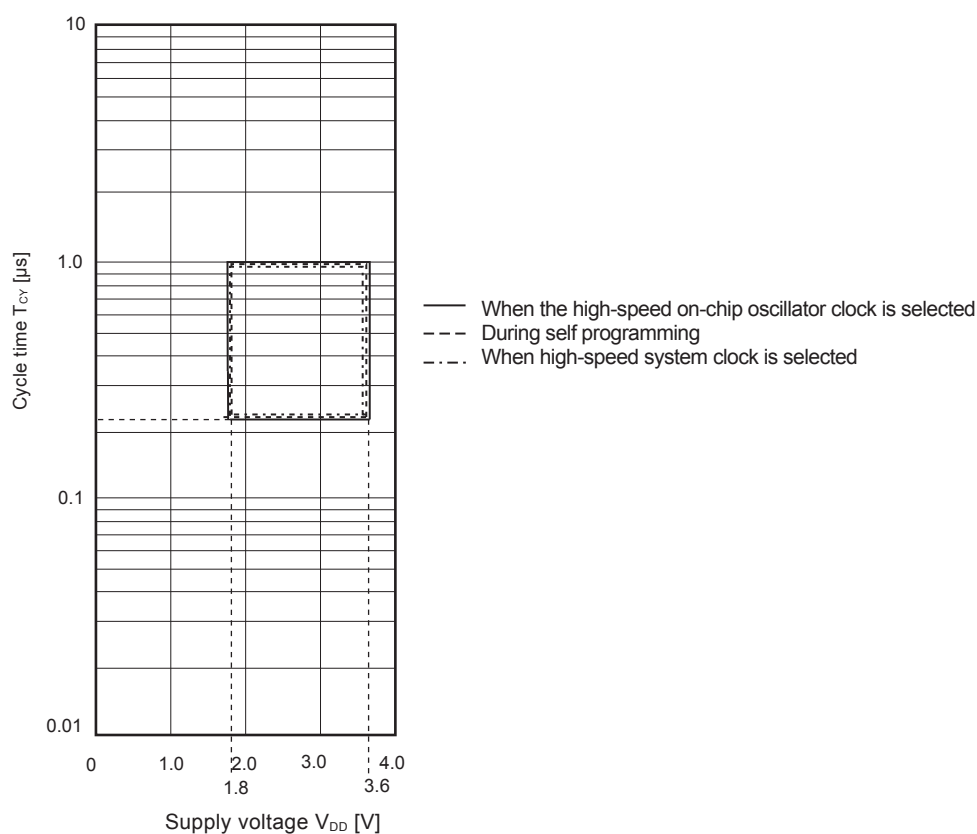   **2.** When high speed on-chip oscillator and high-speed system clock are stopped.

      3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the XT1 oscillator). The value of the current value of the RL78 microcontroller is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. Also, add the value of IFIL in case of selecting low-speed on-chip oscillator. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

      4. Current flowing only to the 12 bit interval timer (including the operating current of the low-speed on-chip oscillator). The current value of the MCU is the sum of I_{DD1} or I_{DD2} and I_{IT} when $f_{CLK} = f_{SUB}$ when the watchdog timer operates in STOP mode. When using low-speed on-chip oscillator, add I_{FIL}.

      5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the MCU is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.

      6. Current flowing only to the A/D converter. The current value of MCU is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

      7. Current flowing only to the LVD circuit. The current value of MCU is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit is in operation.

      8. Current flowing when operates rewriting to Data flash.

      9. Current flowing when operates flash self-programming.
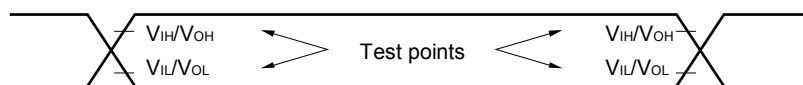
      10. Shift time to the SNOOZE mode is referred User's Manual: Hardware.

   (**Remarks** are listed on the next page.)

T_{CY} vs V_{DD} (LS (low-speed main) mode)

- —— When the high-speed on-chip oscillator clock is selected
- --- During self programming
- -·-· When high-speed system clock is selected

Supply voltage V_{DD} [V]

T_{CY} vs V_{DD} (LV (low-voltage main) mode)

- —— When the high-speed on-chip oscillator clock is selected
- --- During self programming
- -·-· When high-speed system clock is selected

Supply voltage V_{DD} [V]

2.7 Peripheral Functions Characteristics

AC Timing Test Points

2.7.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode	LS (low-speed main) Mode	LV (low-voltage main) Mode	Unit
				MAX.	MAX.	MAX.	
Transfer rate [Note 1]		2.4 V ≤ V_{DD} ≤ 3.6 V		$f_{MCK}/6$	$f_{MCK}/6$	$f_{MCK}/6$	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ [Note 2]	5.3	1.3	0.6	Mbps
		1.8 V ≤ V_{DD} ≤ 3.6 V		–	$f_{MCK}/6$	$f_{MCK}/6$	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ [Note 2]	–	1.3	0.6	Mbps
		1.6 V ≤ V_{DD} ≤ 3.6 V		–	–	$f_{MCK}/6$	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ [Note 2]	–	–	0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** Maximum operating frequency of CPU and peripheral hardware clock (f_{CLK}) is following

HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 3.6 V)

16 MHz (2.4 V ≤ V_{DD} ≤ 3.6 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 3.6 V)

LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 3.6 V)

Caution   Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)
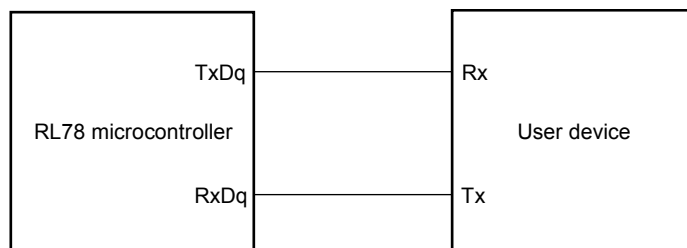
UART mode bit width (during communication at same potential) (reference)
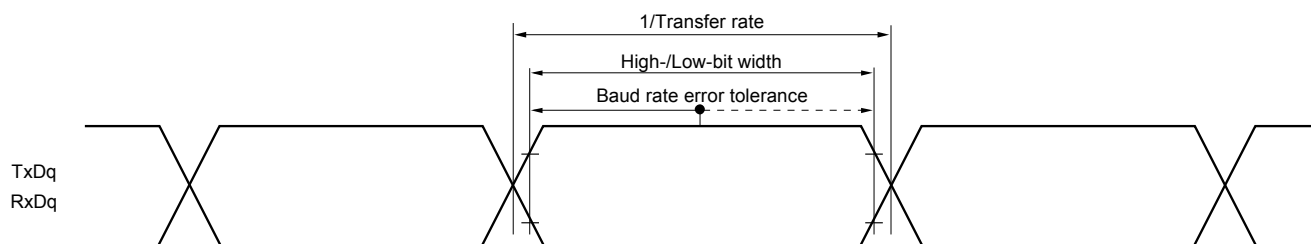
Remarks 1. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

   2. f_{MCK}: Serial array unit operation clock frequency
      (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
      m: Unit number, n: Channel number (mn = 00, 01))

(3) During communication at same potential (CSI mode) (Internal communication, supporting CSI21 only)

(T$_A$ = –40 to +85°C, 1.6 V ≤ V$_{DD}$ = V$_{DD\_RF}$ = AV$_{DD\_RF}$ ≤ 3.6 V, V$_{SS}$ = V$_{SS\_RF}$ = AV$_{SS\_RF}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ ≥ 2/f$_{CLK}$ Note	2.4 V ≤ V$_{DD}$ ≤ 3.6 V	250		250		500		ns
			1.8 V ≤ V$_{DD}$ ≤ 3.6 V	–		250		500		ns
			1.6 V ≤ V$_{DD}$ ≤ 3.6 V	–		–		500		ns

Note Use the f$_{CLK}$ more than 6.5 MHz and lower than 24 MHz.

Remark This specification is for CSI21 only.

(4) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, supporting CSI00 and CSI20)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq$ 4/ f_{CLK}	2.7 V ≤ V_{DD} ≤ 3.6 V	125		500		1000		ns
			2.4 V ≤ V_{DD} ≤ 3.6 V	250		500		1000		ns
			1.8 V ≤ V_{DD} ≤ 3.6 V	–		500		1000		ns
			1.6 V ≤ V_{DD} ≤ 3.6 V	–		–		1000		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V		$t_{KCY1}/2 - 18$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		$t_{KCY1}/2 - 38$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		$t_{KCY1}/2 - 100$		ns
SIp setup time (to SCKp↑) [Note 1]	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V		44		110		110		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		75		110		110		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		110		110		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		220		ns
SIp hold time (from SCKp↑) [Note 1]	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V		19		19		19		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		19		19		19		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		19		19		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		19		ns
Delay time from SCKp↓ to SOp output [Note 2]	t_{KSO1}	C = 30 pF [Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V		25		25		25	ns
			2.4 V ≤ V_{DD} ≤ 3.6 V		25		25		25	ns
			1.8 V ≤ V_{DD} ≤ 3.6 V		–		25		25	ns
			1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
   2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
   3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 10), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1),
      g: PIM and POM numbers (g = 0, 1)
   2. f_{MCK}: Serial array unit operation clock frequency
      (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 11))

RENESAS

(6)　During communication at same potential (simplified I^{2}C mode)　(1/2)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		400 Note 1		400 Note 1	kHz
		2.4 V ≤ V_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ V_{DD} < 3.6 V, C_b = 100 pF, R_b = 3 kΩ		–		400 Note 1		400 Note 1	kHz
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		–		300 Note 1		300 Note 1	kHz
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		–		–		250 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ V_{DD} < 3.6 V, C_b = 100 pF, R_b = 3 kΩ	–		1150		1150		ns
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	–		1550		1550		ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–		–		1850		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ V_{DD} < 3.6 V, C_b = 100 pF, R_b = 3 kΩ	–		1150		1150		ns
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	–		1550		1550		ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–		–		1850		ns

(**Notes**, **Caution**, and **Remarks** are listed on the page after the next page.)

RENESAS

(8) Communication at different potential (2.5 V) (CSI mode) (master mode: SCKp... internal clock output, supporting CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

| Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 2/f_{CLK} 2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	t_{KH1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 120		t_{KCY1}/2 – 120		t_{KCY1}/2 – 120		ns
SCKp low-level width	t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 10		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
SIp setup time (to SCKp↑) [Note 1]	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	121		479		479		ns
SIp hold time (from SCKp↑) [Note 1]	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↓ to SOp output [Note 1]	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ		130		130		130	ns
SIp setup time (to SCKp↓) [Note 2]	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	33		110		110		ns
SIp hold time (from SCKp↓) [Note 2]	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↑ to SOp output [Note 2]	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ		10		10		10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
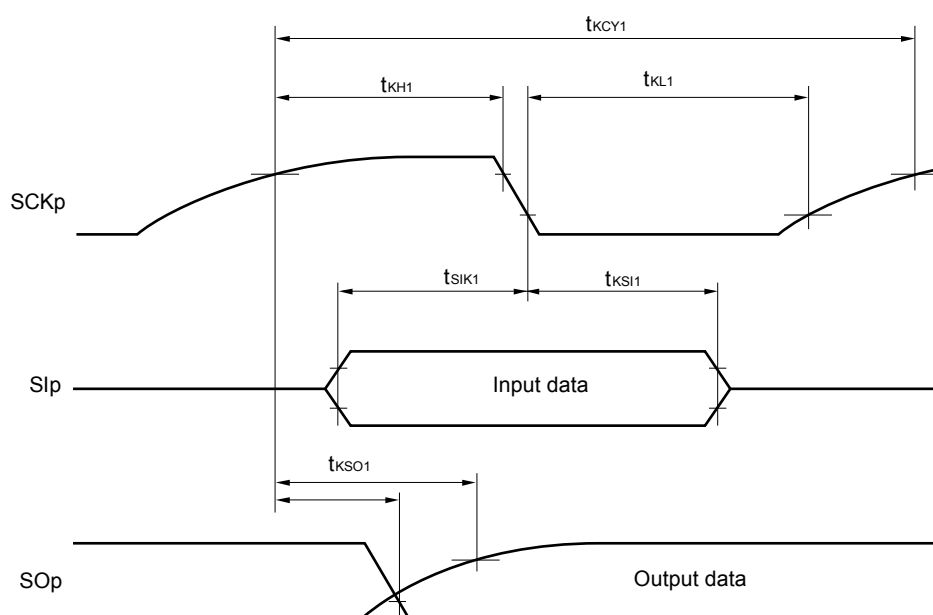
Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]:Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
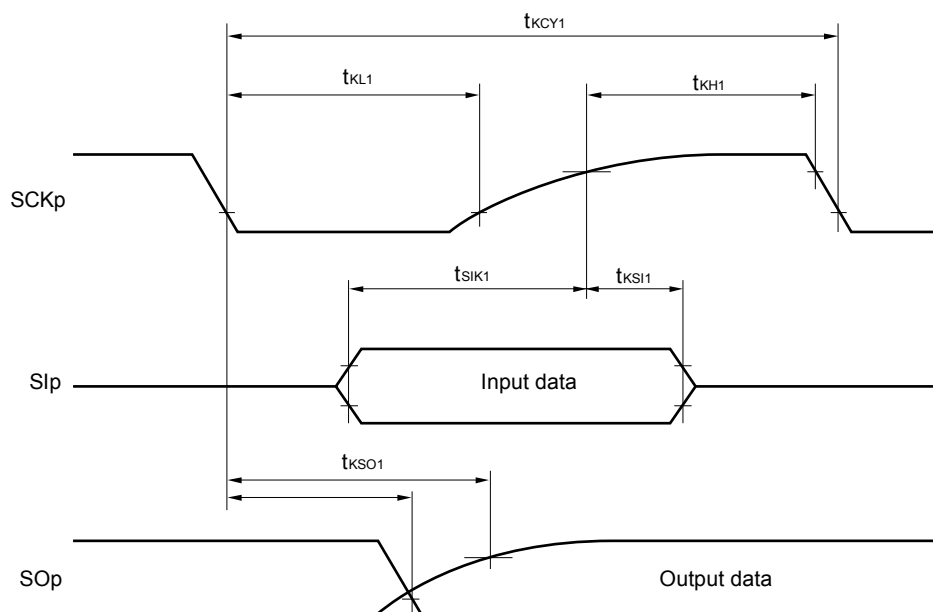
CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

(T$_A$ = –40 to +85°C, 1.8 V ≤ V$_{DD}$ = V$_{DD\_RF}$ = AV$_{DD\_RF}$ ≤ 3.6 V, V$_{SS}$ = V$_{SS\_RF}$ = AV$_{SS\_RF}$ = 0 V) (2/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	2.7 V ≤ V$_{DD}$ ≤ 3.6 V 2.3 V ≤ V$_b$ ≤ 2.7 V	t$_{KCY2}$/2 – 18		t$_{KCY2}$/2 – 50		t$_{KCY2}$/2 – 50		ns
		2.4 V ≤ V$_{DD}$ < 3.3 V 1.6 V ≤ V$_b$ ≤ 2.0 V	t$_{KCY2}$/2 – 50		t$_{KCY2}$/2 – 50		t$_{KCY2}$/2 – 50		ns
		1.8 V ≤ V$_{DD}$<3.3 V 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]	–		t$_{KCY2}$/2 – 50		t$_{KCY2}$/2 – 50		ns
SIp setup time (to SCKp↑) [Note 3]	t$_{SIK2}$	2.7 V ≤ V$_{DD}$ ≤ 3.6 V 2.3 V ≤ V$_b$ ≤ 4.0 V	1/f$_{MCK}$ + 20		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		ns
		2.4 V ≤ V$_{DD}$ < 3.3 V 1.6 V ≤ V$_b$ ≤ 2.0 V	1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		ns
		1.8 V ≤ V$_{DD}$<3.3 V 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]	–		1/f$_{MCK}$ + 30		1/f$_{MCK}$ + 30		ns
SIp hold time (from SCKp↑) [Note 3]	t$_{KSI2}$	2.7 V ≤ V$_{DD}$ ≤ 3.6 V 2.3 V ≤ V$_b$ ≤ 4.0 V	1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		ns
		2.4 V ≤ V$_{DD}$ < 3.3 V 1.6 V ≤ V$_b$ ≤ 2.0 V	1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		ns
		1.8 V ≤ V$_{DD}$<3.3 V 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]	–		1/f$_{MCK}$ + 31		1/f$_{MCK}$ + 31		ns
Delay time from SCKp↓ to SOp output [Note 4]	t$_{KSO2}$	2.7 V ≤ V$_{DD}$ < 3.6 V 2.3 V ≤ V$_b$ ≤ 2.7 V C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		2/f$_{MCK}$ + 214		2/f$_{MCK}$ + 573		2/f$_{MCK}$ + 573	ns
		2.4 V ≤ V$_{DD}$ < 3.3 V 1.6 V ≤ V$_b$ ≤ 2.0 V C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		2/f$_{MCK}$ + 573		2/f$_{MCK}$ + 573		2/f$_{MCK}$ + 573	ns
		1.8 V ≤ V$_{DD}$< 3.3 V 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2] C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		–		2/f$_{MCK}$ + 573		2/f$_{MCK}$ + 573	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

2. Use it with V$_{DD}$ ≥ V$_b$.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution **Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V$_{DD}$ tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

Simplified I^{2}C mode connection diagram (during communication at different potential)
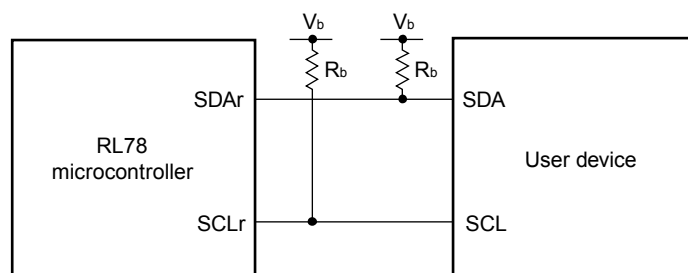
Simplified I^{2}C mode serial transfer timing (during communication at different potential)
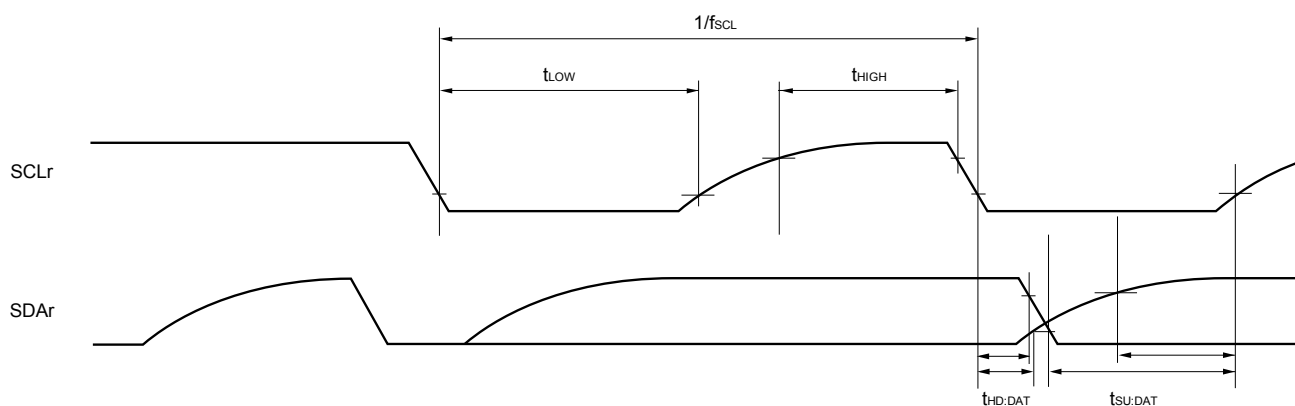
Remarks 1. $R_b[\Omega]$:Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage

2. r: IIC number (r = 00, 10), g: PIM, POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02))

2.8.2 Temperature sensor and internal reference voltage characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V, HS (high-speed main) mode)

| Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}		5			µs

2.8.3 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Rise time	1.47	1.51	1.55	V
	V_{PDR}	Fall time	1.46	1.50	1.54	V
Minimum pulse width[Note]	T_{PW}	Other than STOP/SUB_RUN/SUB_HALT	300			µs

Note This is the time required for the POR circuit to execute a reset operation when V_{DD} falls below V_{PDR}. When the main system clock (f_{MAIN}) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC) or when the microcontroller enters STOP mode, this is the time required for the POR circuit to execute a reset operation between when V_{DD} falls below 0.7 V and when V_{DD} rises to V_{POR} or higher.

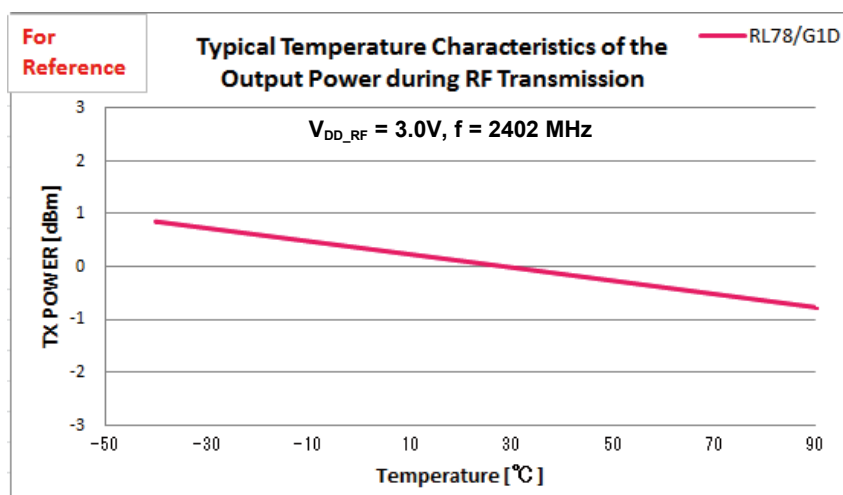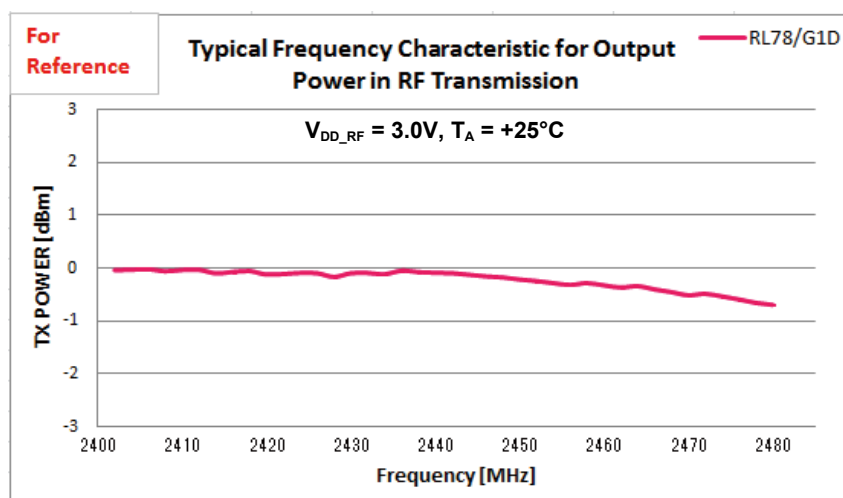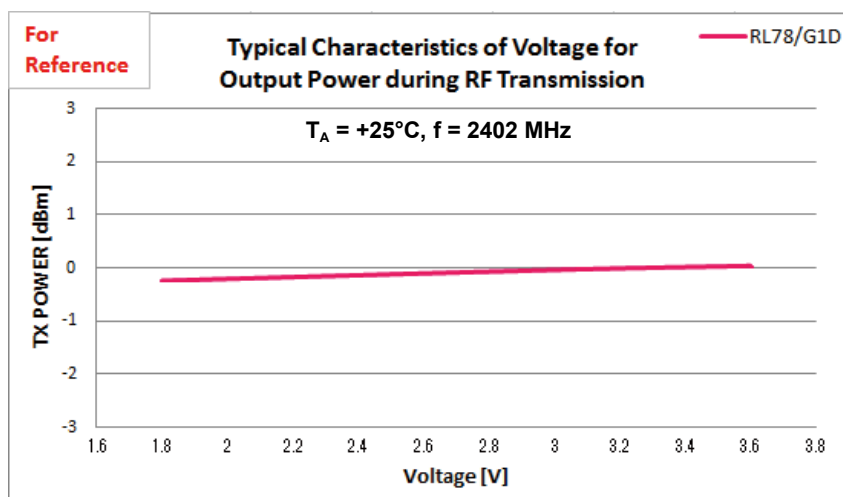Typical Characteristics of Voltage for RF Reception at Peak Current
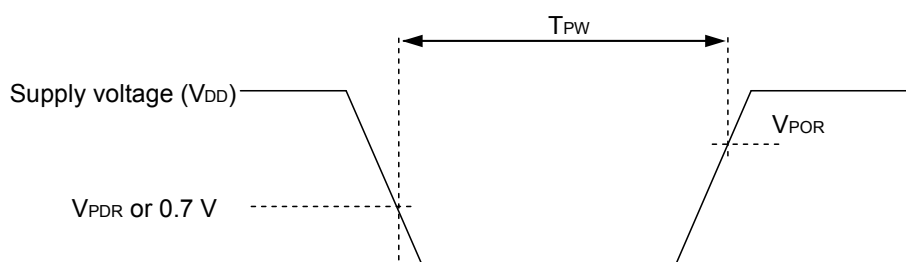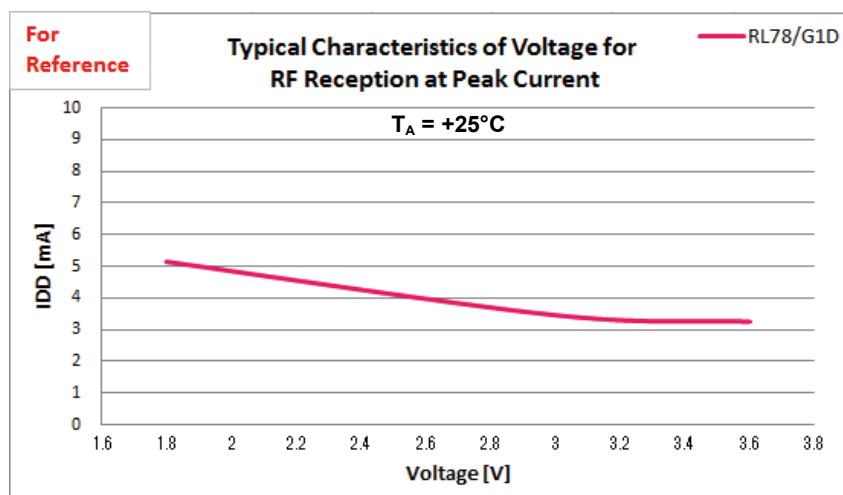
(3) RF Output Power during Transmission

Unless specified otherwise, the measurement is performed by our evaluation board.

Current consumption is not including MCU unit.

Typical Temperature Characteristics of the Output Power during RF Transmission

Typical Characteristics of Voltage for Output Power during RF Transmission
RL78/G1D
T_A = +25°C, f = 2402 MHz

Typical Frequency Characteristic for Output Power in RF Transmission
RL78/G1D
V_{DD_RF} = 3.0V, T_A = +25°C

3. PACKAGE DRAWINGS

3.1 48-pin plastic WQFN (6 × 6)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-HWQFN48-6x6-0.40	PWQN0048LB-A	-	0.07

Unit: mm

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	5.90	6.00	6.10
E	5.90	6.00	6.10
A	-	-	0.80
A_1	0.00	-	-
b	0.15	0.20	0.25
$\boxed{e}$	-	0.40	-
L_P	0.20	0.30	0.40
x	-	-	0.05
y	-	-	0.05
Z_D	-	0.80	-
Z_E	-	0.80	-
c	-	0.20	-
D_2	-	4.73	-
E_2	-	4.73	-