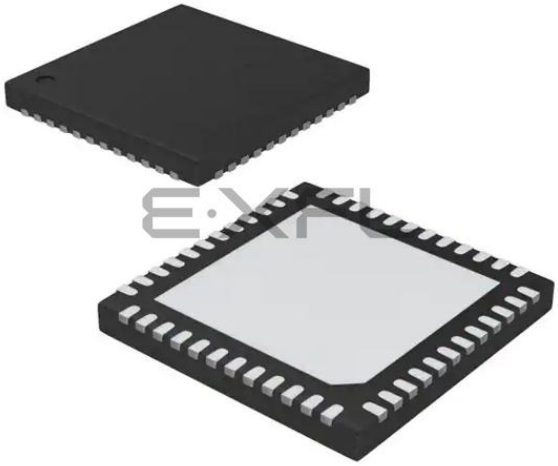

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11agganb-40

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G1D

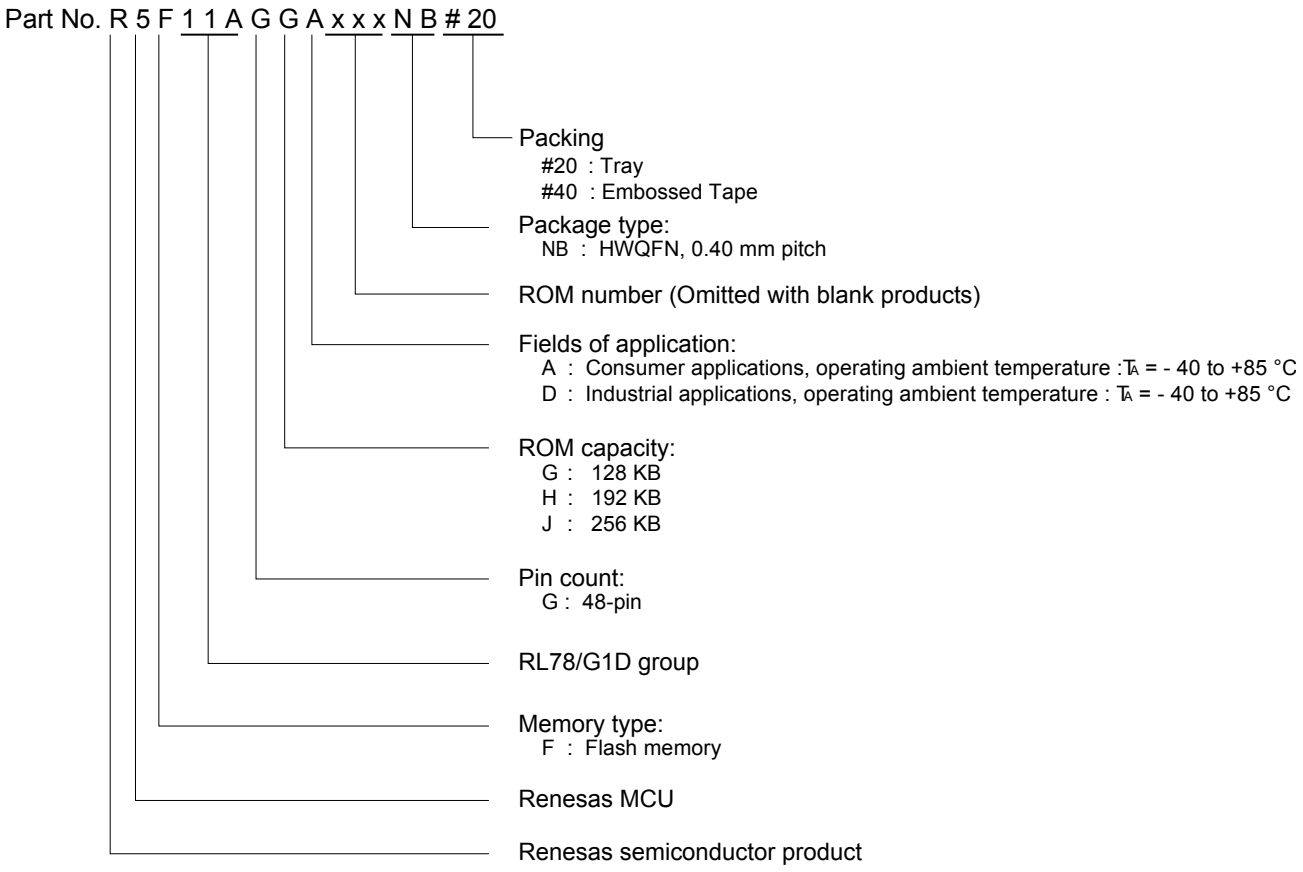


Table 1-1. List of Ordering Part Numbers

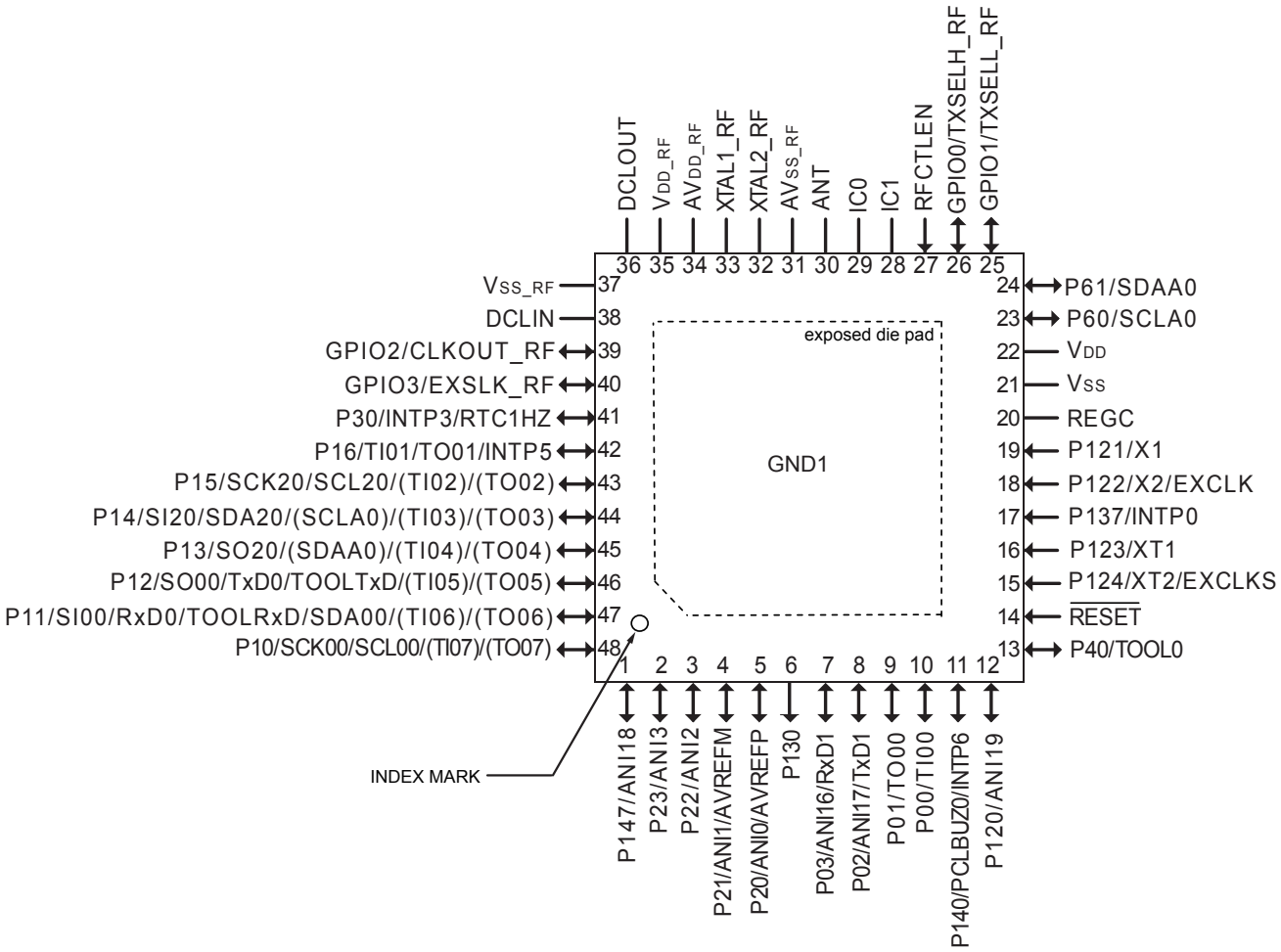
Pin count	Package	Fields of Application[Note]	Ordering Part Number	Code Flash Memory	Data Flash Memory
48 pins	Plastic WQFN (6 × 6)	A	R5F11AGGANB#20 R5F11AGGANB#40	128 KB	8 KB
		D	R5F11AGGDNB#20 R5F11AGGDNB#40		
		A	R5F11AGHANB#20 R5F11AGHANB#40	192 KB	8 KB
		D	R5F11AGHDNB#20 R5F11AGHDNB#40		
		A	R5F11AGJANB#20 R5F11AGJANB#40	256 KB	8 KB
		D	R5F11AGJDNB#20 R5F11AGJDNB#40		

Note For the fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/G1D**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

<R> ● 48-pin plastic WQFN (6 × 6 mm, 0.4 mm pitch)



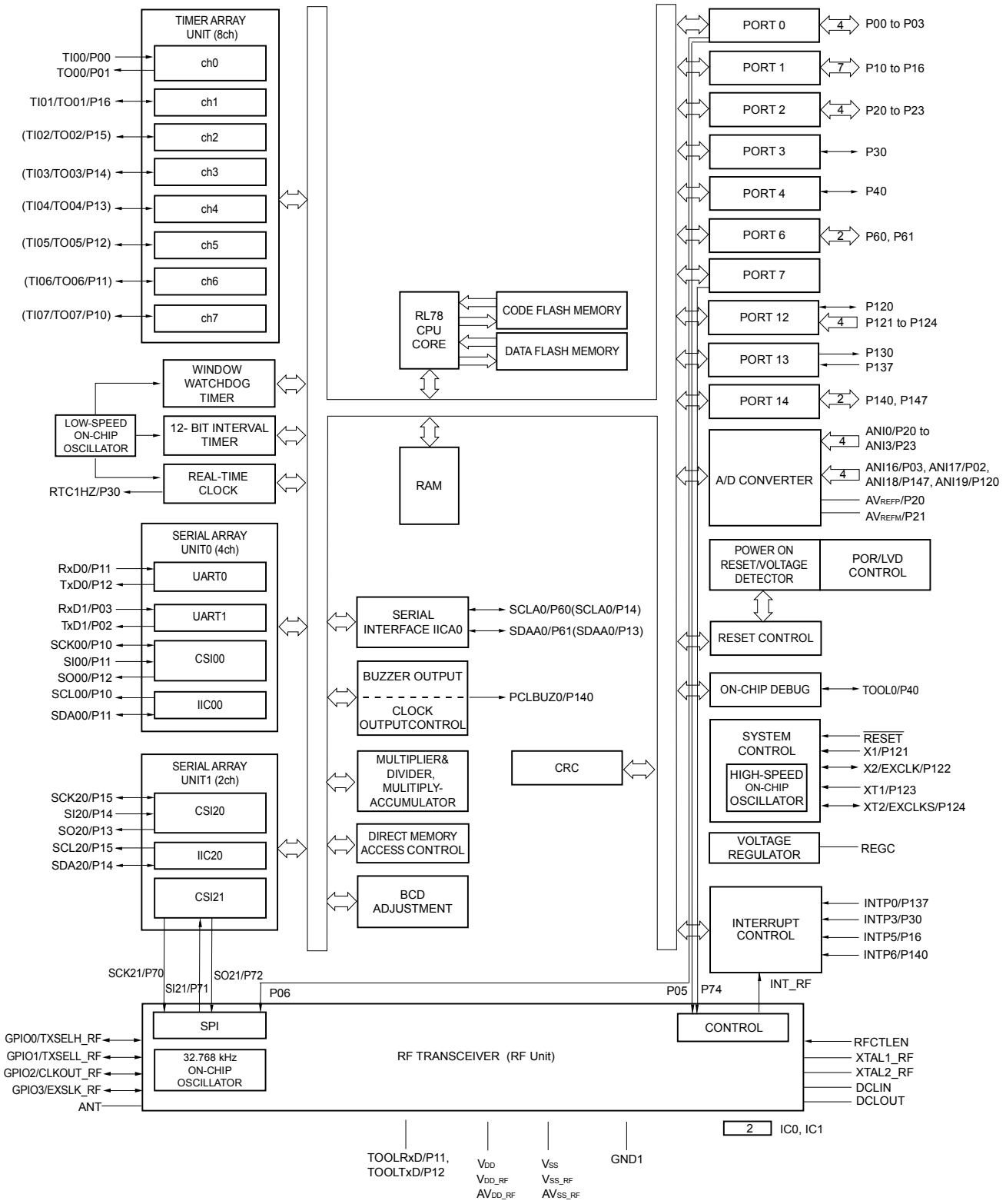
Cautions 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).

2. Connect the metal pad (GND1) on the back of the package that has the same potential as AV_{SS_RF}.

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)..

1.5 Block Diagram



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	(This is applicable to all pins listed below.)	–40	mA
		Total of all pins –170mA	P00, P01, P02, P03, P40, P120, P130, P140	–70	mA
			P10, P11, P12, P13, P14, P15, P16, P30, P147	–100	mA
	I_{OH2}	Per pin	(This is applicable to all pins listed below.)	–0.5	mA
		Total of all pins	P20, P21, P22, P23	–2	mA
	I_{OHMRF}	Per pin	GPIO0, GPIO1, GPIO2, GPIO3	–17	mA
Output current, low	I_{OL1}	Per pin	(This is applicable to all pins listed below.)	40	mA
		Total of all pins 170mA	P00, P01, P02, P03, P40, P120, P130, P140	70	mA
			P10, P11, P12, P13, P14, P15, P16, P30, P60, P61, P147	100	mA
	I_{OL2}	Per pin	(This is applicable to all pins listed below.)	1	mA
		Total of all pins	P20, P21, P22, P23	5	mA
	I_{OLRF}	Per pin	GPIO0, GPIO1, GPIO2, GPIO3	17	mA
Operating ambient temperature	T_A	In normal operation mode		–40 to +85	°C
		In flash memory programming mode		–40 to +85	°C
Storage temperature	Tstg			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. Reference voltage is V_{SS}.

2.2 Operating Voltage

(T_A = –40 to +85°C, V_{DD} = V_{DD_RF} = AV_{DD_RF}, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Clock generator		Flash operation mode	Operation voltage	CPU operation clocks (f_{CLK})[Note 1]
Main system clock (f_{MAIN})	High-speed on-chip oscillator (f_{IH})	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 32 MHz
			2.4 V ≤ V_{DD} < 2.7 V	1 MHz to 16 MHz
		LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 8 MHz
		LV (low-voltage main) mode[Note 2]	1.6 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 4 MHz
	X1 clock oscillator (f_X)	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 20 MHz
		LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 8 MHz
		LV (low-voltage main) mode[Note 2]	1.6 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 4 MHz
	External main system clock (f_{EX})	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 20 MHz
			2.4 V ≤ V_{DD} < 2.7 V	1 MHz to 16 MHz
		LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 8 MHz
		LV (low-voltage main) mode[Note 2]	1.6 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 4 MHz
Subsystem clock (f_{SUB})	XT1 clock oscillator (f_{XT})	–	1.6 V ≤ V_{DD} ≤ 3.6 V	32.768 kHz
	External subsystem clock (f_{EXT})	–	1.6 V ≤ V_{DD} ≤ 3.6 V	32.768 kHz

Notes 1. Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time.Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

2. This mode is prohibited to use in case of using DC-DC converter.

2.4 DC Characteristics

2.4.1 Output current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			–10.0[Note 2]	mA
		P00, P01, P02, P03, P40, P120, P130, P140	Total[Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V			–10.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			–5.0	mA
				1.6 V ≤ V_{DD} < 1.8 V			–2.5	mA
		P10, P11, P12, P13, P14, P15, P16, P30, P147	Total[Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V			–19.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			–10.0	mA
				1.6 V ≤ V_{DD} < 1.8 V			–5.0	mA
		Total of all pins[Note 3]		1.6 V ≤ V_{DD} ≤ 3.6 V			–135.0[Note 4]	mA
	I_{OH2}	P20, P21, P22, P23	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			–0.1[Note 2]	mA
			Total[Note 3]	1.6 V ≤ V_{DD} ≤ 3.6 V			–1.5	mA
	I_{OHRF}	GPIO0, GPIO1, GPIO2, GPIO3	Per pin	1.6 V ≤ V_{DD_RF} ≤ 3.6 V			–2.0	mA
Output current, low[Note 1]	I_{OL1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			20.0[Note 2]	mA
		P60, P61	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			15.0[Note 2]	mA
		P00, P01, P02, P03, P40, P120, P130, P140	Total[Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V			15.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
				1.6 V ≤ V_{DD} < 1.8 V			4.5	mA
		P10, P11, P12, P13, P14, P15, P16, P30, P60, P61, P147	Total[Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V			35.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			20.0	mA
				1.6 V ≤ V_{DD} < 1.8 V			10.0	mA
		Total of all pins[Note 3]		1.6 V ≤ V_{DD} ≤ 3.6 V			150.0	mA
	I_{OL2}	P20, P21, P22, P23	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			0.4[Note 2]	mA
			Total[Note 3]	1.6 V ≤ V_{DD} ≤ 3.6 V			5.0	mA
	I_{OLRF}	GPIO0, GPIO1, GPIO2, GPIO3	Per pin	1.6 V ≤ V_{DD_RF} ≤ 3.6 V			2.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 50% and I_{OH} = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(50 × 0.01) = –14.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. Product for industrial applications (R5F11AGGDNB, R5F11AGHDNB, R5F11AGJDNB) is –100.0 mA.

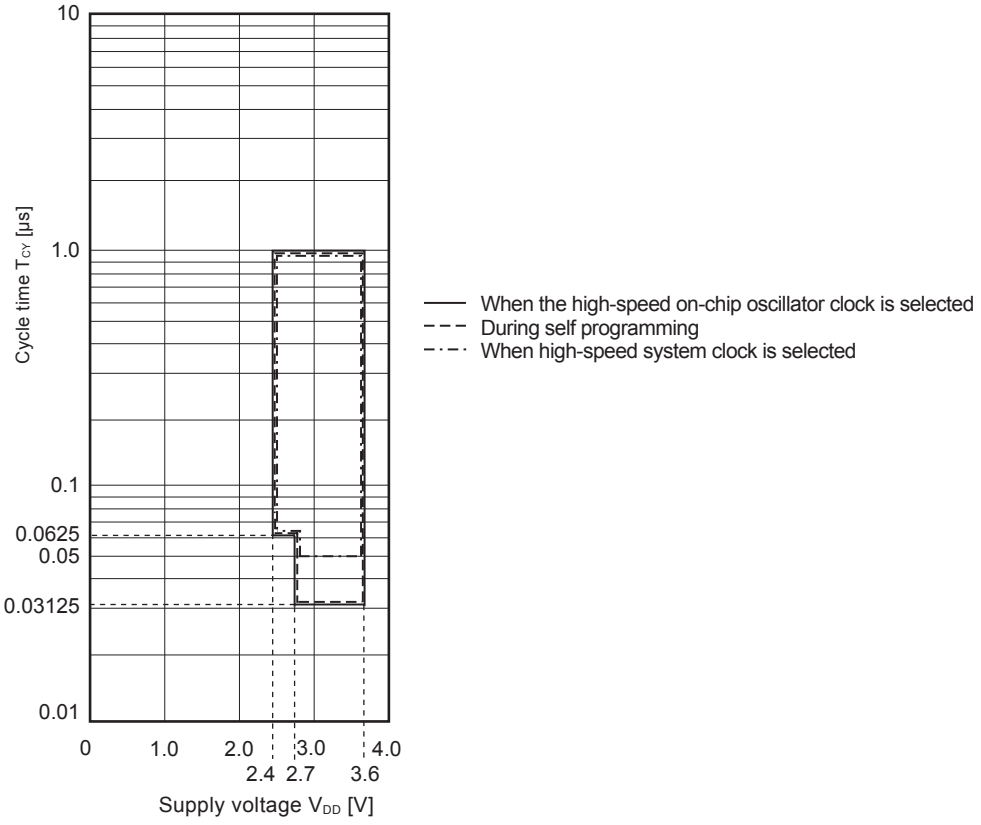
(**Caution** and **Remark** are listed on the next page.)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) (2/2)

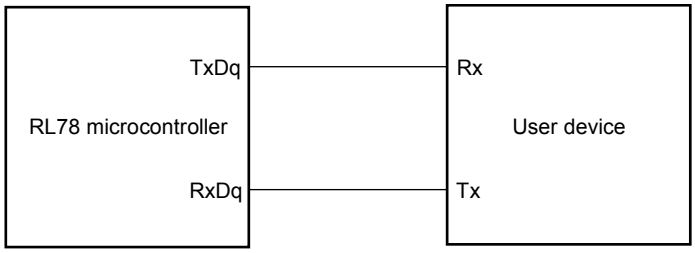
Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0, INTP3, INTP5, INTP6	1			µs
External PA control output High-level width	t_{PAHRF}	TXSELH_RF	283			µs
External PA control output low-level width	t_{PALRF}	TXSELL_RF	283			µs
$\overline{RESET}$ low-level width	t_{RSL}	$\overline{RESET}$	10			µs
$\overline{RESET\_RF}$ internal pin low-level width	t_{RSTLRF}	$\overline{RESET\_RF}$ internal pin	31			µs

Minimum Instruction Execution Time during Main System Clock Operation

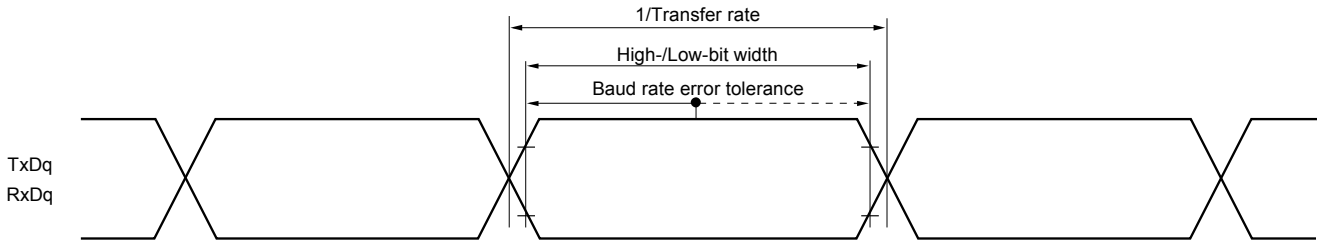
T_{CY} vs V_{DD} (HS (high-speed main) mode)



UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01))

(4) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, supporting CSI00 and CSI20)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/ f_{CLK}	2.7 V ≤ V_{DD} ≤ 3.6 V	125		500		1000		ns
			2.4 V ≤ V_{DD} ≤ 3.6 V	250		500		1000		ns
			1.8 V ≤ V_{DD} ≤ 3.6 V	–		500		1000		ns
			1.6 V ≤ V_{DD} ≤ 3.6 V	–		–		1000		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V		t_{KCY1}/2 – 18		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		t_{KCY1}/2 – 38		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		t_{KCY1}/2 – 100		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V		44		110		110		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		75		110		110		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		110		110		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		220		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V		19		19		19		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		19		19		19		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		19		19		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		19		ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO1}	C = 30 pF Note 3	2.7 V ≤ V_{DD} ≤ 3.6 V		25		25		25	ns
			2.4 V ≤ V_{DD} ≤ 3.6 V		25		25		25	ns
			1.8 V ≤ V_{DD} ≤ 3.6 V		–		25		25	ns
			1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 10), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 11))

(8) Communication at different potential (2.5 V) (CSI mode) (master mode: SCKp... internal clock output, supporting CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$ 2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	t_{KH1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 120		t_{KCY1}/2 – 120		t_{KCY1}/2 – 120		ns
SCKp low-level width	t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 10		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	121		479		479		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ		130		130		130	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	33		110		110		ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ		10		10		10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]:Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(9) Communication at different potential (1.8 V, 2.5 V) (CSI mode: master mode, SCKp... internal clock output)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) (1/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK} 2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		1150		1150		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		1150		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	–		1150		1150		ns
SCKp high-level width Note 1	t_{KH1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2-170		t_{KCY1}/2-170		t_{KCY1}/2-170		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	t_{KCY1}/2-458		t_{KCY1}/2-458		t_{KCY1}/2-458		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	–		t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		ns
SCKp low-level width Note 1	t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 18		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	–		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
SIp setup time (to SCKp↑) Note 1, 2	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		479		479		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	479		479		479		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	–		479		479		ns
SIp hold time (from SCKp↑) Note 1, 2	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	–		19		19		ns

Notes 1. Supporting CSI00 and CSI20.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

3. Use it with V_{DD} ≥ V_b.

(Caution are listed on the next page.)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Delay time from SCKp↓ to SOp output Note 1, 3	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ		195		195		195	ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ		483		483		483	ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 5 C_b = 30 pF, R_b = 5.5 kΩ		–		483		483	ns
SIp setup time (to SCKp↓) Note 2, 4	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ	44		110		110		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ	110		110		110		ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 5 C_b = 30 pF, R_b = 5.5 kΩ	–		110		110		ns
SIp hold time (from SCKp↓) Note 2, 4	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 5 C_b = 30 pF, R_b = 5.5 kΩ	–		19		19		ns
Delay time from SCKp↑ to SOp output Note 2, 4	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 5 C_b = 30 pF, R_b = 5.5 kΩ		–		25		25	ns

Notes 1. Supporting CSI00 and CSI20.

2. Supporting CSI00 only.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

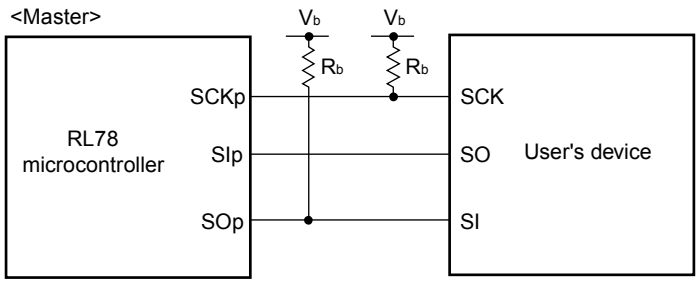
4. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. Use it with $V_{DD} \geq V_b$.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

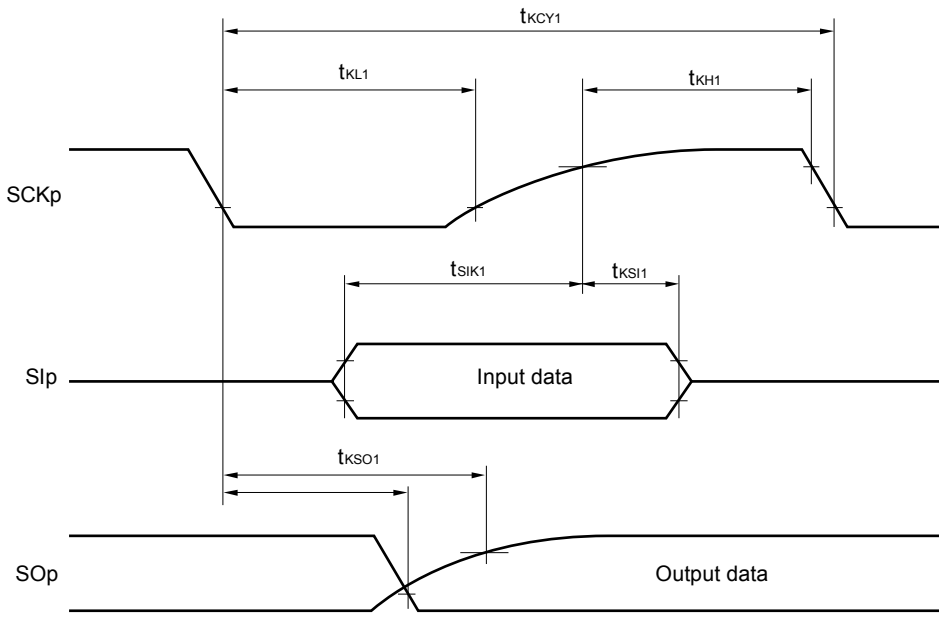


Remarks 1. R_b[Ω]:Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

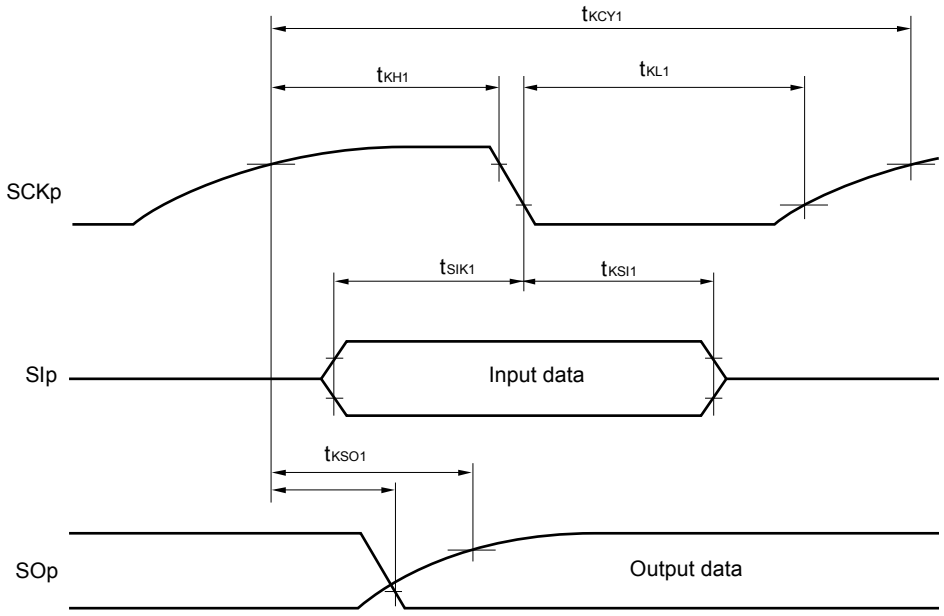
2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

3. f_{MCK} : Operation clock frequency of the serial array unit
(Operation clock to be set by the CKSmn bit of the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.
Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), conversion target : ANI0 to ANI3, ANI16 to ANI19

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (–) = AV_{REFM} Note 4 = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	T_{cony}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V	17		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to 2.**8.2 Temperature sensor and internal reference voltage characteristics.**

4. When reference voltage (-) = V_{SS}, MAX. value is following.

Zero-scale error: ±0.35 %FSR is added to the MAX. value of reference voltage (–) = AV_{REFM}.

Integral linearity error: ±0.5 LSB is added to the MAX. value of reference voltage (–) = AV_{REFM}.

Differential linearity error: ±0.2 LSB is added to the MAX. value of reference voltage (–) = AV_{REFM}.

LVD Detection Voltage of Interrupt & Reset Mode
(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

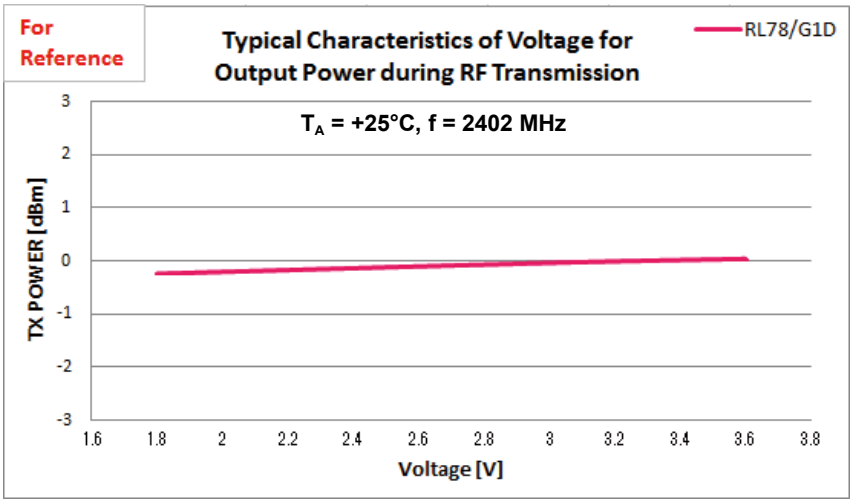
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDA0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 0, falling reset voltage		1.60	1.63	1.66	V
	V_{LVDA1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	V_{LVDA2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.8	1.84	1.87	V
	V_{LVDA3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDB0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1, falling reset voltage		1.80	1.84	1.87	V
	V_{LVDB1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVDB2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVDB3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVDC0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	V_{LVDC1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	V_{LVDD1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V

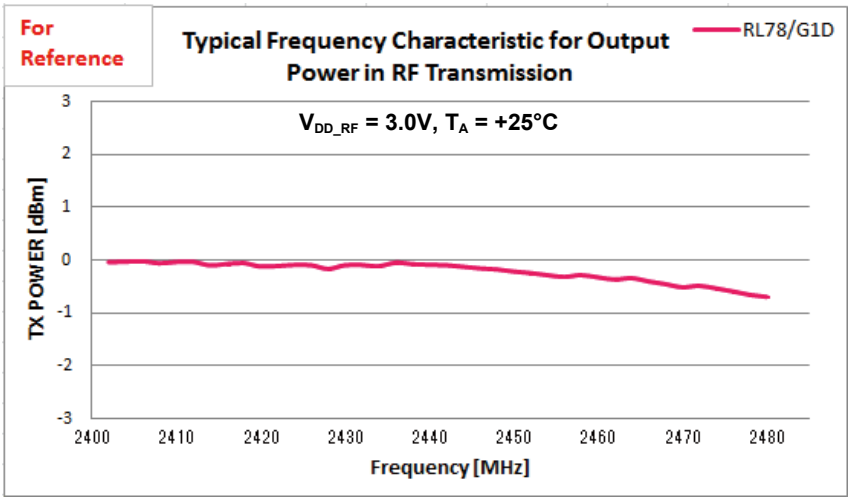
2.8.5 Supply voltage rise time

(T_A = –40 to +85°C, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD} rise slope	S_{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.6 AC Characteristics.


For Reference
Typical Characteristics of Voltage for Output Power during RF Transmission
RL78/G1D
T_A = +25°C, f = 2402 MHz
TX POWER [dBm]
3
2
1
0
-1
-2
-3
1.6
1.8
2
2.2
2.4
2.6
2.8
3
3.2
3.4
3.6
3.8
Voltage [V]


For Reference
Typical Frequency Characteristic for Output Power in RF Transmission
RL78/G1D
V_{DD_RF} = 3.0V, T_A = +25°C
TX POWER [dBm]
3
2
1
0
-1
-2
-3
2400
2410
2420
2430
2440
2450
2460
2470
2480
Frequency [MHz]

Revision History	RL78/G1D Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Apr 24, 2015	-	First Edition issued
1.10	Sep 25, 2015	p.1	Change of description in 1.1 Features
		p.7, 9	Change of 1.6 Outline of Functions
		p.14	Change of description in 2.3.2 On-chip oscillator characteristics
		p.19	Change of description in 2.5. Current Consumption
		p.23	Addition of specification to 2.5.1(3) Current for each peripheral circuit
		p.65	Change of description in 2.9.1 RF transmission characteristics
		p.66	Change of description in 2.9.2 RF reception characteristics
		p.67 to 71	Change of description in 30.9.3 Performance mapping for typical RF (Reference)
1.20	Dec 16, 2016	p.4	Change of pin name in 1.3 Pin Configuration (Top View)
		p.58	Change of pin names in 2.8 Analog Characteristics (1)
		p.60	Change of pin name in 2.8 Analog Characteristics (3)

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.