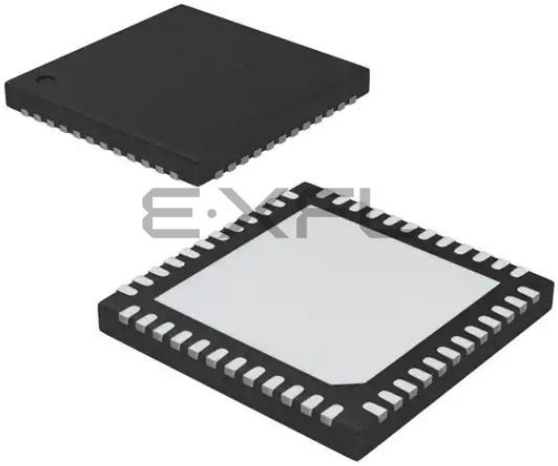
# Renesas Electronics America Inc - R5F11AGGDNB#20 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 12K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-WFQFN Exposed Pad |
| Supplier Device Package | 48-HWQFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11aggdnb-20 |

## 2.3 Oscillator Characteristics

### 2.3.1 X1, XT1, XRF oscillator characteristics

**($T_A$ = –40 to +85°C, 1.6 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| X1 clock oscillation frequency[Note 1] | Ceramic resonator Crystal resonator | $f_X$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 1 | | 20 | MHz |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 1 | | 8 | MHz |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 1.8 V | 1 | | 4 | MHz |
| XT1 clock oscillation frequency[Note 1] | | $f_{XT}$ | | 32 | 32.768 | 35 | kHz |
| RF base clock oscillation frequency[Note 2] | | $f_{XRF}$ | | | 32 | | MHz |
| RF base clock oscillation frequency accuracy[Note 2] | | $f_{XRFP}$ | | -20 | | +20 | ppm |

**Notes 1.** Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time.
Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**2.** This Oscillator characteristics is base clock for RF Transceiver.

**Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user.**
**Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

### 2.3.2 On-chip oscillator characteristics

**($T_A$ = –40 to +85°C, 1.6 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Oscillators | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency[Notes 1, 2] | $f_{IH}$ | | | 1 | | 32 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | $f_{IHP}$ | –20 to +85°C | 1.8 V ≤ $V_{DD}$ ≤3.6 V | -1.5 | | +1.5. | % |
| | | | 1.6 V ≤ $V_{DD}$ <1.8 V | -5.0 | | +5.0 | % |
| | | –40 to –20°C | 1.8 V ≤ $V_{DD}$ ≤3.6 V | -2.5 | | +2.5. | % |
| | | | 1.6 V ≤ $V_{DD}$ <1.8 V | -5.5 | | +5.5 | % |
| Low-speed on-chip oscillator clock frequency[Notes 3] | $f_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | $f_{ILP}$ | | | –15 | | +15 | % |
| On-chip oscillator clock frequency for the RF slow clock[Note 3] | $f_{ILRF}$ | | | | 32.768 | | kHz |
| On-chip oscillator clock frequency accuracy for the RF slow clock | $f_{ILRFP}$ | | | -0.025 | | 0.025 | % |

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

**2.** This indicates the oscillator characteristics only. Refer to **AC Characteristics** for instruction execution time.

**3.** This indicates the oscillator characteristics only.

## 2.4 DC Characteristics

### 2.4.1 Output current

**($T_A$ = –40 to +85°C, 1.6 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Output current, high[Note 1] | $I_{OH1}$ | P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147 | Per pin | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | | –10.0[Note 2] | mA |
| | | P00, P01, P02, P03, P40, P120, P130, P140 | Total[Note 3] | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | –10.0 | mA |
| | | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | –5.0 | mA |
| | | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | –2.5 | mA |
| | | P10, P11, P12, P13, P14, P15, P16, P30, P147 | Total[Note 3] | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | –19.0 | mA |
| | | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | –10.0 | mA |
| | | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | –5.0 | mA |
| | | Total of all pins[Note 3] | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | | –135.0[Note 4] | mA |
| | $I_{OH2}$ | P20, P21, P22, P23 | Per pin | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | | –0.1[Note 2] | mA |
| | | | Total[Note 3] | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | | –1.5 | mA |
| | $I_{OHRF}$ | GPIO0, GPIO1, GPIO2, GPIO3 | Per pin | 1.6 V ≤ $V_{DD\_RF}$ ≤ 3.6 V | | | –2.0 | mA |
| Output current, low[Note 1] | $I_{OL1}$ | P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147 | Per pin | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | | 20.0[Note 2] | mA |
| | | P60, P61 | Per pin | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | | 15.0[Note 2] | mA |
| | | P00, P01, P02, P03, P40, P120, P130, P140 | Total[Note 3] | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | 15.0 | mA |
| | | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 9.0 | mA |
| | | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | 4.5 | mA |
| | | P10, P11, P12, P13, P14, P15, P16, P30, P60, P61, P147 | Total[Note 3] | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | 35.0 | mA |
| | | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 20.0 | mA |
| | | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | 10.0 | mA |
| | | Total of all pins[Note 3] | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | | 150.0 | mA |
| | $I_{OL2}$ | P20, P21, P22, P23 | Per pin | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | | 0.4[Note 2] | mA |
| | | | Total[Note 3] | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | | 5.0 | mA |
| | $I_{OLRF}$ | GPIO0, GPIO1, GPIO2, GPIO3 | Per pin | 1.6 V ≤ $V_{DD\_RF}$ ≤ 3.6 V | | | 2.0 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from the $V_{DD}$ pin to an output pin.

**2.** However, do not exceed the total current value.

**3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 50% and $I_{OH}$ = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(50 × 0.01) = –14.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**4.** Product for industrial applications (R5F11AGGDNB, R5F11AGHDNB, R5F11AGJDNB) is –100.0 mA.

(**Caution** and **Remark** are listed on the next page.)

**Notes 1.** Current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**4.** When high-speed system clock and subsystem clock are stopped.

**5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 4 MHz

**8.** If operation of the subsystem clock when STOP mode, same as when HALT mode of subsystem clock operation.

**9.** The upper value is for square-wave input and the lower is with an oscillator connected.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (External main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

### (3) Current for each peripheral circuit

**($T_A$ = –40 to +85°C, 1.6 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed on-chip oscillator operating current | $I_{FIL}$ Note 1 | | | | 0.20 | | μA |
| Current when PCLBUZ0 and EXSLK_RF are connected together and MCU supplies RF slow clock to RF | $I_{PCEX}$ Note 1 | | | | 1.0 | | μA |
| RTC operating current | $I_{RTC}$ Notes 1, 2, 3 | | | | 0.02 | | μA |
| 12-bit interval timer operating current | $I_{IT}$ Notes 1, 2, 4 | | | | 0.02 | | μA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 5 | $f_{IL}$ is 15 kHz | | | 0.22 | | μA |
| A/D converter operating current | $I_{ADC}$ Notes 1, 6 | When conversion at maximum speed | $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 0.5 | 0.7 | mA |
| A/D converter reference voltage current | $I_{ADREF}$ Note 1 | | | | 75.0 | | μA |
| Thermometer sensor operating current | $I_{TMPS}$ Note 1 | | | | 75.0 | | μA |
| LVD operating current | $I_{LVI}$ Note 1, 7 | | | | 0.08 | | μA |
| Flash self-programming operating current | $I_{FSP}$ Notes 1, 9 | | | | 2.50 | 12.20 | mA |
| BGO current | $I_{BGO}$ Notes 1, 8 | | | | 2.50 | 12.20 | mA |
| SNOOZE operating current | $I_{SNOZ}$ Note 1 | ADC operation | The mode is performed Note 10 | | 0.50 | 0.60 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 1.20 | 1.44 | mA |
| | | CSI/UART operation | | | 0.70 | 0.84 | mA |

**Notes 1.** Current flowing to $V_{DD}$.

**2.** When high speed on-chip oscillator and high-speed system clock are stopped.

**3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the XT1 oscillator). The value of the current value of the RL78 microcontroller is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{RTC}$, when the real-time clock operates in operation mode or HALT mode. Also, add the value of IFIL in case of selecting low-speed on-chip oscillator. $I_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.

**4.** Current flowing only to the 12 bit interval timer (including the operating current of the low-speed on-chip oscillator). The current value of the MCU is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{IT}$ when $f_{CLK}$ = $f_{SUB}$ when the watchdog timer operates in STOP mode. When using low-speed on-chip oscillator, add $I_{FIL}$.

**5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the MCU is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer is in operation.

**6.** Current flowing only to the A/D converter. The current value of MCU is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

**7.** Current flowing only to the LVD circuit. The current value of MCU is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVI}$ when the LVD circuit is in operation.

**8.** Current flowing when operates rewriting to Data flash.

**9.** Current flowing when operates flash self-programming.

**10.** Shift time to the SNOOZE mode is referred User's Manual: Hardware.

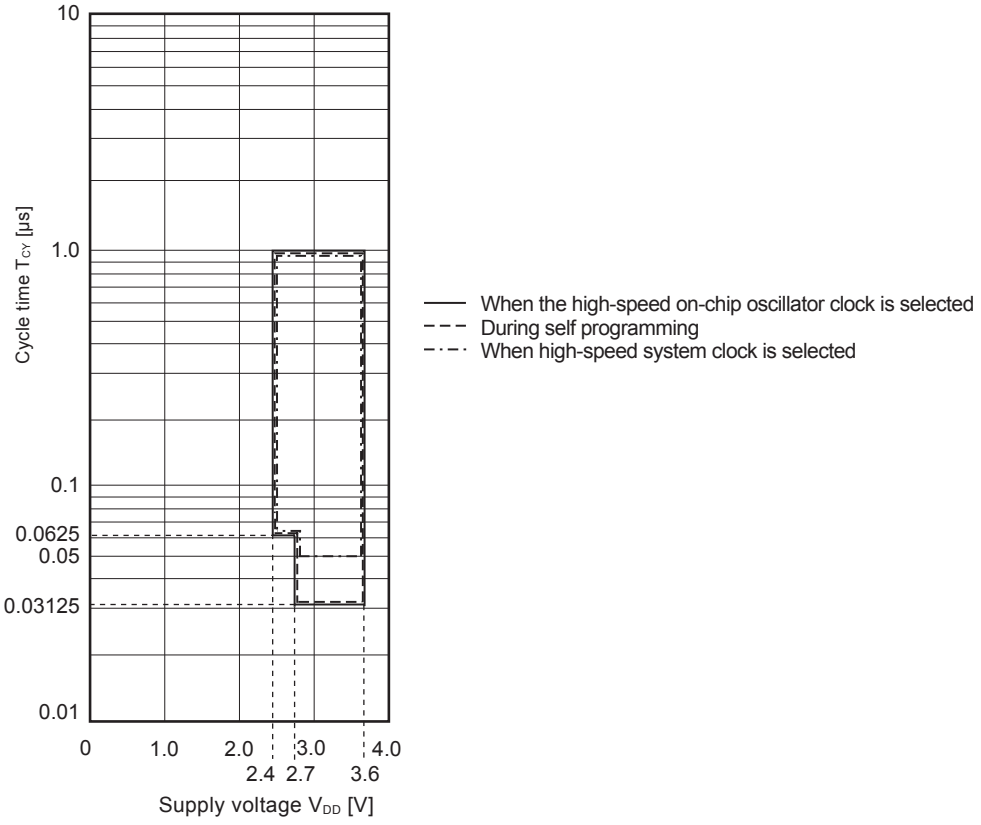
(**Remarks** are listed on the next page.)

**($T_A$ = –40 to +85°C, 1.6 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V) (2/2)**

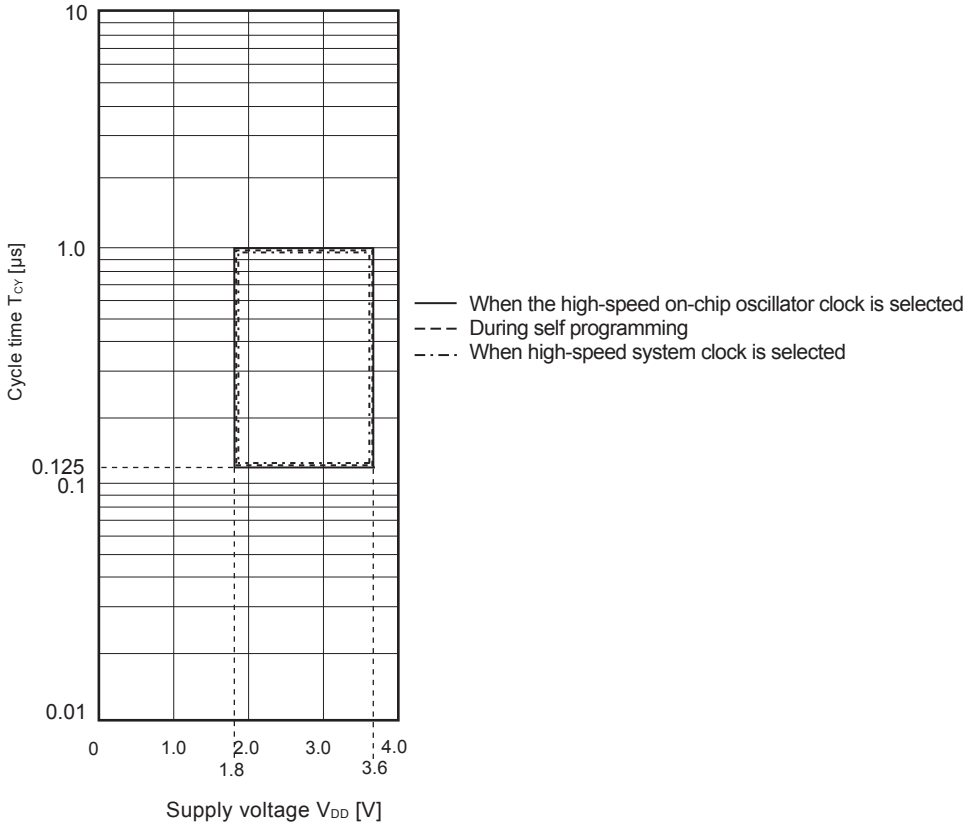
| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Interrupt input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | INTP0, INTP3, INTP5, INTP6 | 1 | | | µs |
| External PA control output High-level width | $t_{PAHRF}$ | TXSELH_RF | 283 | | | µs |
| External PA control output low-level width | $t_{PALRF}$ | TXSELL_RF | 283 | | | µs |
| $\overline{RESET}$ low-level width | $t_{RSL}$ | $\overline{RESET}$ | 10 | | | µs |
| $\overline{RESET\_RF}$ internal pin low-level width | $t_{RSTLRF}$ | $\overline{RESET\_RF}$ internal pin | 31 | | | µs |

**Minimum Instruction Execution Time during Main System Clock Operation**

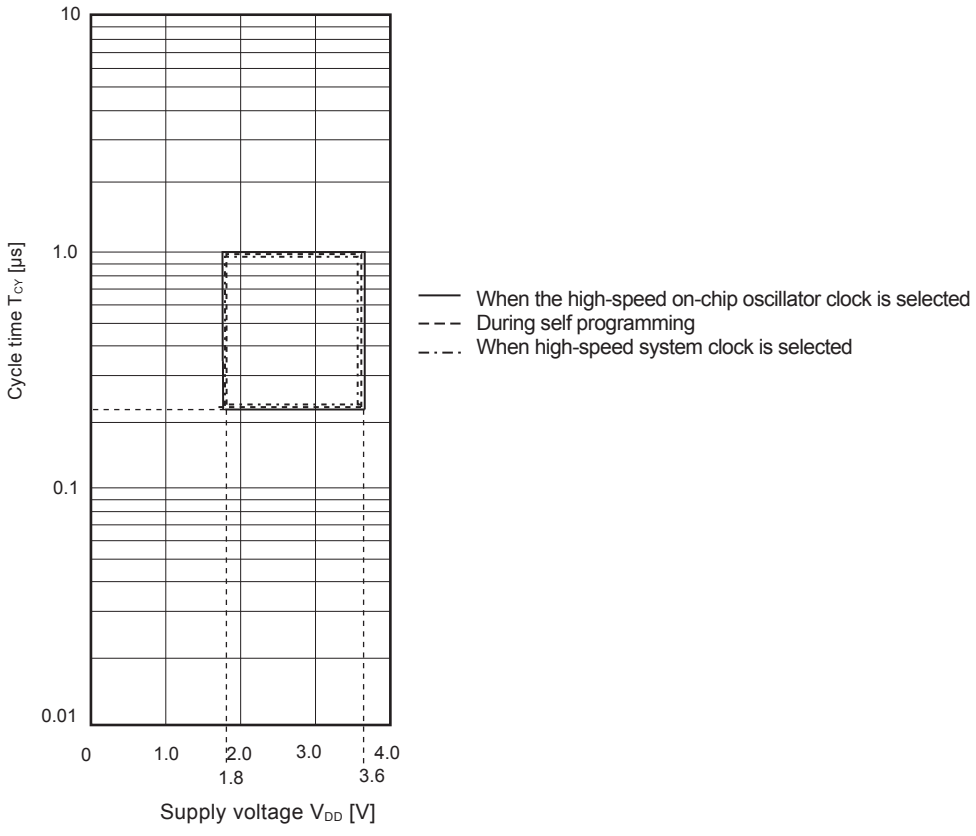
$T_{CY}$ vs $V_{DD}$ (HS (high-speed main) mode)



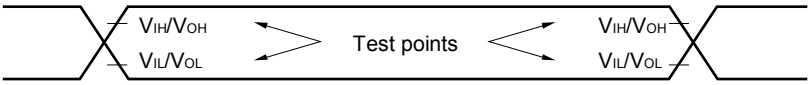
$T_{CY}$ vs $V_{DD}$ (LS (low-speed main) mode)



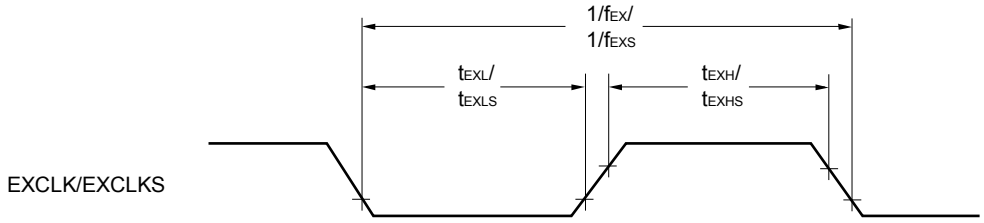

$T_{CY}$ vs $V_{DD}$ (LV (low-voltage main) mode)



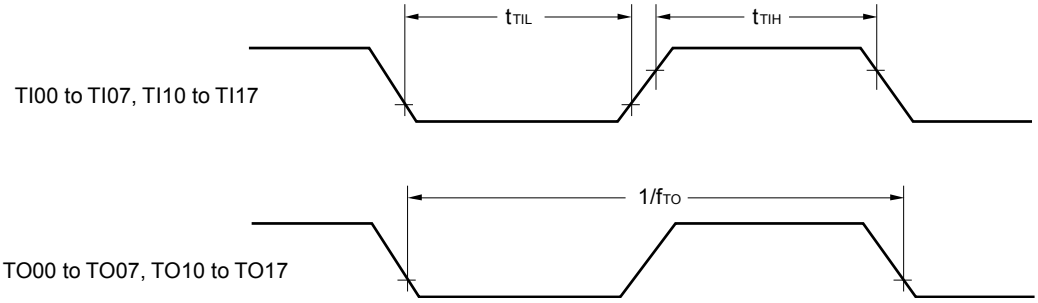
### AC Timing Test Points



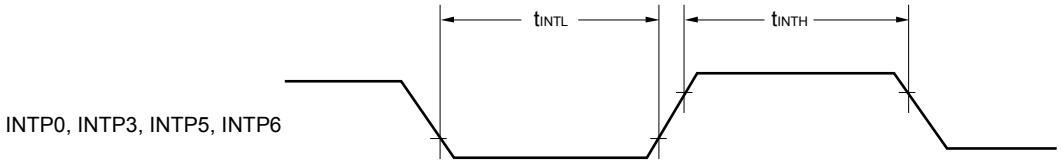

### External System Clock Timing



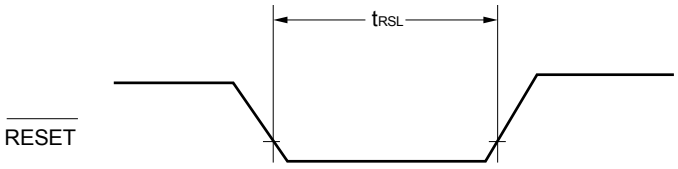

### TI/TO Timing




### Interrupt Request Input Timing




### $\overline{\text{RESET}}$ Input Timing



**(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, supporting CSI00 only)**

**($T_A$ = –40 to +85°C, 2.7 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 2/f_{CLK}$ | 83.3 | | 250 | | 500 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | | $t_{KCY1}/2 - 10$ | | $t_{KCY1}/2 - 50$ | | $t_{KCY1}/2 - 50$ | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | | 33 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↓ to SOp output Note 2 | $t_{KSO1}$ | C = 20 pF Note 3 | | 10 | | 10 | | 10 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** C is the load capacitance of the SCKp and SOp output lines.

**Cautions Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remarks 1.** This specification is valid only when CSI00's peripheral I/O redirect function is not used.

**2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

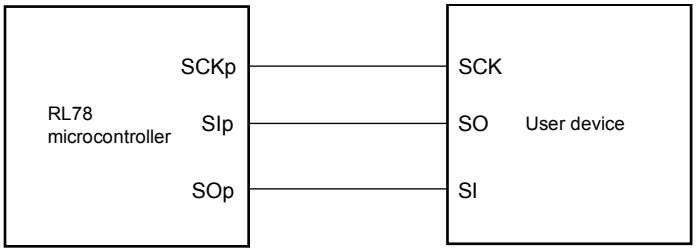
**3.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

**Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remarks 1.** p: CSI number (p = 00, 20), m: Unit number (m = 0, 1),
n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

**2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 10))

**CSI mode connection diagram (during communication at same potential)**



### (9) Communication at different potential (1.8 V, 2.5 V) (CSI mode: master mode, SCKp... internal clock output)

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY1}$ | $t_{KCY1}$ ≥ 4/$f_{CLK}$ 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 500 | | 1150 | | 1150 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | – | | 1150 | | 1150 | | ns |
| SCKp high-level width Note 1 | $t_{KH1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | $t_{KCY1}$/2-170 | | $t_{KCY1}$/2-170 | | $t_{KCY1}$/2-170 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | $t_{KCY1}$/2-458 | | $t_{KCY1}$/2-458 | | $t_{KCY1}$/2-458 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | – | | $t_{KCY1}$/2 – 458 | | $t_{KCY1}$/2 – 458 | | ns |
| SCKp low-level width Note 1 | $t_{KL1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | $t_{KCY1}$/2 – 18 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | – | | $t_{KCY1}$/2 – 50 | | $t_{KCY1}$/2 – 50 | | ns |
| SIp setup time (to SCKp↑) Note 1, 2 | $t_{SIK1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 177 | | 479 | | 479 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 479 | | 479 | | 479 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | – | | 479 | | 479 | | ns |
| SIp hold time (from SCKp↑) Note 1, 2 | $t_{KSI1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | 19 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | – | | 19 | | 19 | | ns |

**Notes 1.** Supporting CSI00 and CSI20.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**3.** Use it with $V_{DD}$ ≥ $V_b$.

**(Caution** are listed on the next page.)

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>2.3 V ≤ $V_b$ ≤ 2.7 V | $t_{KCY2}$/2 – 18 | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V<br>1.6 V ≤ $V_b$ ≤ 2.0 V | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| | | 1.8 V ≤ $V_{DD}$<3.3 V<br>1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | – | | $t_{KCY2}$/2 – 50 | | $t_{KCY2}$/2 – 50 | | ns |
| SIp setup time (to SCKp↑) Note 3 | $t_{SIK2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>2.3 V ≤ $V_b$ ≤ 4.0 V | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V<br>1.6 V ≤ $V_b$ ≤ 2.0 V | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $V_{DD}$<3.3 V<br>1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | – | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) Note 3 | $t_{KSI2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>2.3 V ≤ $V_b$ ≤ 4.0 V | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V<br>1.6 V ≤ $V_b$ ≤ 2.0 V | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| | | 1.8 V ≤ $V_{DD}$<3.3 V<br>1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | – | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output Note 4 | $t_{KSO2}$ | 2.7 V ≤ $V_{DD}$ < 3.6 V<br>2.3 V ≤ $V_b$ ≤ 2.7 V<br>$C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 2/$f_{MCK}$ + 214 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V<br>1.6 V ≤ $V_b$ ≤ 2.0 V<br>$C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |
| | | 1.8 V ≤ $V_{DD}$< 3.3 V<br>1.6 V ≤ $V_b$ ≤ 2.0 V Note 2<br>$C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | – | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |

**Notes 1.** Transfer rate in the SNOOZE mode : MAX. 1 Mbps

**2.** Use it with $V_{DD}$ ≥ $V_b$.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

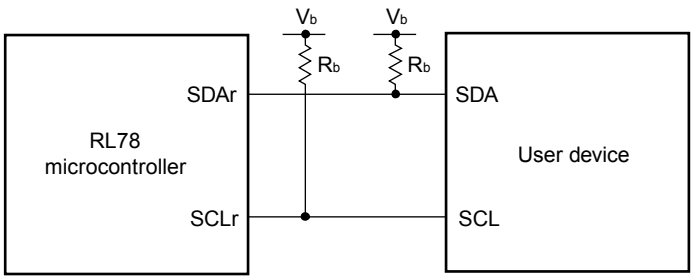
### (11) Communication at different potential (1.8 V, 2.5 V) (simplified $I^2C$ mode)

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)** **(1/2)**

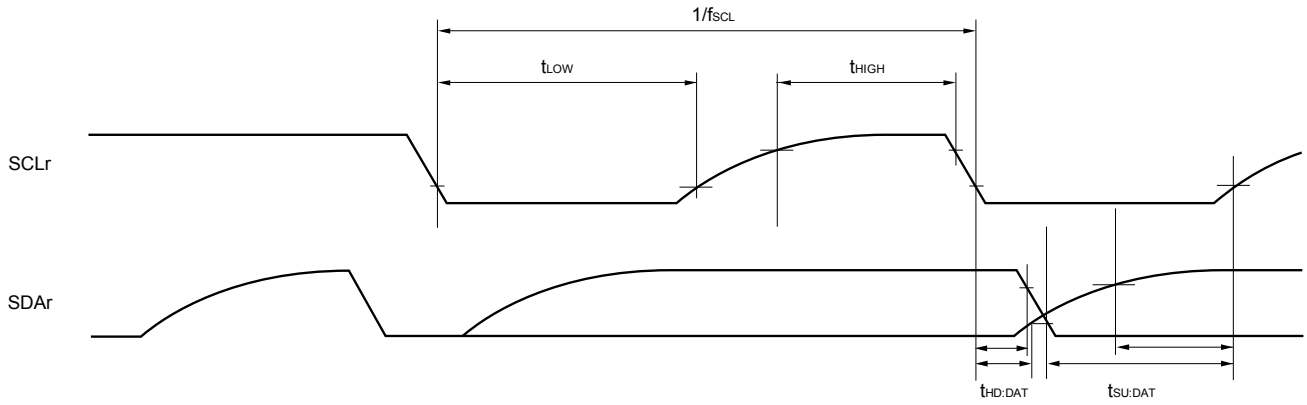
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>2.3 V ≤ $V_b$ ≤ 2.7 V<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 300 Note 5 | | 300 Note 5 | kHz |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>2.3 V ≤ $V_b$ ≤ 2.7 V<br>$C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | | 300 Note 5 | | 300 Note 5 | kHz |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V<br>1.6 V ≤ $V_b$ ≤ 2.0 V<br>$C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 300 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V<br>1.6 V ≤ $V_b$ ≤ 2.0 V Note 2<br>$C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | – | | 300 Note 1 | | 300 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>2.3 V ≤ $V_b$ ≤ 2.7 V<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1550 | | 1550 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>2.3 V ≤ $V_b$ ≤ 2.7 V<br>$C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1150 | | 1550 | | 1550 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V<br>1.6 V ≤ $V_b$ ≤ 2.0 V<br>$C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1150 | | 1550 | | 1550 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V<br>1.6 V ≤ $V_b$ ≤ 2.0 V Note 2<br>$C_b$ = 100 pF, $R_b$ = 5.5 kΩ | – | | 1550 | | 1550 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>2.3 V ≤ $V_b$ ≤ 2.7 V<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 200 | | 610 | | 610 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>2.3 V ≤ $V_b$ ≤ 2.7 V<br>$C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 600 | | 610 | | 610 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V<br>1.6 V ≤ $V_b$ ≤ 2.0 V<br>$C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 610 | | 610 | | 610 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V<br>1.6 V ≤ $V_b$ ≤ 2.0 V Note 2<br>$C_b$ = 100 pF, $R_b$ = 5.5 kΩ | – | | 610 | | 610 | | ns |

(**Note, Caution** and **Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at different potential)**




**Simplified I²C mode serial transfer timing (during communication at different potential)**




**Remarks 1.** $R_b$[Ω]:Communication line (SDAr, SCLr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance, $V_b$[V]: Communication line voltage

**2.** r: IIC number (r = 00, 10), g: PIM, POM number (g = 0, 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02))

### 2.7.2 Serial interface IICA

#### (1) $I^2C$ standard mode

**($T_A$ = –40 to +85°C, 1.6 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Standard mode: $f_{CLK}$ ≥ 1 MHz | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | – | | 0 | 100 | 0 | 100 | kHz |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | – | | – | | 0 | 100 | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | – | | 4.7 | | µs |
| Hold time[Note 1] | $t_{HD:STA}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | – | | 4.0 | | µs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | – | | 4.7 | | µs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | – | | 4.0 | | µs |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 250 | | 250 | | 250 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 250 | | 250 | | 250 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | 250 | | 250 | | ns |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | – | | 250 | | ns |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | µs |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | µs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | 0 | 3.45 | 0 | 3.45 | µs |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | – | | 0 | 3.45 | µs |
| Setup time of stop condition | $t_{SU:STO}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | – | | 4.0 | | µs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | – | | 4.7 | | µs |

(**Notes**, **Caution** and **Remark** are listed on the next page.)

### (2) $I^2C$ fast mode

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | – | | 0 | 400 | 0 | 400 | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | 0.6 | | 0.6 | | μs |
| Hold time[Note 1] | $t_{HD:STA}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | 0.6 | | 0.6 | | μs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 1.3 | | 1.3 | | 1.3 | | μs |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 1.3 | | 1.3 | | 1.3 | | μs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | 1.3 | | 1.3 | | μs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | 0.6 | | 0.6 | | μs |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 100 | | 100 | | 100 | | μs |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 100 | | 100 | | 100 | | μs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | 100 | | 100 | | μs |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | μs |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | μs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | 0 | 0.9 | 0 | 0.9 | μs |
| Setup time of stop condition | $t_{SU:STO}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | 0.6 | | 0.6 | | μs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 1.3 | | 1.3 | | 1.3 | | μs |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 1.3 | | 1.3 | | 1.3 | | μs |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | – | | 1.3 | | 1.3 | | μs |

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

**Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: $C_b$ = 320 pF, $R_b$ = 1.1 kΩ

### (3) $I^2C$ fast mode plus

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode plus: $f_{CLK}$ ≥ 10 MHz | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 0 | 1000 | – | | – | | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.26 | | – | | – | | μs |
| Hold time[Note 1] | $t_{HD:STA}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.26 | | – | | – | | μs |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.5 | | – | | – | | μs |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.26 | | – | | – | | μs |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 50 | | – | | – | | μs |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0 | 0.45 | – | | – | | μs |
| Setup time of stop condition | $t_{SU:STO}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.26 | | – | | – | | μs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.5 | | – | | – | | μs |

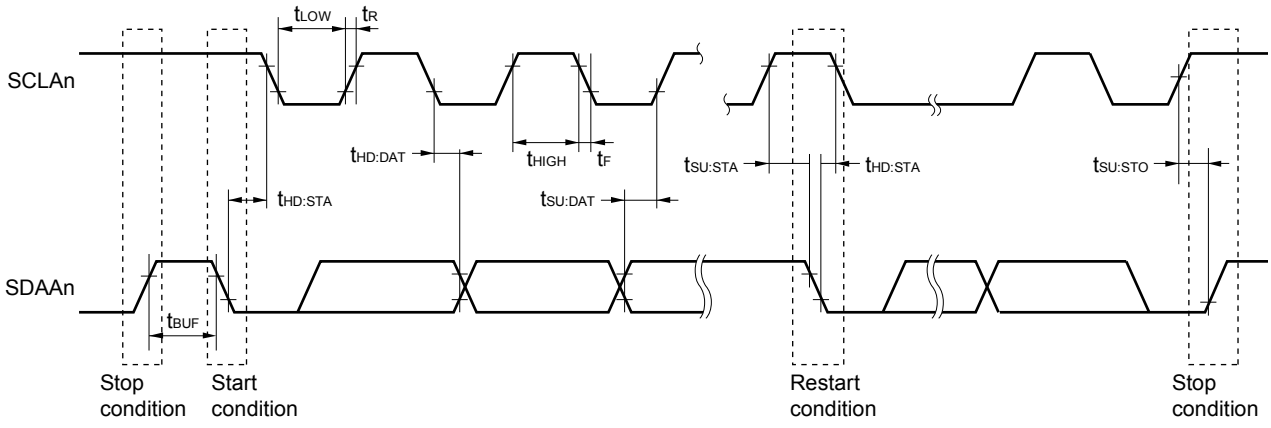
**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

**Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: $C_b$ = 120 pF, $R_b$ = 1.1 kΩ

**IICA serial transfer timing**




**Remark** n = 0

### 2.8.2 Temperature sensor and internal reference voltage characteristics

**($T_A$ = –40 to +85°C, 2.4 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V, HS (high-speed main) mode)**

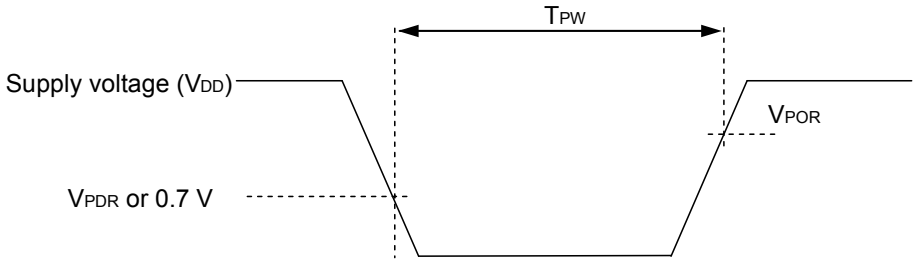
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor output voltage that depends on the temperature | | –3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

### 2.8.3 POR circuit characteristics

**($T_A$ = –40 to +85°C, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{POR}$ | Rise time | 1.47 | 1.51 | 1.55 | V |
| | $V_{PDR}$ | Fall time | 1.46 | 1.50 | 1.54 | V |
| Minimum pulse width[Note] | $T_{PW}$ | Other than STOP/SUB_RUN/SUB_HALT | 300 | | | μs |

**Note** This is the time required for the POR circuit to execute a reset operation when $V_{DD}$ falls below $V_{PDR}$. When the main system clock ($f_{MAIN}$) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC) or when the microcontroller enters STOP mode, this is the time required for the POR circuit to execute a reset operation between when $V_{DD}$ falls below 0.7 V and when $V_{DD}$ rises to $V_{POR}$ or higher.

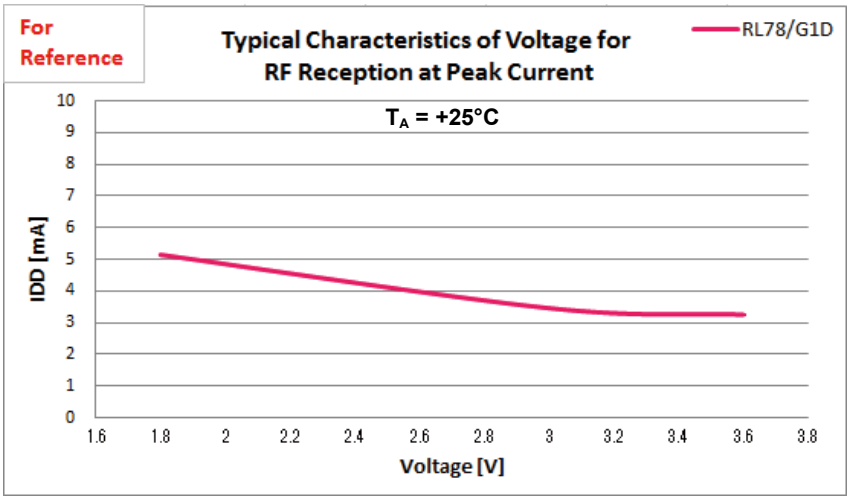


### 2.9.2 RF reception characteristics

Unless specified otherwise, the measurement is performed by our evaluation board.

**($T_A$ = +25°C, $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ = 3.0 V, f = 2440 MHz, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

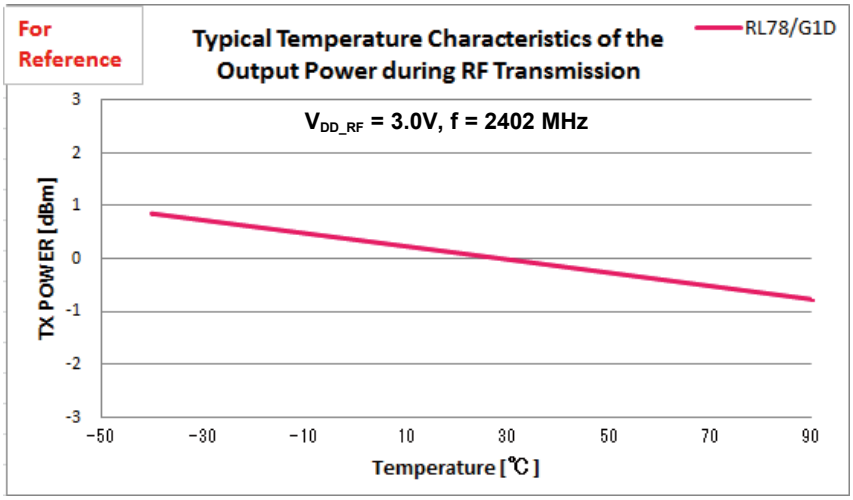
| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| RF input frequency | $RF_{RXFRIN}$ | | | 2402 | | 2480 | MHz |
| Maximum input level | $RF_{LEVL}$ | PER ≤ 30.8% RF input pin | RF low power mode | -10 | 0 | - | dBm |
| | | | RF normal mode | -10 | 1 | - | dBm |
| | | | RF high performance mode | -10 | 1 | - | dBm |
| Receiver sensitivity | $RF_{STY}$ | PER ≤ 30.8% | RF low power mode | - | -60 | -50 | dBm |
| | | | RF normal mode | - | -90 | -70 | dBm |
| | | | RF high performance mode | - | -92 | -70 | dBm |
| Secondary radiation | $RF_{RXSP}$ | | 30 MHz to 1 GHz | - | -72 | -57 | dBm/ 100 kHz |
| | | | 1 GHz to 12 GHz | - | -57 | -54 | dBm/ 100 kHz |
| Common channel rejection ratio | $RF_{CCR}$ | PER ≤ 30.8%, Prf = –67dBm | | -21 | -12 | - | dB |
| Adjacent channel rejection ratio | $RF_{ADCR}$ | PER ≤ 30.8% Prf = –67 dBm | ±1 MHz | -15 | -5 | - | dB |
| | | | ±2 MHz | 17 | 29 | - | dB |
| | | | ±3 MHz | 27 | 34 | - | dB |
| Blocking | $RF_{BLK}$ | PER ≤ 30.8% Prf = –67 dBm | 30 MHz - 2000 MHz | -30 | -13 | - | dB |
| | | | 2000 MHz to 2399 MHz | -35 | -30 | - | dBm |
| | | | 2484 MHz to 3000 MHz | -35 | -30 | - | dBm |
| | | | > 3000 MHz | -30 | -17 | - | dBm |
| Frequency tolerance | $RF_{RXFERR}$ | PER ≤ 30.8% | | -250 | | +250 | kHz |
| RSSI accuracy | $RF_{RSSIS}$ | $T_A$ = +25°C, –70 dBm ≤ Prf ≤ –10 dBm | | -4 | 0 | 4 | dB |




**(3) RF Output Power during Transmission**

Unless specified otherwise, the measurement is performed by our evaluation board.

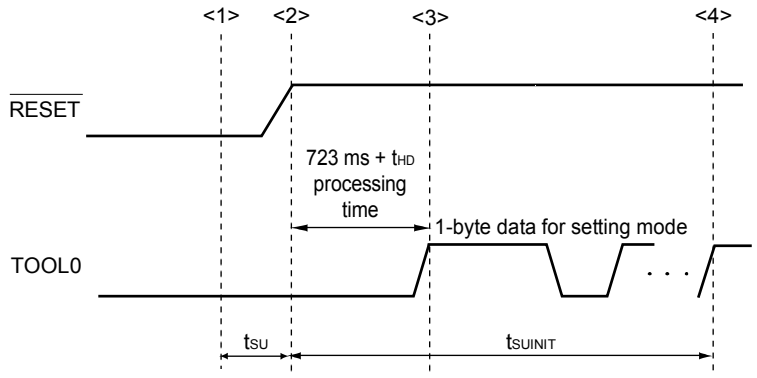
Current consumption is not including MCU unit.



## 2.13 Timing of Entry to Flash Memory Programming Modes

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Time to complete the communication for the initial setting after the external reset is released | $t_{SUINIT}$ | POR and LVD reset must be released before the external reset is released. | | 100 | ms |
| Time to release the external reset after the TOOL0 pin is set to the low level | $t_{SU}$ | POR and LVD reset must be released before the external reset is released. | 10 | | μs |
| Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset must be released before the external reset is released. | 1 | | ms |




<1> The low level is input to the TOOL0 pin.
<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** $t_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.
$t_{SU}$: Time to release the external reset after the TOOL0 pin is set to the low level
$t_{HD}$: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)