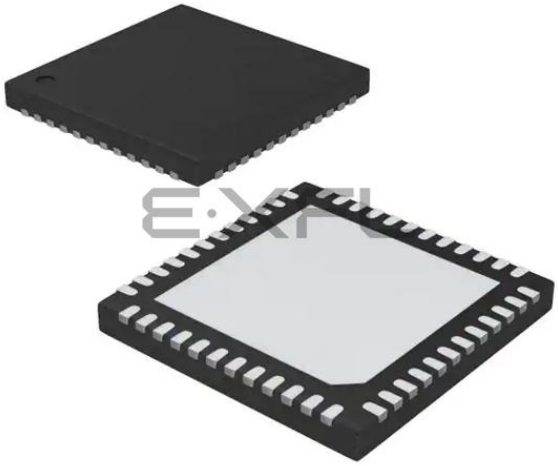

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	32
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11aghanb-20

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}	V_{DD}	–0.5 to +6.5	V
	V_{DDRF1}	V_{DD_RF}	–0.5 to +4.0	V
	V_{DDRF2}	AV_{DD_RF}	–0.5 to +4.0	V
	V_{DDRF3}	DCLIN	–0.5 to +4.0	V
	V_{SSRF}	V_{SS_RF}, AV_{SS_RF}	–0.5 to +0.3	V
Input voltage	V_{I1}	P00, P01, P02, P03, P10, P11, P12, P14, P15, P16, P20, P21, P22, P23, P30, P40, P120, P121, P122, P123, P124, P137, P140, P147, RESET	–0.3 to V_{DD}+0.3 Note 1	V
	V_{I2}	P60, P61	–0.3 to +6.5	V
	V_{IRF1}	GPIO0, GPIO1, GPIO2, GPIO3	–0.3 to V_{DD_RF}+0.3 Note 2	V
	V_{IRF2}	ANT	–0.5 to +1.4	V
Output voltage	V_O	P00, P01, P02, P03, P10, P11, P12, P14, P15, P16, P20, P21, P22, P23, P30, P40, P60, P61, P120, P130, P140, P147	–0.3 to V_{DD}+0.3 Note 1	V
	V_{ORF}	GPIO0, GPIO1, GPIO2, GPIO3, DCLOUT	–0.3 to V_{DD_RF}+0.3 Note 2	V
Analog input voltage	V_{AI}	ANI0, ANI1, ANI2, ANI3, ANI16, ANI17, ANI18, ANI19	–0.3 to V_{DD}+0.3 and –0.3 to $V_{REF(+)}$+0.3 Notes 2, 4	V
REGC pin input voltage	V_{IREGC}	REGC	–0.3 to +2.8 and –0.3 to V_{DD}+0.3 Note 3	V
IC pin input voltage	V_{IIC}	IC0, IC1	–0.5 to +0.3	V

Notes 1. Must be 6.5 V or lower.

2. Must be 4.0 V or lower.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

4. Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. Reference voltage is V_{SS}.

2.4.3 Output voltage

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	I_{OH} = –2.0 mA	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P140, P147	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} – 0.6			V
		I_{OH} = –1.5 mA		1.8 V ≤ V_{DD} ≤ 3.6 V	V_{DD} – 0.5			V
		I_{OH} = –1.0 mA		1.6 V ≤ V_{DD} ≤ 3.6 V	V_{DD} – 0.5			V
		I_{OH} = –10 μA	P130		V_{DD} – 0.3			V
	V_{OH2}	I_{OH} = –100 μA	P20, P21, P22, P23		V_{DD} – 0.5			V
	V_{OHRF}	I_{OH} = –2.0 mA	GPIO0, GPIO1, GPIO2, GPIO3	2.7 V ≤ V_{DD_RF} ≤ 3.6 V	V_{DD_RF} – 0.3			V
		I_{OH} = –1.5 mA		1.8 V ≤ V_{DD_RF} ≤ 3.6 V	V_{DD_RF} – 0.3			V
Output voltage, low	V_{OL1}	I_{OL} = 3.0 mA	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	2.7 V ≤ V_{DD} ≤ 3.6 V			0.6	V
		I_{OL} = 1.5 mA					0.4	V
		I_{OL} = 0.6 mA		1.8 V ≤ V_{DD} ≤ 3.6 V			0.4	V
		I_{OL} = 0.3 mA		1.6 V ≤ V_{DD} ≤ 3.6 V			0.4	V
	V_{OL2}	I_{OL} = 400 μA	P20, P21, P22, P23				0.4	V
	V_{OLRF}		GPIO0, GPIO1, GPIO2, GPIO3				0.3	V

Caution P00, P02, P03, and P10 to P15 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.4.4 Input leakage current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	VI = V_{DD}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P60, P61, P120, P140, P147			1	μA
	I_{LIH2}	VI = V_{DD}	P20, P21, P22, P23, P137, $\overline{\text{RESET}}$			1	μA
	I_{LIH3}	VI = V_{DD}	P121, P122, P123, P124 (EXCLK, EXCLKS) (XT1, XT2) In input port			1	μA
			In external clock input			1	μA
			In resonator connection			10	μA
	I_{LIHRF}	VI = V_{DD_RF}	GPIO0, GPIO1, GPIO2, GPIO3			10	μA
Input leakage current, low	I_{LIL1}	VI = V_{SS}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P60, P61, P120, P140, P147			-1	μA
	I_{LIL2}	VI = V_{SS}	P20, P21, P22, P23, P137, $\overline{\text{RESET}}$			-1	μA
	I_{LIL3}	VI = V_{SS}	P121, P122, P123, P124 (EXCLK, EXCLKS) (XT1, XT2) In input port			-1	μA
			In external clock input			-1	μA
			In resonator connection			-10	μA
	I_{LILRF}	VI = V_{SS_RF}	GPIO0, GPIO1, GPIO2, GPIO3			-10	μA

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.4.5 Resistance

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
On-chip pll-up resistance	R_U	VI = V_{SS}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P140, P147 In input mode	10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) Standby current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
HALT current Note 1, 2	I_{DD2}	HS (high-speed main) mode Note 7	f_{IH} = 32 MHz Note 4	V_{DD} = 3.0 V		0.62	1.86	mA
			f_{IH} = 24 MHz Note 4	V_{DD} = 3.0 V		0.50	1.45	mA
			f_{IH} = 16 MHz Note 4	V_{DD} = 3.0 V		0.44	1.11	mA
		LS (low-speed main) mode Note 7	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		290	620	μA
				V_{DD} = 2.0 V		290	620	μA
		LV (low-voltage main) mode Note 7	f_{IH} = 4 MHz Note 4	V_{DD} = 3.0 V		440	680	μA
				V_{DD} = 2.0 V		440	680	μA
		HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3	V_{DD} = 3.0 V Note 9		0.31	1.08	mA
						0.48	1.28	mA
			f_{MX} = 10 MHz Note 3	V_{DD} = 3.0 V Note 9		0.21	0.63	mA
						0.28	0.71	mA
		LS (low-speed main) mode Note 7	f_{MX} = 8 MHz Note 3	V_{DD} = 3.0 V Note 9		110	360	μA
						160	420	μA
				V_{DD} = 2.0 V Note 9		110	360	μA
						160	420	μA
		Subsystem clock operation	f_{SUB} = 32.768kHz Note 5	T_A = –40°C Note 9		0.28	0.61	μA
						0.47	0.80	μA
				T_A = +25°C Note 9		0.34	0.61	μA
						0.53	0.80	μA
				T_A = +50°C Note 9		0.41	2.30	μA
						0.60	2.49	μA
				T_A = +70°C Note 9		0.64	4.03	μA
						0.83	4.22	μA
				T_A = +85°C Note 9		1.09	8.04	μA
						1.28	8.23	μA
STOP current Note 6, 8	I_{DD3}	T_A = –40°C				0.19	0.52	μA
		T_A = +25°C				0.25	0.52	μA
		T_A = +50°C				0.32	2.21	μA
		T_A = +70°C				0.55	3.94	μA
		T_A = +85°C				1.00	7.95	μA

(**Notes** and **Remarks** are listed on the next page.)

(3) Current for each peripheral circuit

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
Current when PCLBUZ0 and EXSLK_RF are connected together and MCU supplies RF slow clock to RF	I_{PCEX} Note 1				1.0		μA
RTC operating current	I_{RTC} Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} is 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1				75.0		μA
Thermometer sensor operating current	I_{TMPS} Note 1				75.0		μA
LVD operating current	I_{LVI} Note 1, 7				0.08		μA
Flash self-programming operating current	I_{FSP} Notes 1, 9				2.50	12.20	mA
BGO current	I_{BGO} Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 10		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Notes 1. Current flowing to V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the XT1 oscillator). The value of the current value of the RL78 microcontroller is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. Also, add the value of IFIL in case of selecting low-speed on-chip oscillator. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

4. Current flowing only to the 12 bit interval timer (including the operating current of the low-speed on-chip oscillator). The current value of the MCU is the sum of I_{DD1} or I_{DD2} and I_{IT} when f_{CLK} = f_{SUB} when the watchdog timer operates in STOP mode. When using low-speed on-chip oscillator, add I_{FIL}.

5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the MCU is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.

6. Current flowing only to the A/D converter. The current value of MCU is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

7. Current flowing only to the LVD circuit. The current value of MCU is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit is in operation.

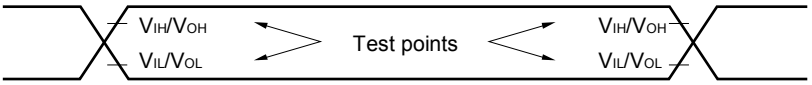
8. Current flowing when operates rewriting to Data flash.

9. Current flowing when operates flash self-programming.

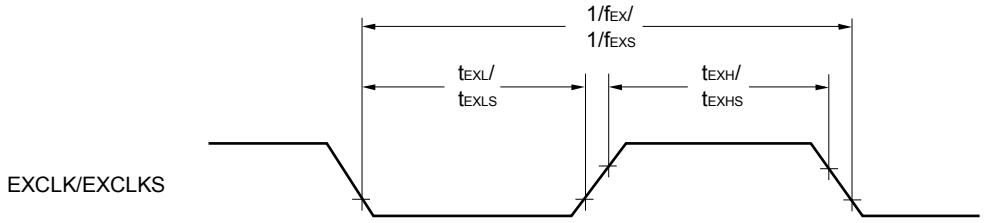
10. Shift time to the SNOOZE mode is referred User's Manual: Hardware.

(**Remarks** are listed on the next page.)

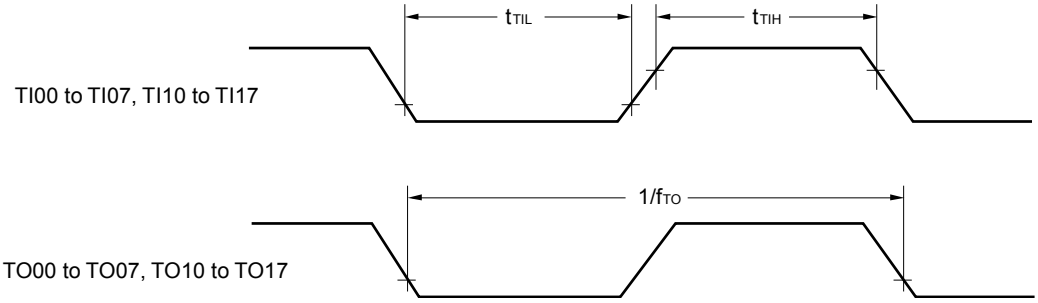
AC Timing Test Points



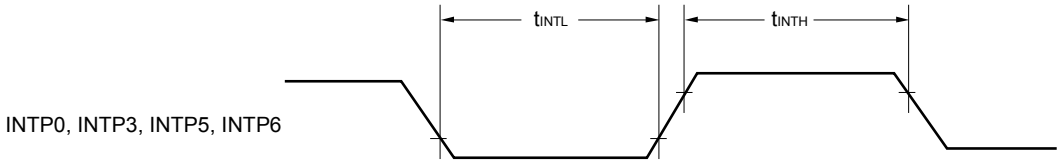
External System Clock Timing



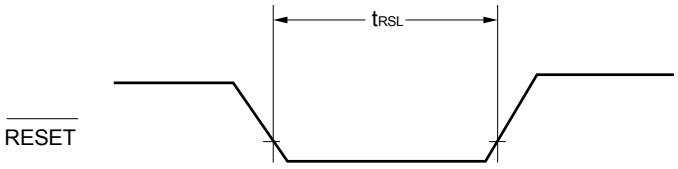
TI/TO Timing



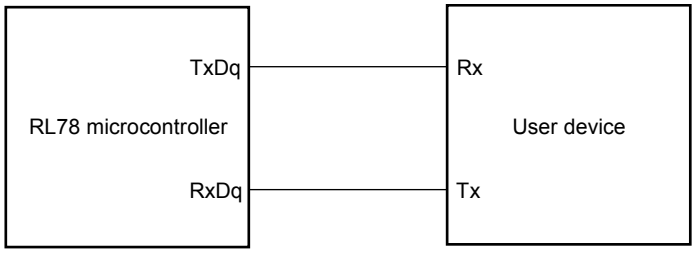
Interrupt Request Input Timing



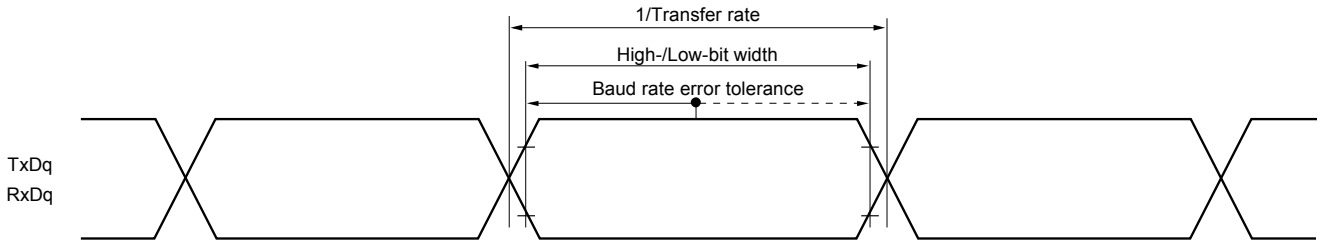
$\overline{\text{RESET}}$ Input Timing



UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01))

(3) During communication at same potential (CSI mode) (Internal communication, supporting CSI21 only)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ $2/f_{CLK}$ Note	2.4 V ≤ V_{DD} ≤ 3.6 V	250		250		500		ns
			1.8 V ≤ V_{DD} ≤ 3.6 V	–		250		500		ns
			1.6 V ≤ V_{DD} ≤ 3.6 V	–		–		500		ns

Note Use the f_{CLK} more than 6.5 MHz and lower than 24 MHz.

Remark This specification is for CSI21 only.

(4) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, supporting CSI00 and CSI20)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/ f_{CLK}	2.7 V ≤ V_{DD} ≤ 3.6 V	125		500		1000		ns
			2.4 V ≤ V_{DD} ≤ 3.6 V	250		500		1000		ns
			1.8 V ≤ V_{DD} ≤ 3.6 V	–		500		1000		ns
			1.6 V ≤ V_{DD} ≤ 3.6 V	–		–		1000		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V		t_{KCY1}/2 – 18		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		t_{KCY1}/2 – 38		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		t_{KCY1}/2 – 100		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V		44		110		110		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		75		110		110		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		110		110		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		220		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V		19		19		19		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		19		19		19		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		19		19		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		19		ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO1}	C = 30 pF Note 3	2.7 V ≤ V_{DD} ≤ 3.6 V		25		25		25	ns
			2.4 V ≤ V_{DD} ≤ 3.6 V		25		25		25	ns
			1.8 V ≤ V_{DD} ≤ 3.6 V		–		25		25	ns
			1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 10), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 0, 1)

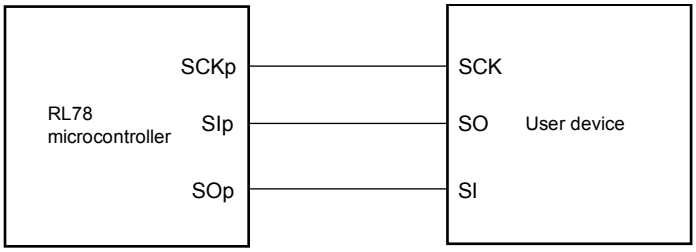
2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 11))

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

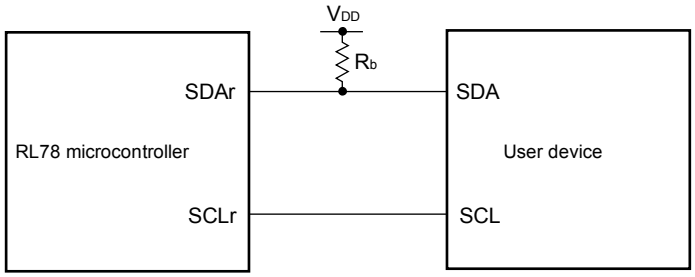
Remarks 1. p: CSI number (p = 00, 20), m: Unit number (m = 0, 1),
n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 10))

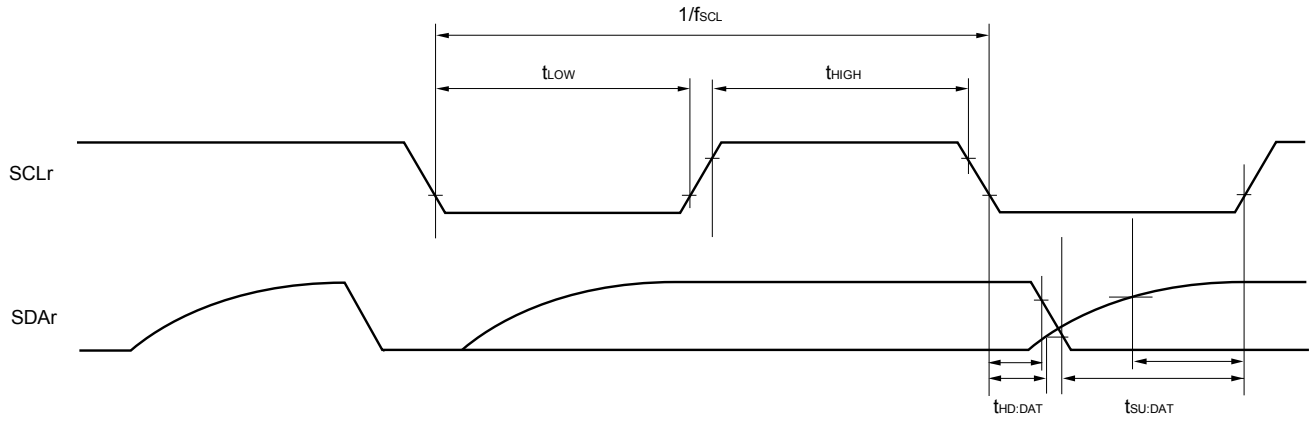
CSI mode connection diagram (during communication at same potential)



Simplified I²C mode mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remarks 1. R_b[Ω]:Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 20), g: PIM number (g =1), h: POM number (h = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clockw to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0), mn = 00, 02)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Delay time from SCKp↓ to SOp output Note 1, 3	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ		195		195		195	ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ		483		483		483	ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 5 C_b = 30 pF, R_b = 5.5 kΩ		–		483		483	ns
SIp setup time (to SCKp↓) Note 2, 4	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ	44		110		110		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ	110		110		110		ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 5 C_b = 30 pF, R_b = 5.5 kΩ	–		110		110		ns
SIp hold time (from SCKp↓) Note 2, 4	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 5 C_b = 30 pF, R_b = 5.5 kΩ	–		19		19		ns
Delay time from SCKp↑ to SOp output Note 2, 4	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 5 C_b = 30 pF, R_b = 5.5 kΩ		–		25		25	ns

Notes 1. Supporting CSI00 and CSI20.

2. Supporting CSI00 only.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

4. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. Use it with $V_{DD} \geq V_b$.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

(10) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	20/ f_{MCK}		–		–		ns
			20 MHz < f_{MCK} ≤ 24 MHz	16/ f_{MCK}		–		–		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/ f_{MCK}		–		–		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/ f_{MCK}		–		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/ f_{MCK}		–		ns
			f_{MCK} ≤ 4MHz	6/f_{MCK}		10/ f_{MCK}		10/ f_{MCK}		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V	24 MHz < f_{MCK}	48/ f_{MCK}		–		–		ns
			20 MHz < f_{MCK} ≤ 24 MHz	36/ f_{MCK}		–		–		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/ f_{MCK}		–		–		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/ f_{MCK}		–		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/ f_{MCK}		16/ f_{MCK}		–		ns
			f_{MCK} ≤ 4MHz	10/ f_{MCK}		10/ f_{MCK}		10/ f_{MCK}		ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2	24 MHz < f_{MCK}	–		–		–		ns
			20 MHz < f_{MCK} ≤ 24 MHz	–		–		–		ns
			16 MHz < f_{MCK} ≤ 20 MHz	–		–		–		ns
			8 MHz < f_{MCK} ≤ 16 MHz	–		–		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	–		16/ f_{MCK}		–		ns
			f_{MCK} ≤ 4MHz	–		10/ f_{MCK}		10/ f_{MCK}		ns

(**Notes** and **Caution** are listed on the next page.)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V	t_{KCY2}/2 – 18		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V	t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
		1.8 V ≤ V_{DD}<3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2	–		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 4.0 V	1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V	1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ V_{DD}<3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2	–		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 3	t_{KSI2}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 4.0 V	1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V	1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		1.8 V ≤ V_{DD}<3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2	–		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 4	t_{KSO2}	2.7 V ≤ V_{DD} < 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ		2/f_{MCK} + 214		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 30 pF, R_b = 5.5 kΩ		2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		1.8 V ≤ V_{DD}< 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 30 pF, R_b = 5.5 kΩ		–		2/f_{MCK} + 573		2/f_{MCK} + 573	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

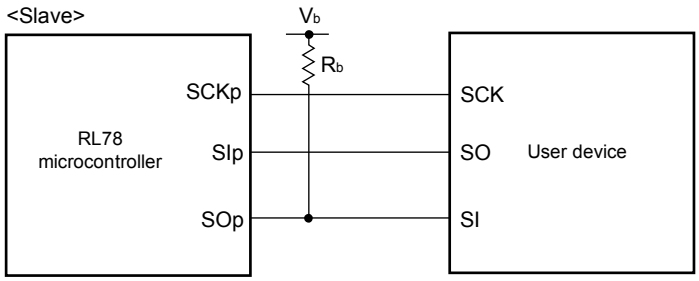
2. Use it with V_{DD} ≥ V_b.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



Remarks 1. R_b[Ω]:Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 20), m: Unit number, n: Channel number (mn = 00, 10), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 10))

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 135 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 100 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 100 pF, R_b = 5.5 kΩ	$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 100 pF, R_b = 5.5 kΩ	–		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 50 pF, R_b = 2.7 kΩ	0 Note 4	305	0 Note 4	305	0 Note 4	305	ns
		2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 100 pF, R_b = 2.7 kΩ	0 Note 4	355	0 Note 4	355	0 Note 4	355	ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 100 pF, R_b = 5.5 kΩ	0 Note 4	405	0 Note 4	405	0 Note 4	405	ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 100 pF, R_b = 5.5 kΩ	–	–	0 Note 4	405	0 Note 4	405	ns

Notes 1. The value must also be f_{MCK}/4 or lower.

2. Use it with $V_{DD} \geq V_b$.

3. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(2) I^2C fast mode

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ V_{DD} ≤ 3.6 V	0	400	0	400	0	400	kHz
			2.4 V ≤ V_{DD} ≤ 3.6 V	0	400	0	400	0	400	kHz
			1.8 V ≤ V_{DD} ≤ 3.6 V	–		0	400	0	400	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		μs
		2.4 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		0.6		0.6		μs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		μs
		2.4 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		0.6		0.6		μs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		1.3		μs
		2.4 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		1.3		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		1.3		1.3		μs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		μs
		2.4 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		0.6		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		100		100		100		μs
		2.4 V ≤ V_{DD} ≤ 3.6 V		100		100		100		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		100		100		μs
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0	0.9	0	0.9	0	0.9	μs
		2.4 V ≤ V_{DD} ≤ 3.6 V		0	0.9	0	0.9	0	0.9	μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		0	0.9	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		μs
		2.4 V ≤ V_{DD} ≤ 3.6 V		0.6		0.6		0.6		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		0.6		0.6		μs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		1.3		μs
		2.4 V ≤ V_{DD} ≤ 3.6 V		1.3		1.3		1.3		μs
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		1.3		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

2.8.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode
(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD} = V_{DD\_RF} = AV_{DD\_RF} \leq 3.6$ V, $V_{SS} = V_{SS\_RF} = AV_{SS\_RF}$ = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage	V_{LVI2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3	3.06	3.12	V
		V_{LVI3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.9	2.96	3.02	V
		V_{LVI4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.8	2.86	2.91	V
		V_{LVI5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.7	2.75	2.81	V
		V_{LVI6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.6	2.65	2.7	V
		V_{LVI7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.5	2.55	2.6	V
		V_{LVI8}	Power supply rise time	2.45	2.5	2.55	V
			Power supply fall time	2.4	2.45	2.5	V
		V_{LVI9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2	2.04	2.08	V
		V_{LVI10}	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.9	1.94	1.98	V
		V_{LVI11}	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.8	1.84	1.87	V
		V_{LVI12}	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.7	1.73	1.77	V
		V_{LVI13}	Power supply rise time	1.64	1.67	1.7	V
			Power supply fall time	1.6	1.63	1.66	V
Minimum pulse width		T_{LW}		300			μs
Detection delay time						300	μs

2.9.2 RF reception characteristics

Unless specified otherwise, the measurement is performed by our evaluation board.

(T_A = +25°C, V_{DD} = V_{DD_RF} = AV_{DD_RF} = 3.0 V, f = 2440 MHz, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RF input frequency	RF_{RXFRIN}			2402		2480	MHz
Maximum input level	RF_{LEVL}	PER ≤ 30.8% RF input pin	RF low power mode	-10	0	-	dBm
			RF normal mode	-10	1	-	dBm
			RF high performance mode	-10	1	-	dBm
Receiver sensitivity	RF_{STY}	PER ≤ 30.8%	RF low power mode	-	-60	-50	dBm
			RF normal mode	-	-90	-70	dBm
			RF high performance mode	-	-92	-70	dBm
Secondary radiation	RF_{RXSP}		30 MHz to 1 GHz	-	-72	-57	dBm/ 100 kHz
			1 GHz to 12 GHz	-	-57	-54	dBm/ 100 kHz
Common channel rejection ratio	RF_{CCR}	PER ≤ 30.8%, Prf = –67dBm		-21	-12	-	dB
Adjacent channel rejection ratio	RF_{ADCR}	PER ≤ 30.8% Prf = –67 dBm	±1 MHz	-15	-5	-	dB
			±2 MHz	17	29	-	dB
			±3 MHz	27	34	-	dB
Blocking	RF_{BLK}	PER ≤ 30.8% Prf = –67 dBm	30 MHz - 2000 MHz	-30	-13	-	dB
			2000 MHz to 2399 MHz	-35	-30	-	dBm
			2484 MHz to 3000 MHz	-35	-30	-	dBm
			> 3000 MHz	-30	-17	-	dBm
Frequency tolerance	RF_{RXFERR}	PER ≤ 30.8%		-250		+250	kHz
RSSI accuracy	RF_{RSSIS}	T_A = +25°C, –70 dBm ≤ Prf ≤ –10 dBm		-4	0	4	dB

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.