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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	32
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11aghdnb-20

- ROM, RAM capacities

Flash ROM	Data Flash	RAM	RL78/G1D
128 KB	8 KB	12 KB	R5F11AGG
192 KB	8 KB	16 KB	R5F11AGH
256 KB	8 KB	20 KB ^{Note}	R5F11AGJ

Note 19 KB when the self-programming function is used.

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G1D

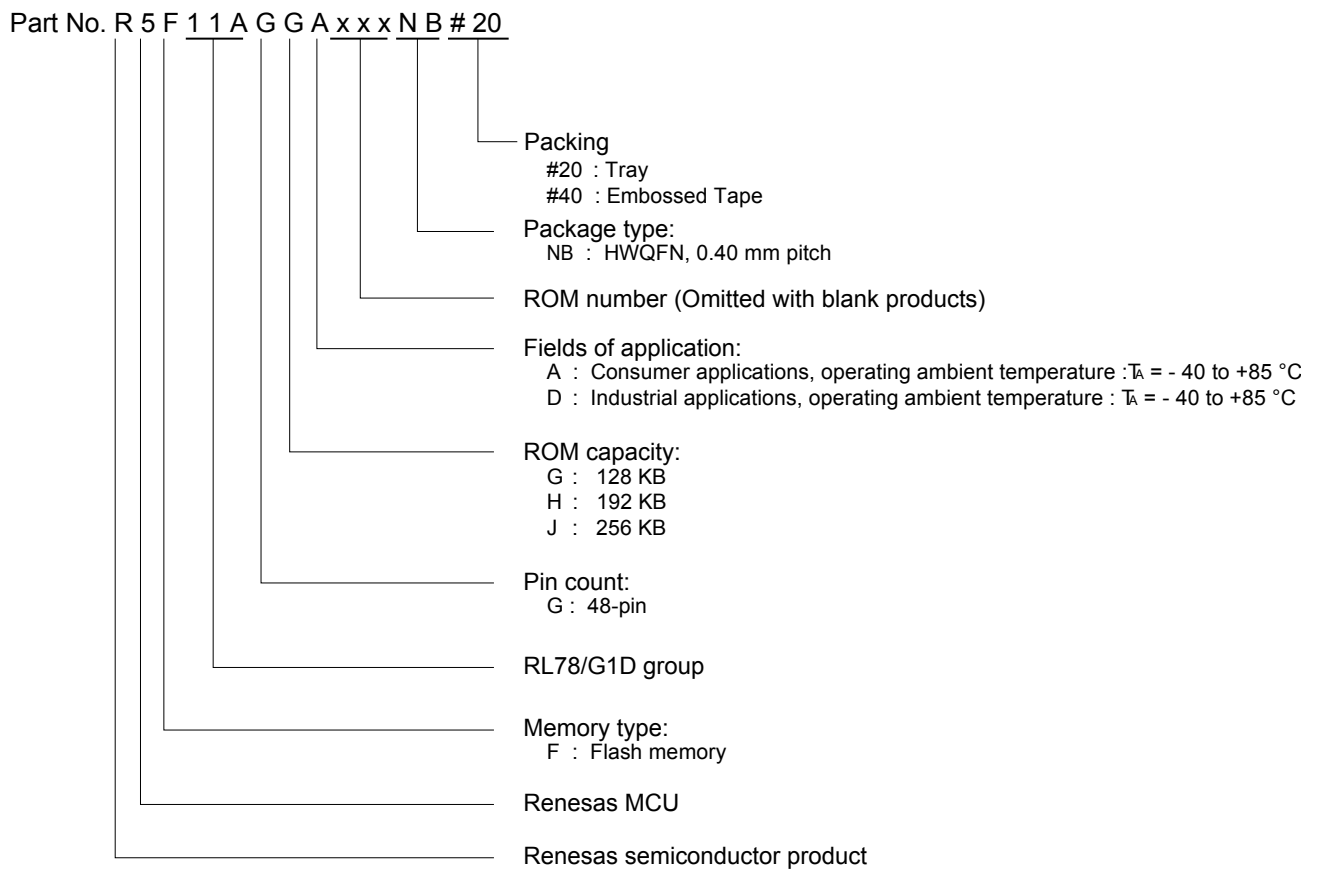


Table 1-1. List of Ordering Part Numbers

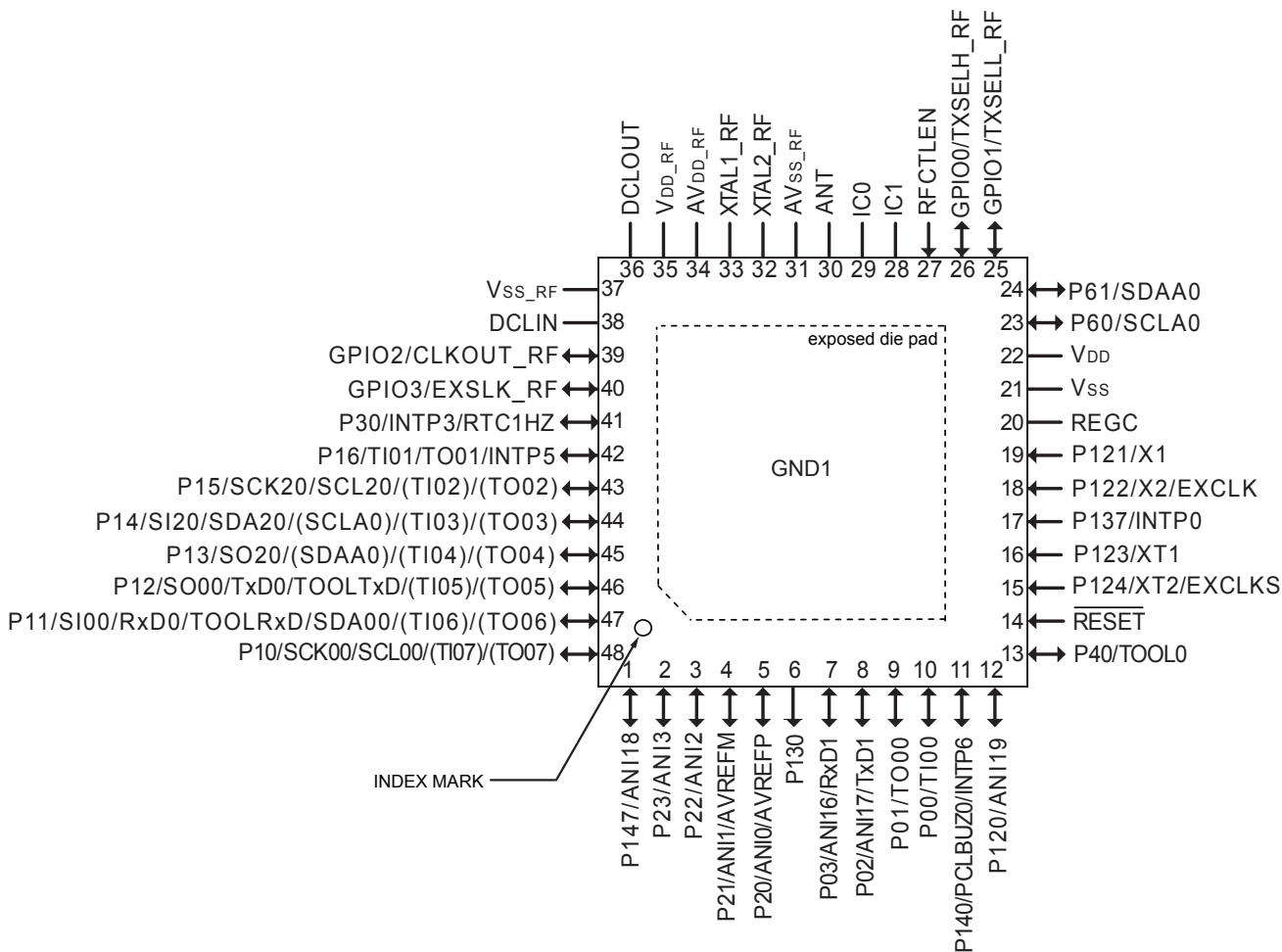
Pin count	Package	Fields of Application ^{Note}	Ordering Part Number	Code Flash Memory	Data Flash Memory
48 pins	Plastic WQFN (6 × 6)	A	R5F11AGGANB#20 R5F11AGGANB#40	128 KB	8 KB
		D	R5F11AGGDNB#20 R5F11AGGDNB#40		
		A	R5F11AGHANB#20 R5F11AGHANB#40	192 KB	8 KB
		D	R5F11AGHDNB#20 R5F11AGHDNB#40		
		A	R5F11AGJANB#20 R5F11AGJANB#40	256 KB	8 KB
		D	R5F11AGJDNB#20 R5F11AGJDNB#40		

Note For the fields of application, see Figure 1-1 Part Number, Memory Size, and Package of RL78/G1D.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

- <R> • 48-pin plastic WQFN (6 × 6 mm, 0.4 mm pitch)



- Cautions**
1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).
 2. Connect the metal pad (GND1) on the back of the package that has the same potential as AVSS_RF.

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)..

1.4 Pin Identification

ANI0 to ANI3, ANI16 to ANI19:	Analog input	PCLBUZ0:	Programmable clock output/buzzer output
ANT:	Antenna connection	REGC:	Regulator capacitance
AVDD_RF:	Power supply for RF analog	RFCTLEN:	RF control enable
AVREFM:	Analog reference voltage minus	RTC1HZ:	Real-time clock correction clock (1 Hz) output
AVREFP:	Analog reference voltage plus	$\overline{\text{RESET}}$:	Reset
AVSS_RF:	Ground for RF analog	RxD0, RxD1:	Receive data
CLKOUT_RF:	Clock output	SCLA0:	Serial clock input/output
DCLIN:	DC-DC converter inductor and DCLOUT capacitor	SCK00, SCK20, SCL00, SCL20:	Serial clock output
DCLOUT:	DC-DC converter output	SDAA0, SDA00, SDA20:	Serial data input/output
EXCLK:	External clock input (Main system clock)	SI00, SI20:	Serial data input
EXCLKS:	External clock input (Subsystem clock)	SO00, SO20:	Serial data output
EXSLK_RF:	External slow clock input	TI00 to TI07:	Timer input
GND1:	Package exposed die pad	TO00 to TO07:	Timer output
GPIO0 to GPIO3:	GPIO at RF unit	TOOL0:	Data input/output for tool
IC0, IC1:	Internal circuit	TOOLRxD, TOOLTxD:	Data input/output for external device
INTP0, INTP3, INTP5, INTP6:	External interrupt input	TxD0, TxD1:	Transmit data
P00 to P03:	Port 0	TXSELL_RF, TXSELH_RF:	External PA/LNA control
P10 to P16:	Port 1	VDD:	Power supply
P20 to P23:	Port 2	VDD_RF:	Power Supply for RF
P30:	Port 3	VSS:	Ground
P40:	Port 4	VSS_RF:	Ground for RF
P60, P61:	Port 6	X1, X2:	Crystal oscillator (Main system clock)
P120 to P124:	Port 12	XT1, XT2:	Crystal oscillator (Subsystem clock)
P130, P137:	Port 13	XTAL1_RF, XTAL2_RF:	Crystal oscillator (RF clock)
P140, P147:	Port 14		

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions	Ratings	Unit	
Output current, high	I _{OH1}	Per pin	(This is applicable to all pins listed below.)	-40	mA
		Total of all pins	P00, P01, P02, P03, P40, P120, P130, P140	-70	mA
		-170mA	P10, P11, P12, P13, P14, P15, P16, P30, P147	-100	mA
	I _{OH2}	Per pin	(This is applicable to all pins listed below.)	-0.5	mA
		Total of all pins	P20, P21, P22, P23	-2	mA
	I _{OHMRF}	Per pin	GPIO0, GPIO1, GPIO2, GPIO3	-17	mA
Output current, low	I _{OL1}	Per pin	(This is applicable to all pins listed below.)	40	mA
		Total of all pins	P00, P01, P02, P03, P40, P120, P130, P140	70	mA
		170mA	P10, P11, P12, P13, P14, P15, P16, P30, P60, P61, P147	100	mA
	I _{OL2}	Per pin	(This is applicable to all pins listed below.)	1	mA
		Total of all pins	P20, P21, P22, P23	5	mA
	I _{OLRF}	Per pin	GPIO0, GPIO1, GPIO2, GPIO3	17	mA
Operating ambient temperature	T _A	In normal operation mode	-40 to +85	°C	
		In flash memory programming mode	-40 to +85	°C	
Storage temperature	T _{stg}		-65 to +150	°C	

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
- 2.** AV_{REF(+)} : + side reference voltage of the A/D converter.
 - 3.** Reference voltage is V_{SS}.

2.3 Oscillator Characteristics

2.3.1 X1, XT1, XRF oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} = V_{DD_RF} = AV_{DD_RF} \leq 3.6\text{ V}$, $V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0\text{ V}$)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency ^{Note 1}	Ceramic resonator	f_x	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	1		20	MHz
	Crystal resonator		$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$	1		8	MHz
			$1.6\text{ V} \leq V_{DD} \leq 1.8\text{ V}$	1		4	MHz
XT1 clock oscillation frequency ^{Note 1}		f_{XT}		32	32.768	35	kHz
RF base clock oscillation frequency ^{Note 2}		f_{XRF}			32		MHz
RF base clock oscillation frequency accuracy ^{Note 2}		f_{XRFP}		-20		+20	ppm

- Notes**
1. Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time.
Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.
 2. This Oscillator characteristics is base clock for RF Transceiver.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user.

Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

2.3.2 On-chip oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} = V_{DD_RF} = AV_{DD_RF} \leq 3.6\text{ V}$, $V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0\text{ V}$)

Oscillators	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy	f_{IHP}	-20 to $+85^\circ\text{C}$	$1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-1.5		+1.5	%
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$	-5.0		+5.0	%
		-40 to -20°C	$1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-2.5		+2.5	%
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$	-5.5		+5.5	%
Low-speed on-chip oscillator clock frequency ^{Note 3}	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy	f_{ILP}			-15		+15	%
On-chip oscillator clock frequency for the RF slow clock ^{Note 3}	f_{ILRF}				32.768		kHz
On-chip oscillator clock frequency accuracy for the RF slow clock	f_{ILRFP}			-0.025		0.025	%

- Notes**
1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.
 2. This indicates the oscillator characteristics only. Refer to **AC Characteristics** for instruction execution time.
 3. This indicates the oscillator characteristics only.

2.4 DC Characteristics

2.4.1 Output current

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} = V_{DD_RF} = AV_{DD_RF} \leq 3.6\text{ V}$, $V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, high ^{Note 1}	I _{OH1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	Per pin	$1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		$-10.0^{\text{Note 2}}$	mA
			Total ^{Note 3}	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		-10.0	mA
		P00, P01, P02, P03, P40, P120, P130, P140	Total ^{Note 3}	$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$		-5.0	mA
				$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$		-2.5	mA
	P10, P11, P12, P13, P14, P15, P16, P30, P147	Total ^{Note 3}	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		-19.0	mA	
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$		-10.0	mA	
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$		-5.0	mA	
	Total of all pins ^{Note 3}		$1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		$-135.0^{\text{Note 4}}$	mA	
	I _{OH2}	P20, P21, P22, P23	Per pin	$1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		$-0.1^{\text{Note 2}}$	mA
			Total ^{Note 3}	$1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		-1.5	mA
I _{OH_{RF}}	GPIO0, GPIO1, GPIO2, GPIO3	Per pin	$1.6\text{ V} \leq V_{DD_RF} \leq 3.6\text{ V}$		-2.0	mA	
Output current, low ^{Note 1}	I _{OL1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	Per pin	$1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		$20.0^{\text{Note 2}}$	mA
			Per pin	$1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		$15.0^{\text{Note 2}}$	mA
		P00, P01, P02, P03, P40, P120, P130, P140	Total ^{Note 3}	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		15.0	mA
				$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$		9.0	mA
	$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$				4.5	mA	
	P10, P11, P12, P13, P14, P15, P16, P30, P60, P61, P147	Total ^{Note 3}	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		35.0	mA	
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$		20.0	mA	
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$		10.0	mA	
	Total of all pins ^{Note 3}		$1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		150.0	mA	
	I _{OL2}	P20, P21, P22, P23	Per pin	$1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		$0.4^{\text{Note 2}}$	mA
Total ^{Note 3}			$1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		5.0	mA	
I _{OL_{RF}}	GPIO0, GPIO1, GPIO2, GPIO3	Per pin	$1.6\text{ V} \leq V_{DD_RF} \leq 3.6\text{ V}$		2.0	mA	

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. However, do not exceed the total current value.
3. Specification under conditions where the duty factor $\leq 70\%$.

The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = $(I_{OH} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 50\%$ and $I_{OH} = -10.0\text{ mA}$

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(50 \times 0.01) = -14.0\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. Product for industrial applications (R5F11AGGDNB, R5F11AGHDNB, R5F11AGJDNB) is -100.0 mA .

(Caution and Remark are listed on the next page.)

Caution P00, P02, P03, and P10 to P15 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.4.2 Input current

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} = V_{DD_RF} = AV_{DD_RF} \leq 3.6\text{ V}$, $V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	V_{IH1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	Normal mode ($I_{THL} = 1$)	$0.8V_{DD}$		V_{DD}	V
	V_{IH2}	P01, P03, P10, P11, P13, P14, P15, P16	TTL mode $3.3\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	2.0		V_{DD}	V
			TTL mode $1.6\text{ V} \leq V_{DD} < 3.3\text{ V}$	1.5		V_{DD}	V
	V_{IH3}	P20, P21, P22, P23		$0.7V_{DD}$		V_{DD}	V
	V_{IH4}	P60, P61		$0.7V_{DD}$		6.0	V
	V_{IH5}	P121, P122, P123, P124, P137, RESET		$0.8V_{DD}$		V_{DD}	V
	V_{IHRF}	GPIO0, GPIO1, GPIO2, GPIO3		$0.85V_{DD_RF}$		V_{DD_RF}	V
Input voltage, low	V_{IL1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P140, P147	Normal mode ($I_{THL} = 1$)	0		$0.2V_{DD}$	V
	V_{IL2}	P01, P03, P10, P11, P13, P14, P15, P16	TTL mode $3.3\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	0		0.5	V
			TTL mode $1.6\text{ V} \leq V_{DD} < 3.3\text{ V}$	0		0.32	V
	V_{IL3}	P20, P21, P22, P23		0		$0.3V_{DD}$	V
	V_{IL4}	P60, P61		0		$0.3V_{DD}$	V
	V_{IL5}	P121, P122, P123, P124, P137, RESET		0		$0.2V_{DD}$	V
	V_{ILRF}	GPIO0, GPIO1, GPIO2, GPIO3		0		$0.1V_{DD_RF}$	V

Caution The maximum value of V_{IH} of pins P00, P02, P03, and P10 to P15 is V_{DD} , even in the N-ch open-drain mode.

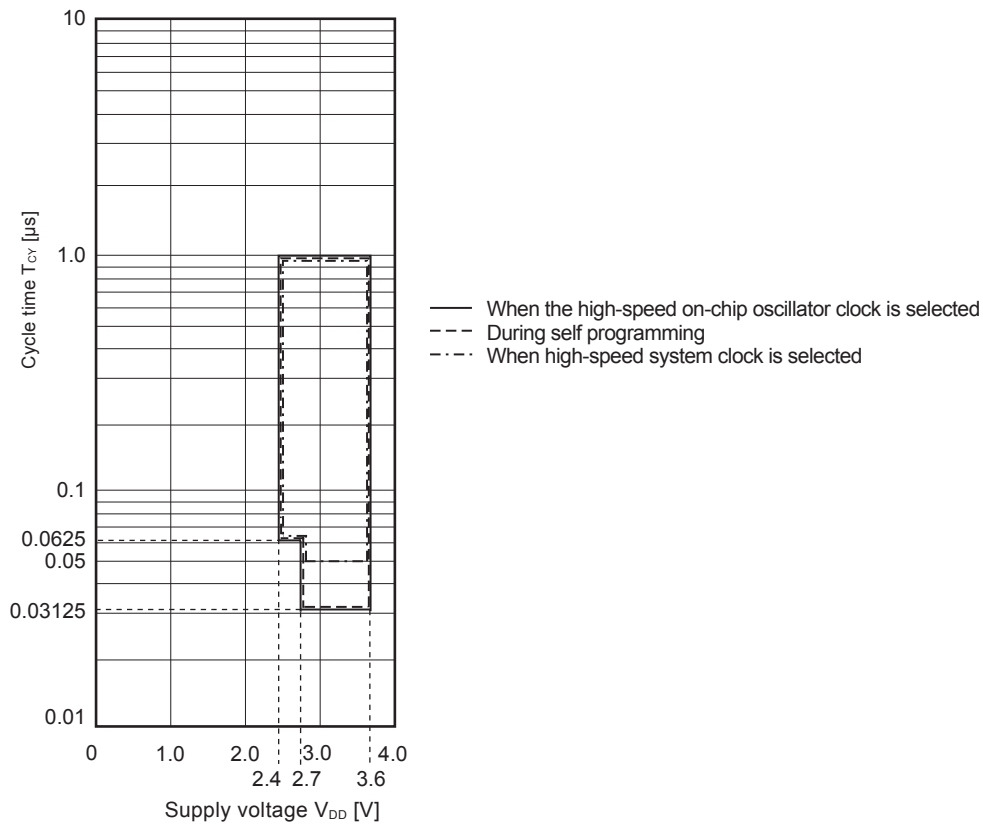
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} = V_{DD_RF} = AV_{DD_RF} \leq 3.6\text{ V}$, $V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0\text{ V}$) (2/2)

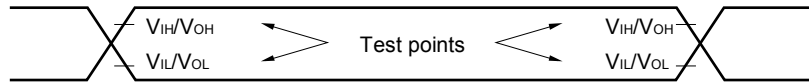
Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Interrupt input high-level width, low-level width	t_{INTH} , t_{INTL}	INTP0, INTP3, INTP5, INTP6	1			μs
External PA control output High-level width	t_{PAHRF}	TXSELH_RF	283			μs
External PA control output low-level width	t_{PALRF}	TXSELL_RF	283			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	$\overline{\text{RESET}}$	10			μs
$\overline{\text{RESET_RF}}$ internal pin low-level width	t_{RSTLRF}	$\overline{\text{RESET_RF}}$ internal pin	31			μs

Minimum Instruction Execution Time during Main System Clock Operation

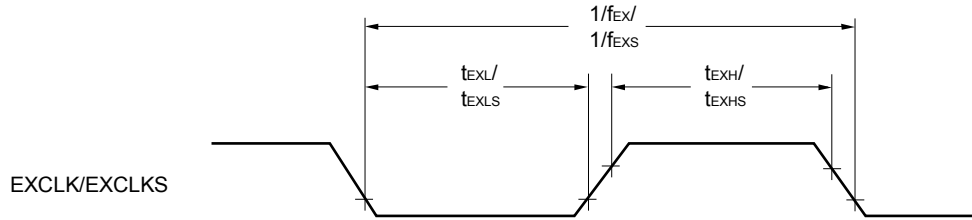
T_{CY} vs V_{DD} (HS (high-speed main) mode)



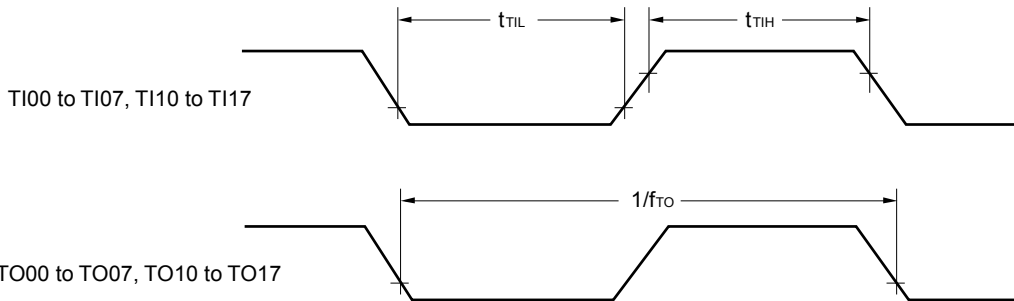
AC Timing Test Points



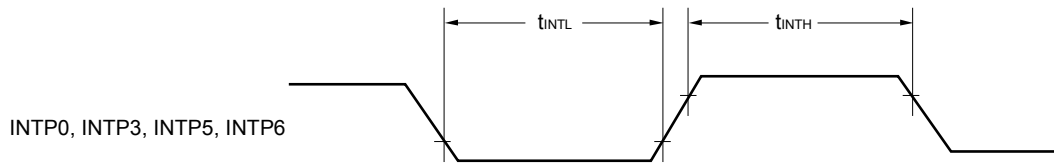
External System Clock Timing



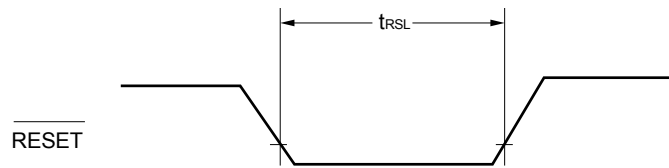
TI/TO Timing

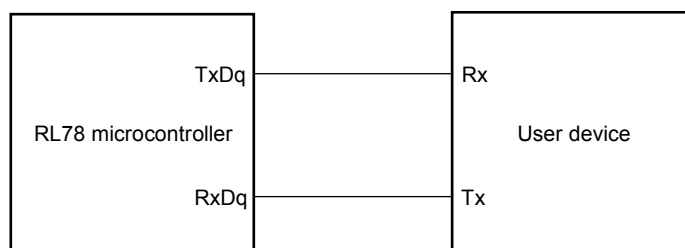
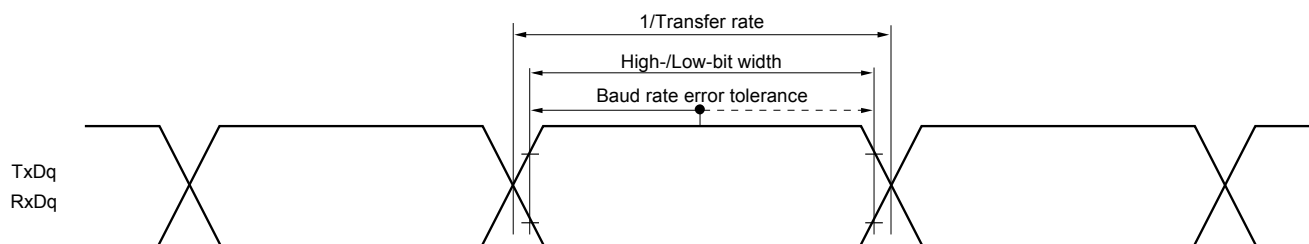


Interrupt Request Input Timing



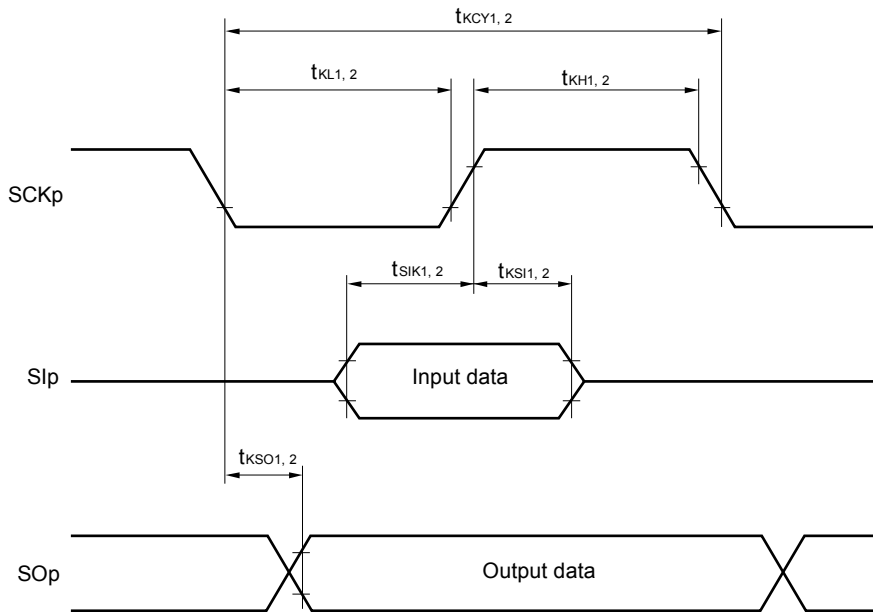
RESET Input Timing



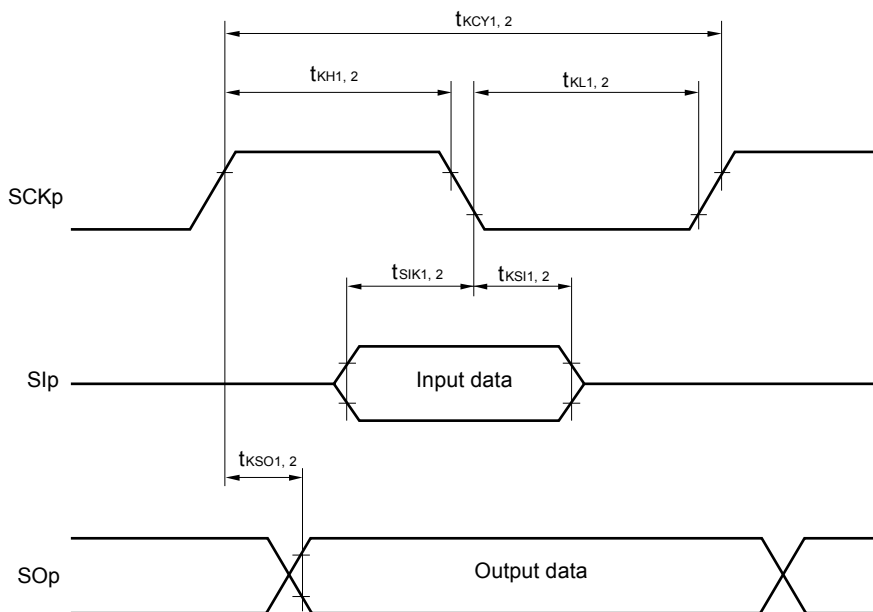
UART mode connection diagram (during communication at same potential)**UART mode bit width (during communication at same potential) (reference)**

- Remarks 1.** q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)
- 2.** f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00, 01))

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks**
1. p: CSI number (p = 00, 10, 21)
 2. m: Unit number, n: Channel number (mn = 00, 02, 11)

(9) Communication at different potential (1.8 V, 2.5 V) (CSI mode: master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

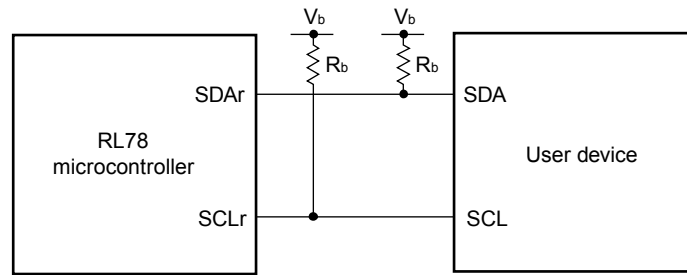
(1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK}	2.7 V ≤ V _{DD} ≤ 3.6 V 2.3 V ≤ V _b ≤ 2.7 V C _b = 30 pF, R _b = 2.7 kΩ	500		1150		1150		ns
			2.4 V ≤ V _{DD} < 3.3 V 1.6 V ≤ V _b ≤ 2.0 V C _b = 30 pF, R _b = 5.5 kΩ	1150		1150		1150		ns
			1.8 V ≤ V _{DD} < 3.3 V 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} C _b = 30 pF, R _b = 5.5 kΩ	–		1150		1150		ns
SCKp high-level width Note 1	t _{KH1}	2.7 V ≤ V _{DD} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1/2} - 170		t _{KCY1/2} - 170		t _{KCY1/2} - 170		ns	
			2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1/2} - 458		t _{KCY1/2} - 458		t _{KCY1/2} - 458		ns
			1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} C _b = 30 pF, R _b = 5.5 kΩ	–		t _{KCY1/2} - 458		t _{KCY1/2} - 458		ns
SCKp low-level width Note 1	t _{KL1}	2.7 V ≤ V _{DD} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1/2} - 18		t _{KCY1/2} - 50		t _{KCY1/2} - 50		ns	
			2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1/2} - 50		t _{KCY1/2} - 50		t _{KCY1/2} - 50		ns
			1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} C _b = 30 pF, R _b = 5.5 kΩ	–		t _{KCY1/2} - 50		t _{KCY1/2} - 50		ns
Slp setup time (to SCKp↑) Note 1, 2	t _{SIK1}	2.7 V ≤ V _{DD} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V C _b = 30 pF, R _b = 2.7 kΩ	177		479		479		ns	
			2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V C _b = 30 pF, R _b = 5.5 kΩ	479		479		479		ns
			1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} C _b = 30 pF, R _b = 5.5 kΩ	–		479		479		ns
Slp hold time (from SCKp↑) Note 1, 2	t _{SI1}	2.7 V ≤ V _{DD} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V C _b = 30 pF, R _b = 2.7 kΩ	19		19		19		ns	
			2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V C _b = 30 pF, R _b = 5.5 kΩ	19		19		19		ns
			1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} C _b = 30 pF, R _b = 5.5 kΩ	–		19		19		ns

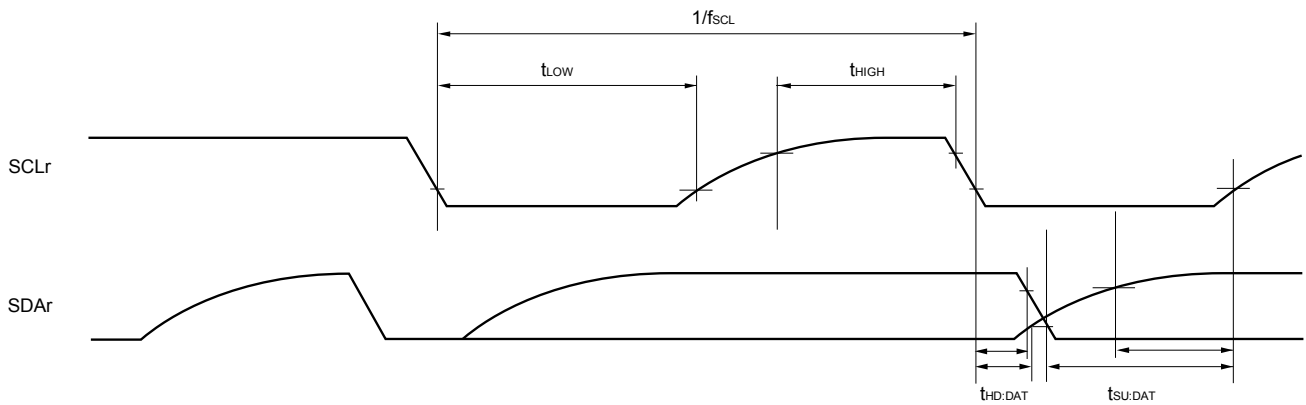
Notes 1. Supporting CSI00 and CSI20.**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.**3.** Use it with V_{DD} ≥ V_b.

(Caution are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
 2. r: IIC number (r = 00, 10), g: PIM, POM number (g = 0, 1)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02))

(3) I²C fast mode plus

(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

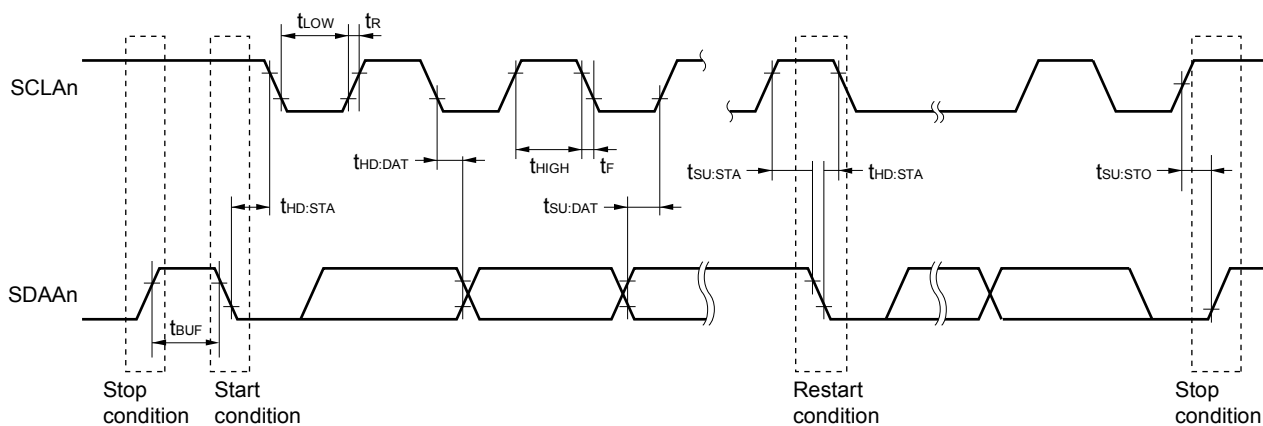
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode plus: f _{CLK} ≥ 10 MHz 2.7 V ≤ V _{DD} ≤ 3.6 V	0	1000	–	–	–	–	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ V _{DD} ≤ 3.6 V	0.26		–	–	–	–	μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ V _{DD} ≤ 3.6 V	0.26		–	–	–	–	μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ V _{DD} ≤ 3.6 V	0.5		–	–	–	–	μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ V _{DD} ≤ 3.6 V	0.26		–	–	–	–	μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ V _{DD} ≤ 3.6 V	50		–	–	–	–	μs
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ V _{DD} ≤ 3.6 V	0	0.45	–	–	–	–	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ V _{DD} ≤ 3.6 V	0.26		–	–	–	–	μs
Bus-free time	t _{BUF}	2.7 V ≤ V _{DD} ≤ 3.6 V	0.5		–	–	–	–	μs

- Notes**
- The first clock pulse is generated after this period when the start/restart condition is detected.
 - The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the \overline{ACK} (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

I²C serial transfer timing



Remark n = 0

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), conversion target : ANI16 to ANI19

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} = V_{DD_RF} = AV_{DD_RF} \leq 3.6\text{ V}$, $V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Resolution	RES			8		10	bit	
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$1.8\text{ V} \leq AV_{REFP} \leq 3.6\text{ V}$		1.2	± 5.0	LSB	
			$1.6\text{ V} \leq AV_{REFP} \leq 3.6\text{ V}$ ^{Note 4}		1.2	± 8.5	LSB	
Conversion time	T_{conv}	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	3.1875		39	μs	
			$1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		17		39	μs
			$1.6\text{ V} \leq AV_{REFP} \leq 3.6\text{ V}$		57		95	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$1.8\text{ V} \leq AV_{REFP} \leq 3.6\text{ V}$			± 0.35	%FSR	
			$1.6\text{ V} \leq AV_{REFP} \leq 3.6\text{ V}$ ^{Note 4}			± 0.60	%FSR	
Full-scale error ^{Notes 1, 2}	E_{FS}	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$1.8\text{ V} \leq AV_{REFP} \leq 3.6\text{ V}$			± 0.35	%FSR	
			$1.6\text{ V} \leq AV_{REFP} \leq 3.6\text{ V}$ ^{Note 4}			± 0.60	%FSR	
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$1.8\text{ V} \leq AV_{REFP} \leq 3.6\text{ V}$			± 3.5	LSB	
			$1.6\text{ V} \leq AV_{REFP} \leq 3.6\text{ V}$ ^{Note 4}			± 6.0	LSB	
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$1.8\text{ V} \leq AV_{REFP} \leq 3.6\text{ V}$			± 2.0	LSB	
			$1.6\text{ V} \leq AV_{REFP} \leq 3.6\text{ V}$ ^{Note 4}			± 2.5	LSB	
Analog input voltage	V_{AIN}			0		AV_{REFP} and V_{DD}	V	

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, MAX. value is following.

Overall error: ± 4 LSB is added to the MAX. value of $AV_{REFP} = V_{DD}$.

Zero-scale error / Full-scale error: ± 0.2 %FSR is added to the MAX. value of $AV_{REFP} = V_{DD}$.

Integral linearity error / Differential linearity error: ± 2 LSB is added to the MAX. value n of $AV_{REFP} = V_{DD}$.

4. When the the conversion time is set to 57 μs (min.) and 95 μs (max.).

2.8.2 Temperature sensor and internal reference voltage characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} = V_{DD_RF} = AV_{DD_RF} \leq 3.6\text{ V}$, $V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0\text{ V}$, HS (high-speed main) mode)

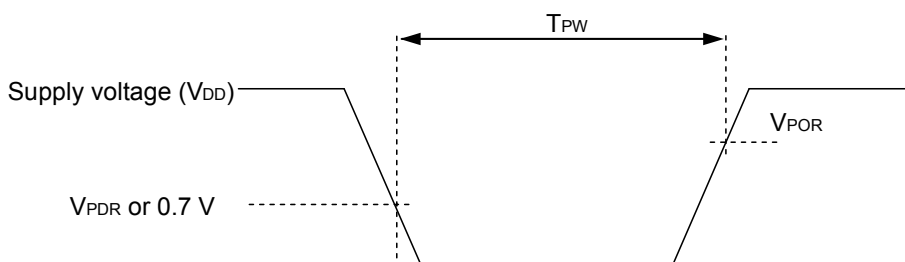
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{TMPS}	Temperature sensor output voltage that depends on the temperature		-3.6		mV/ $^\circ\text{C}$
Operation stabilization wait time	t_{AMP}		5			μs

2.8.3 POR circuit characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Rise time	1.47	1.51	1.55	V
	V_{PDR}	Fall time	1.46	1.50	1.54	V
Minimum pulse width ^{Note}	T_{PW}	Other than STOP/SUB_RUN/SUB_HALT	300			μs

Note This is the time required for the POR circuit to execute a reset operation when V_{DD} falls below V_{PDR} . When the main system clock (f_{MAIN}) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC) or when the microcontroller enters STOP mode, this is the time required for the POR circuit to execute a reset operation between when V_{DD} falls below 0.7 V and when V_{DD} rises to V_{POR} or higher.



LVD Detection Voltage of Interrupt & Reset Mode**($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} = V_{DD_RF} = AV_{DD_RF} \leq 3.6\text{ V}$, $V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Interrupt and reset mode	V _{LVDA0}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 0, 0, falling reset voltage	1.60	1.63	1.66	V	
	V _{LVDA1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	V _{LVDA2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.8	1.84	1.87	V
	V _{LVDA3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V _{LVDB0}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 0, 1, falling reset voltage	1.80	1.84	1.87	V	
	V _{LVDB1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V _{LVDB2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V _{LVDB3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V _{LVDC0}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 0, falling reset voltage	2.40	2.45	2.50	V	
	V _{LVDC1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V _{LVDC2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
Falling interrupt voltage			2.60	2.65	2.70	V	
V _{LVDD0}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 1, falling reset voltage	2.70	2.75	2.81	V		
V _{LVDD1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V	
		Falling interrupt voltage	2.80	2.86	2.91	V	
V _{LVDD2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V	
		Falling interrupt voltage	2.90	2.96	3.02	V	

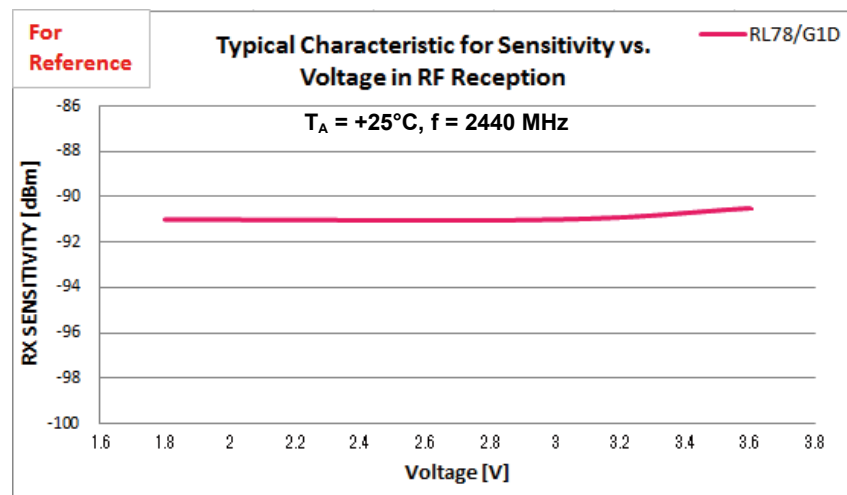
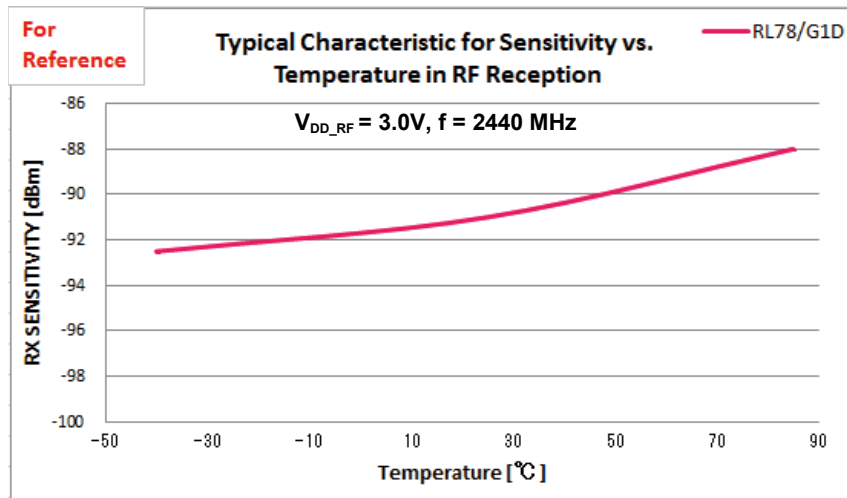
2.8.5 Supply voltage rise time**($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V _{DD} rise slope	S _{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.6 AC Characteristics.

(4) RF Reception Sensitivity

Unless specified otherwise, the measurement is performed by our evaluation board.
 Current consumption is not including MCU unit.



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