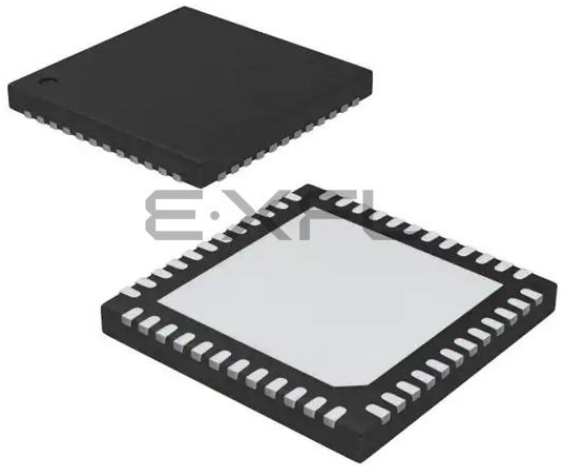

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	32
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11agjanb-20

2.4 DC Characteristics

2.4.1 Output current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			–10.0[Note 2]	mA
		P00, P01, P02, P03, P40, P120, P130, P140	Total[Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V			–10.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			–5.0	mA
				1.6 V ≤ V_{DD} < 1.8 V			–2.5	mA
		P10, P11, P12, P13, P14, P15, P16, P30, P147	Total[Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V			–19.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			–10.0	mA
				1.6 V ≤ V_{DD} < 1.8 V			–5.0	mA
		Total of all pins[Note 3]		1.6 V ≤ V_{DD} ≤ 3.6 V			–135.0[Note 4]	mA
	I_{OH2}	P20, P21, P22, P23	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			–0.1[Note 2]	mA
			Total[Note 3]	1.6 V ≤ V_{DD} ≤ 3.6 V			–1.5	mA
	I_{OHRF}	GPIO0, GPIO1, GPIO2, GPIO3	Per pin	1.6 V ≤ V_{DD_RF} ≤ 3.6 V			–2.0	mA
Output current, low[Note 1]	I_{OL1}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			20.0[Note 2]	mA
		P60, P61	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			15.0[Note 2]	mA
		P00, P01, P02, P03, P40, P120, P130, P140	Total[Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V			15.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
				1.6 V ≤ V_{DD} < 1.8 V			4.5	mA
		P10, P11, P12, P13, P14, P15, P16, P30, P60, P61, P147	Total[Note 3]	2.7 V ≤ V_{DD} ≤ 3.6 V			35.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			20.0	mA
				1.6 V ≤ V_{DD} < 1.8 V			10.0	mA
		Total of all pins[Note 3]		1.6 V ≤ V_{DD} ≤ 3.6 V			150.0	mA
	I_{OL2}	P20, P21, P22, P23	Per pin	1.6 V ≤ V_{DD} ≤ 3.6 V			0.4[Note 2]	mA
			Total[Note 3]	1.6 V ≤ V_{DD} ≤ 3.6 V			5.0	mA
	I_{OLRF}	GPIO0, GPIO1, GPIO2, GPIO3	Per pin	1.6 V ≤ V_{DD_RF} ≤ 3.6 V			2.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 50% and I_{OH} = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(50 × 0.01) = –14.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. Product for industrial applications (R5F11AGGDNB, R5F11AGHDNB, R5F11AGJDNB) is –100.0 mA.

(**Caution** and **Remark** are listed on the next page.)

Notes 1. Current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 4 MHz

8. If operation of the subsystem clock when STOP mode, same as when HALT mode of subsystem clock operation.

9. The upper value is for square-wave input and the lower is with an oscillator connected.

Remarks 1. f_{MX}: High-speed system clock frequency (External main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(3) Current for each peripheral circuit

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
Current when PCLBUZ0 and EXSLK_RF are connected together and MCU supplies RF slow clock to RF	I_{PCEX} Note 1				1.0		μA
RTC operating current	I_{RTC} Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} is 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1				75.0		μA
Thermometer sensor operating current	I_{TMPS} Note 1				75.0		μA
LVD operating current	I_{LVI} Note 1, 7				0.08		μA
Flash self-programming operating current	I_{FSP} Notes 1, 9				2.50	12.20	mA
BGO current	I_{BGO} Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 10		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Notes 1. Current flowing to V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the XT1 oscillator). The value of the current value of the RL78 microcontroller is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. Also, add the value of IFIL in case of selecting low-speed on-chip oscillator. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

4. Current flowing only to the 12 bit interval timer (including the operating current of the low-speed on-chip oscillator). The current value of the MCU is the sum of I_{DD1} or I_{DD2} and I_{IT} when f_{CLK} = f_{SUB} when the watchdog timer operates in STOP mode. When using low-speed on-chip oscillator, add I_{FIL}.

5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the MCU is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.

6. Current flowing only to the A/D converter. The current value of MCU is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

7. Current flowing only to the LVD circuit. The current value of MCU is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit is in operation.

8. Current flowing when operates rewriting to Data flash.

9. Current flowing when operates flash self-programming.

10. Shift time to the SNOOZE mode is referred User's Manual: Hardware.

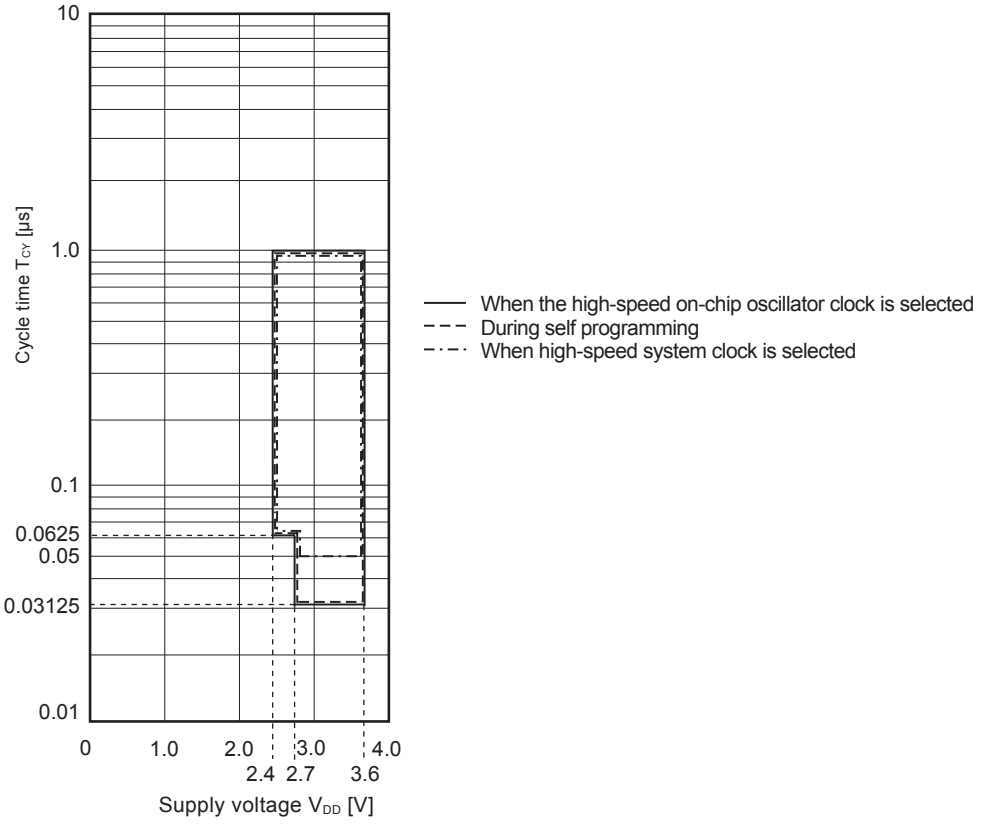
(**Remarks** are listed on the next page.)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) (2/2)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0, INTP3, INTP5, INTP6	1			µs
External PA control output High-level width	t_{PAHRF}	TXSELH_RF	283			µs
External PA control output low-level width	t_{PALRF}	TXSELL_RF	283			µs
$\overline{RESET}$ low-level width	t_{RSL}	$\overline{RESET}$	10			µs
$\overline{RESET\_RF}$ internal pin low-level width	t_{RSTLRF}	$\overline{RESET\_RF}$ internal pin	31			µs

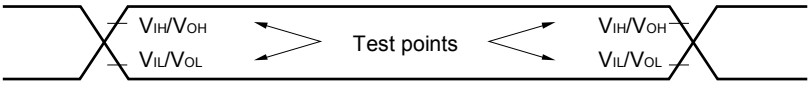
Minimum Instruction Execution Time during Main System Clock Operation

T_{CY} vs V_{DD} (HS (high-speed main) mode)



2.7 Peripheral Functions Characteristics

AC Timing Test Points



2.7.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode	LS (low-speed main) Mode	LV (low-voltage main) Mode	Unit
			MAX.	MAX.	MAX.	
Transfer rate Note 1		2.4 V ≤ V_{DD} ≤ 3.6 V	f_{MCK}/6	f_{MCK}/6	f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2	5.3	1.3	0.6	Mbps
		1.8 V ≤ V_{DD} ≤ 3.6 V	–	f_{MCK}/6	f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2	–	1.3	0.6	Mbps
		1.6 V ≤ V_{DD} ≤ 3.6 V	–	–	f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2	–	–	0.6	Mbps

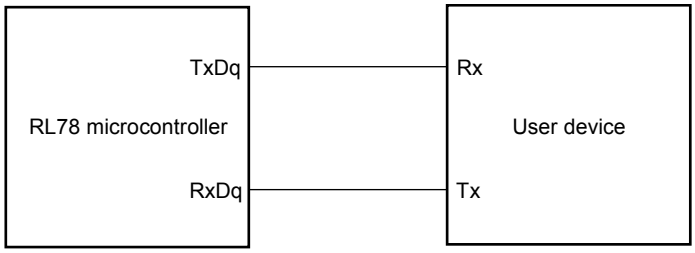
Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. Maximum operating frequency of CPU and peripheral hardware clock (f_{CLK}) is following

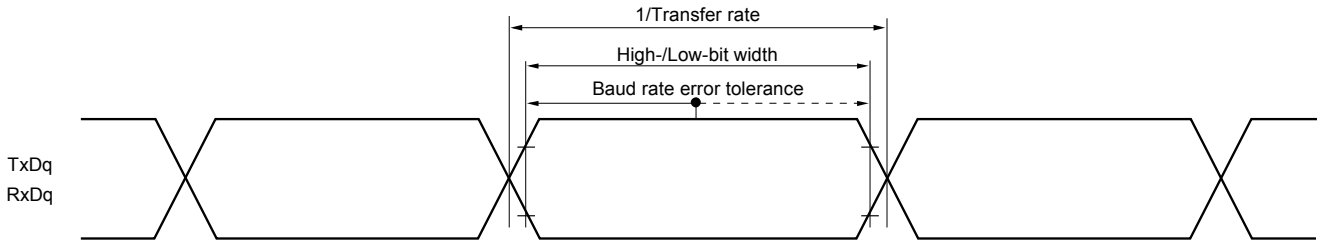
HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 3.6 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 3.6 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 3.6 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 3.6 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01))

(5) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input, supporting CSI00 and CSI20)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 4	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 3.6 V	f_{MCK} > 16 MHz	8/f_{MCK}		–		–		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		
		2.4 V ≤ V_{DD} ≤ 3.6 V		6/f_{MCK} and 500		6/f_{MCK} and 500		6/f_{MCK} and 500		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		6/f_{MCK} and 750		6/f_{MCK} and 750		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		6/f_{MCK} and 1500		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ V_{DD} ≤ 3.6 V		t_{KCY2}/2–8		t_{KCY2}/2–8		t_{KCY2}/2–8		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		t_{KCY2}/2–18		t_{KCY2}/2 – 18		t_{KCY2}/2 – 18		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		t_{KCY2}/2 – 18		t_{KCY2}/2 – 18		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		t_{KCY2}/2 – 66		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 3.6 V		1/f_{MCK} +20		1/f_{MCK} +30		1/f_{MCK} +30		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		1/f_{MCK} +30		1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		1/f_{MCK} +40		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI2}	2.4 V ≤ V_{DD} ≤ 3.6 V		1/f_{MCK} +31		1/f_{MCK} +31		1/f_{MCK} +31		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		–		1/f_{MCK} +31		1/f_{MCK} +31		ns
		1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		1/f_{MCK} +250		ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO2}	C = 30 pF Note 3	2.7 V ≤ V_{DD} ≤ 3.6 V		2/f_{MCK}+ 44		2/f_{MCK}+ 110		2/f_{MCK}+ 110	ns
			2.4 V ≤ V_{DD} ≤ 3.6 V		2/f_{MCK}+ 75		2/f_{MCK}+ 110		2/f_{MCK}+ 110	ns
			1.8 V ≤ V_{DD} ≤ 3.6 V		–		2/f_{MCK}+ 110		2/f_{MCK}+ 110	ns
			1.6 V ≤ V_{DD} ≤ 3.6 V		–		–		2/f_{MCK}+ 220	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. C is the load capacitance of the SOp output lines.

4. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

(**Caution** and **Remarks** are listed on the next page.)

(7) Communication at different potential (1.8 V, 2.5 V) (UART mode)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode	LS (low-speed main) Mode	LV (low-voltage main) Mode	Unit
				MAX.	MAX.	MAX.	
Transfer rate		Reception	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V	f_{MCK}/6 Note 1	f_{MCK}/6 Note 1	f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3	5.3	1.3	0.6	Mbps
			2.4 V ≤ V_{DD} ≤ 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	f_{MCK}/6 Note 1	f_{MCK}/6 Note 1	f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3	2.6	1.3	0.6	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	–	f_{MCK}/6 Notes 1, 2	f_{MCK}/6 Notes 1, 2	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3	–	1.3	1.3	Mbps
		Transmission	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V	**Note 4**	**Note 4**	**Note 4**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V	1.2 Note 5	1.2 Note 5	1.2 Note 5	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	**Notes 2, 6**	**Notes 2, 6**	**Notes 2, 6**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V	0.43	0.43	0.43	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V	–	**Notes 2, 6**	**Notes 2, 6**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V	–	0.43 Notes 7	0.43 Notes 7	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. Use it with $V_{DD} \geq V_b$.

3. Maximum operating frequency of CPU and peripheral hardware clock (f_{CLK}) is following

HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 3.6 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 3.6 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 3.6 V)
LV (low-voltage main) mode: 4 MHz (1.8 V ≤ V_{DD} ≤ 3.6 V)

4. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} ≤ 3.6 V and 2.3 V ≤ Vb ≤ 2.7 V

Maximum transfer rate = 1/{-Cb × Rb × ln (1 - 2.0/Vb)} × 3 [bps]

Baud rate error (theoretical value) =

(1/transfer rate × 2 - {-Cb × Rb × ln (1 - 2.0/Vb)} / (1/transfer rate) × number of transferred bits)

* This value is the theoretical value of the relative difference between the transmission and reception sides.

5. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 4 above to calculate the maximum transfer rate under conditions of the customer.

6. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8V ≤ V_{DD} < 3.3 V and 1.6 V ≤ Vb ≤ 2.0 V

(8) Communication at different potential (2.5 V) (CSI mode) (master mode: SCKp... internal clock output, supporting CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$ 2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	t_{KH1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 120		t_{KCY1}/2 – 120		t_{KCY1}/2 – 120		ns
SCKp low-level width	t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 10		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	121		479		479		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ		130		130		130	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	33		110		110		ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 20 pF, R_b = 2.7 kΩ		10		10		10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]:Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(9) Communication at different potential (1.8 V, 2.5 V) (CSI mode: master mode, SCKp... internal clock output)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) (1/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK} 2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		1150		1150		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		1150		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	–		1150		1150		ns
SCKp high-level width Note 1	t_{KH1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2-170		t_{KCY1}/2-170		t_{KCY1}/2-170		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	t_{KCY1}/2-458		t_{KCY1}/2-458		t_{KCY1}/2-458		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	–		t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		ns
SCKp low-level width Note 1	t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 18		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	–		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
SIp setup time (to SCKp↑) Note 1, 2	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		479		479		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	479		479		479		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	–		479		479		ns
SIp hold time (from SCKp↑) Note 1, 2	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	–		19		19		ns

Notes 1. Supporting CSI00 and CSI20.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

3. Use it with V_{DD} ≥ V_b.

(Caution are listed on the next page.)

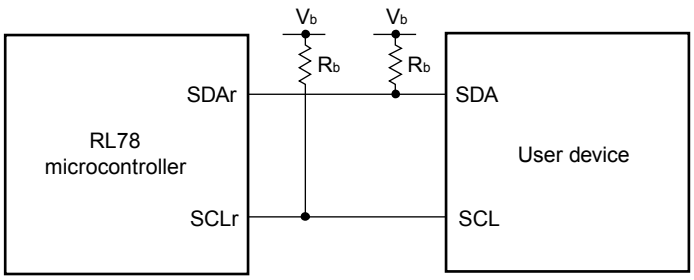
(10) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) (1/2)

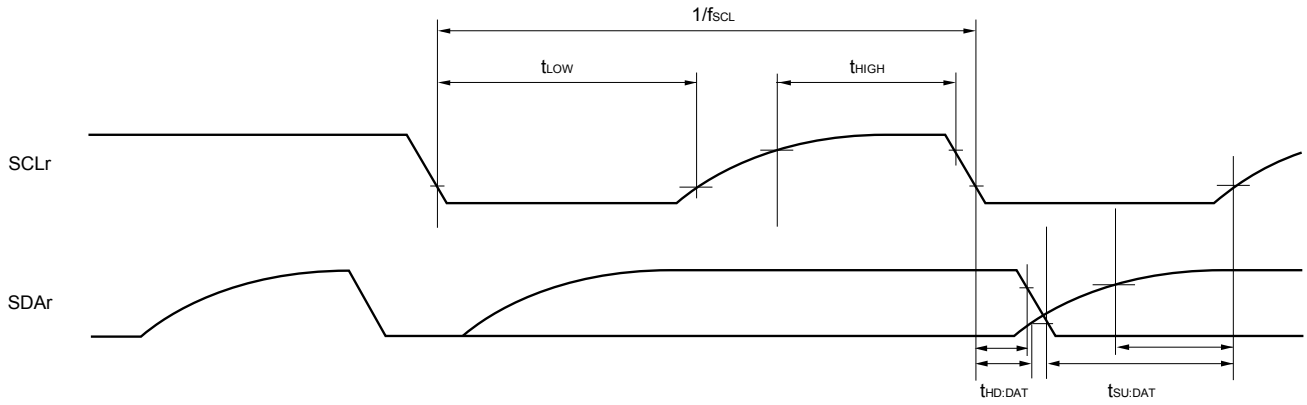
Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	20/ f_{MCK}		–		–		ns
			20 MHz < f_{MCK} ≤ 24 MHz	16/ f_{MCK}		–		–		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/ f_{MCK}		–		–		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/ f_{MCK}		–		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/ f_{MCK}		–		ns
			f_{MCK} ≤ 4MHz	6/f_{MCK}		10/ f_{MCK}		10/ f_{MCK}		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V	24 MHz < f_{MCK}	48/ f_{MCK}		–		–		ns
			20 MHz < f_{MCK} ≤ 24 MHz	36/ f_{MCK}		–		–		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/ f_{MCK}		–		–		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/ f_{MCK}		–		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/ f_{MCK}		16/ f_{MCK}		–		ns
			f_{MCK} ≤ 4MHz	10/ f_{MCK}		10/ f_{MCK}		10/ f_{MCK}		ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2	24 MHz < f_{MCK}	–		–		–		ns
			20 MHz < f_{MCK} ≤ 24 MHz	–		–		–		ns
			16 MHz < f_{MCK} ≤ 20 MHz	–		–		–		ns
			8 MHz < f_{MCK} ≤ 16 MHz	–		–		–		ns
			4 MHz < f_{MCK} ≤ 8 MHz	–		16/ f_{MCK}		–		ns
			f_{MCK} ≤ 4MHz	–		10/ f_{MCK}		10/ f_{MCK}		ns

(**Notes** and **Caution** are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remarks 1. R_b[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 00, 10), g: PIM, POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02))

(2) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AVREFM/ANI1 (ADREFM = 1), conversion target : ANI16 to ANI19

(T_A = –40 to +85°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V		1.2	±5.0	LSB
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4		1.2	±8.5	LSB
Conversion time	T_{cony}	10-bit resolution	2.7 V ≤ V_{DD} ≤ 3.6 V	3.1875		39	µs
			1.8 V ≤ V_{DD} ≤ 3.6 V	17		39	µs
			1.6 V ≤ AV_{REFP} ≤ 3.6 V	57		95	µs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V			±0.35	%FSR
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4			±0.60	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V			±0.35	%FSR
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V			±3.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4			±6.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 3.6 V			±2.0	LSB
			1.6 V ≤ AV_{REFP} ≤ 3.6 V Note 4			±2.5	LSB
Analog input voltage	V_{AIN}			0		AV_{REFP} and V_{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} < V_{DD}, MAX. value is following.

Overall error: ±4 LSB is added to the MAX. value of AV_{REFP} = V_{DD}.

Zero-scale error / Full-scale error: ±0.2 %FSR is added to the MAX. value of AV_{REFP} = V_{DD}.

Integral linearity error / Differential linearity error: ±2 LSB is added to the MAX. value n of AV_{REFP} = V_{DD}.

4. When the the conversion time is set to 57 µs (min.) and 95 µs (max.).

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), conversion target : ANI0 to ANI3, ANI16 to ANI19, Internal reference voltage, Temperature sensor output voltage

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V		1.2	±7.0	LSB
			1.6 V ≤ V_{DD} ≤ 3.6 V Note 3		1.2	±10.5	LSB
Conversion time	T_{conv}	10-bit resolution conversion target : ANI0 to ANI3, ANI16 to ANI19	2.7 V ≤ V_{DD} ≤ 3.6 V	3.1875		39	µs
			1.8 V ≤ V_{DD} ≤ 3.6 V	17		39	µs
			1.6 V ≤ V_{DD} ≤ 3.6 V	57		95	µs
		10-bit resolution conversion target : Internal reference voltage, Temperature sensor output voltage (HS (high-speed main) Mode)	2.7 V ≤ V_{DD} ≤ 3.6 V	3.5635		39	µs
			2.7 V ≤ V_{DD} ≤ 3.6 V	17		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±0.60	%FSR
			1.6 V ≤ V_{DD} ≤ 3.6 V Note 3			±0.85	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±0.60	%FSR
			1.6 V ≤ V_{DD} ≤ 3.6 V Note 3			±0.85	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±4.0	LSB
			1.6 V ≤ V_{DD} ≤ 3.6 V Note 3			±6.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±2.0	LSB
			1.6 V ≤ V_{DD} ≤ 3.6 V Note 3			±2.5	LSB
<R> Analog input voltage	V_{AIN}	ANI0 to ANI3, ANI16 to ANI19		0		V_{DD}	V
		Select internal reference voltage 2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode		V_{BGR} Note 4			V
		Select temperature sensor output voltage 2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode		V_{TMPS25} Note 4			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the the conversion time is set to 57 µs (min.) and 95 µs (max.).

4. Refer to **2.8.2 Temperature sensor and internal reference voltage characteristics**

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), conversion target : ANI0 to ANI3, ANI16 to ANI19

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (–) = AV_{REFM} Note 4 = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	T_{cony}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V	17		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to 2.**8.2 Temperature sensor and internal reference voltage characteristics.**

4. When reference voltage (-) = V_{SS}, MAX. value is following.

Zero-scale error: ±0.35 %FSR is added to the MAX. value of reference voltage (–) = AV_{REFM}.

Integral linearity error: ±0.5 LSB is added to the MAX. value of reference voltage (–) = AV_{REFM}.

Differential linearity error: ±0.2 LSB is added to the MAX. value of reference voltage (–) = AV_{REFM}.

2.9 RF Transceiver Characteristics

2.9.1 RF transmission characteristics

Unless specified otherwise, the measurement is performed by our evaluation board.

(T_A = +25°C, V_{DD} = V_{DD_RF} = AV_{DD_RF} = 3.0 V, f = 2440 MHz, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

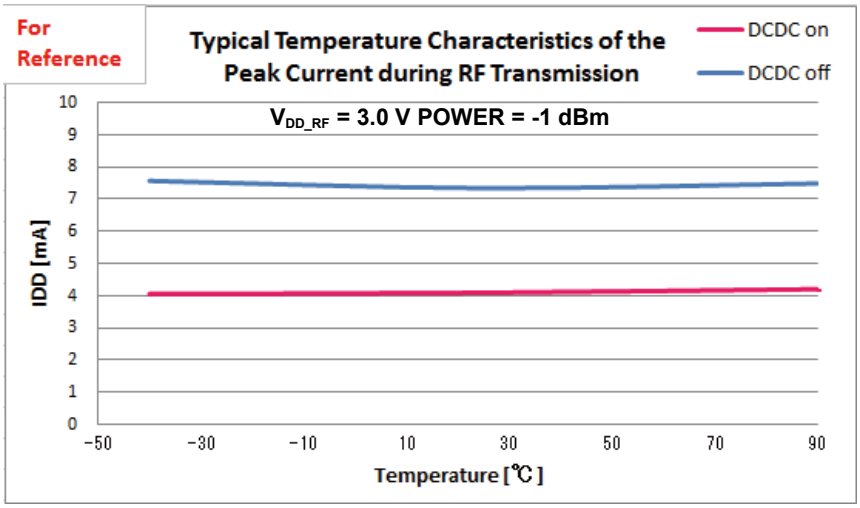
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RF frequency range	RF_{CF}			2402		2480	MHz
Data rate	RF_{DATA}				1		Mbps
Maximum transmitted output power	RF_{POWER}	RF output pin	RF low power mode	-18	-15	-12	dBm
			RF normal mode	-3	0	3	dBm
			RF high performance mode	-3	0	3	dBm
Transmitted output power setting	RF_{TXPOW}	0, -1, -2, -7, -10, -15 dBm		-15		0	dBm
Spurious radiation	RF_{TXSP}	30 to 88 MHz			-76	-55	dBm
		88 to 216 MHz			-76	-52	dBm
		216 to 960 MHz			-74	-49	dBm
		960 to 1000 MHz			-74	-30	dBm
		1 to 12.75 GHz			-42	-41	dBm
		1.8 to 1.9 GHz			-73	-47	dBm
		5.15 to 5.3 GHz			-71	-47	dBm
Harmonics	RF_{TXHC1}	2^{nd} Harmonics			-52	-41	dBm
	RF_{TXHC2}	3^{rd} Harmonics			-51	-41	dBm
Frequency tolerance	RF_{TXFERR}			-30		+30	ppm
Impedance	RF_{Z1}				50+j0		Ω

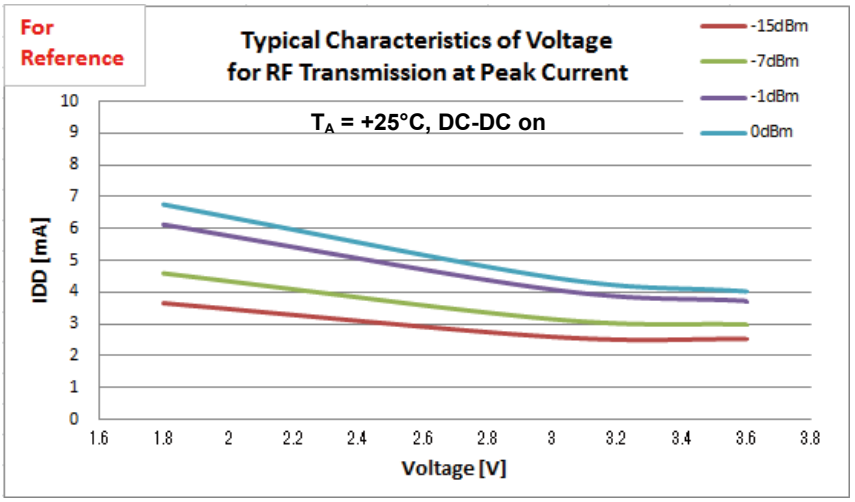
Caution Install EMI countermeasures as required to prevent EMI effects of the RF transmission characteristics.

2.9.3 Performance mapping for typical RF (Reference)

(1) Peak Current during RF Transmission

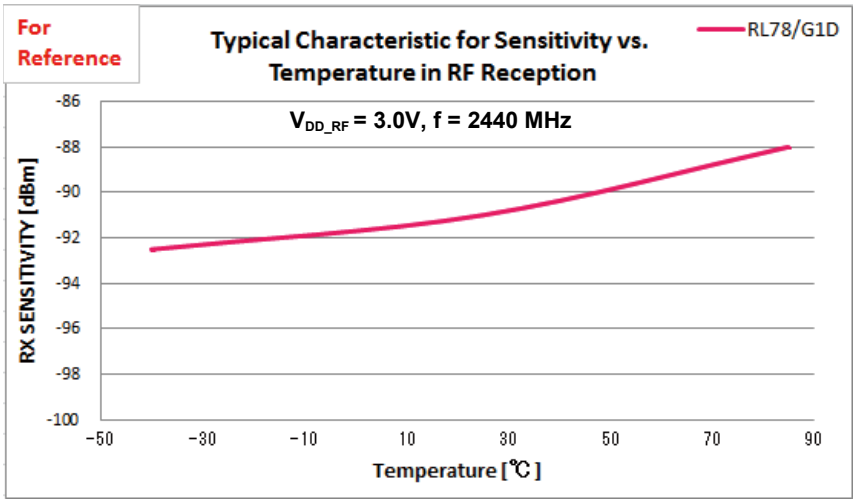
Unless specified otherwise, the measurement is performed by our evaluation board.
Current consumption is not including MCU unit.

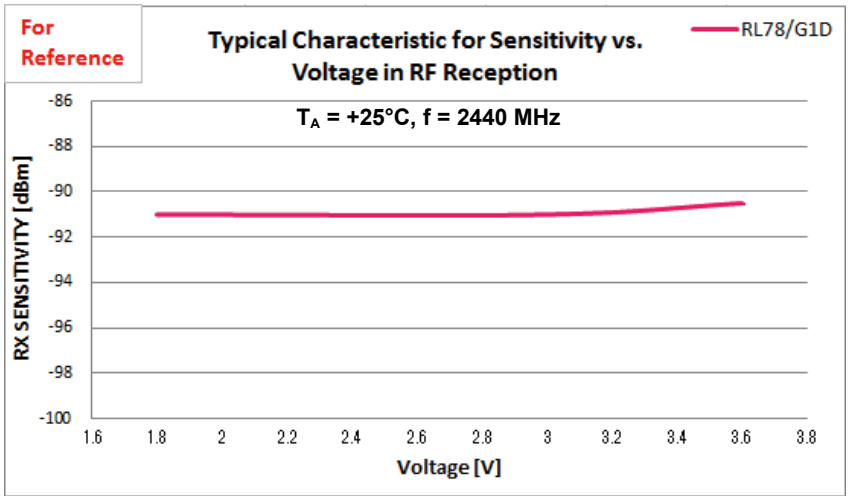




(4) RF Reception Sensitivity

Unless specified otherwise, the measurement is performed by our evaluation board.
Current consumption is not including MCU unit.

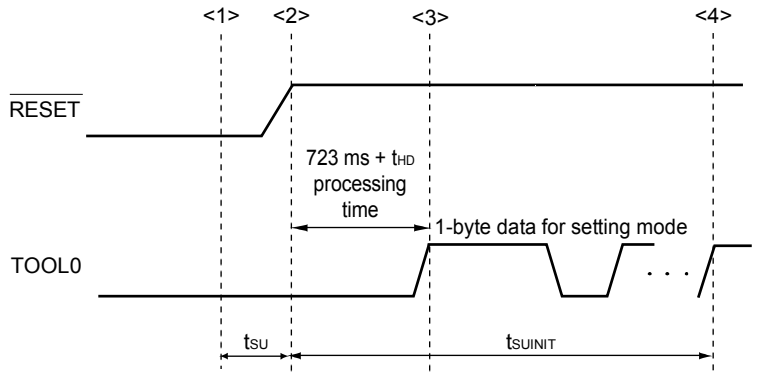




2.13 Timing of Entry to Flash Memory Programming Modes

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.		100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10		μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1		ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.
t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level
t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

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