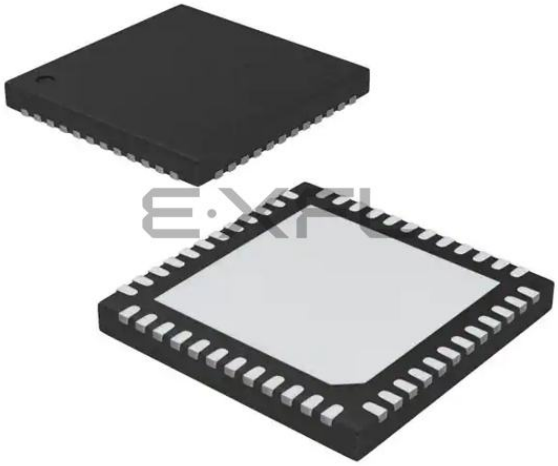


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-WFQFN Exposed Pad |
| Supplier Device Package | 48-HWQFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11agjanb-40 |

## 1.2 List of Part Numbers

**Figure 1-1. Part Number, Memory Size, and Package of RL78/G1D**

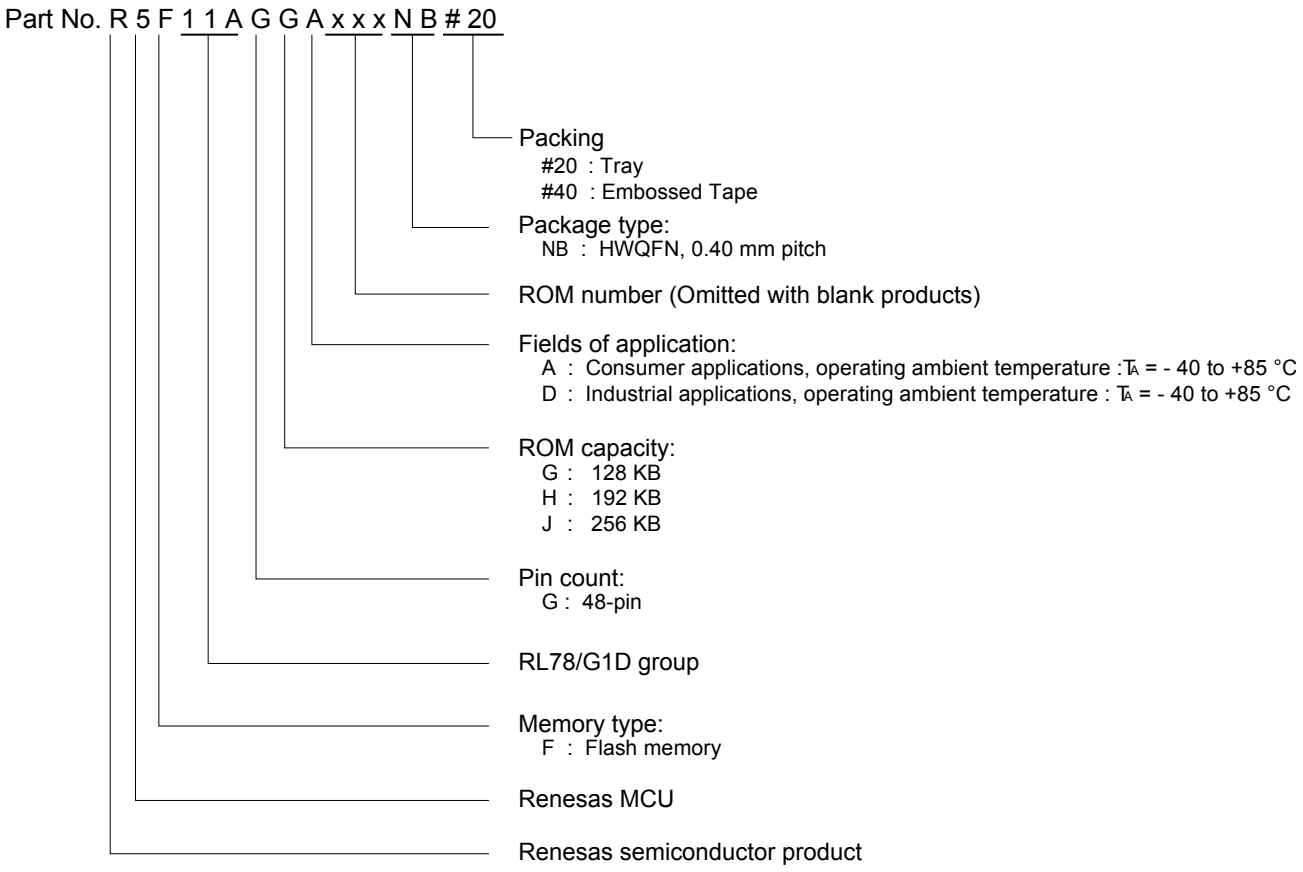



**Table 1-1. List of Ordering Part Numbers**

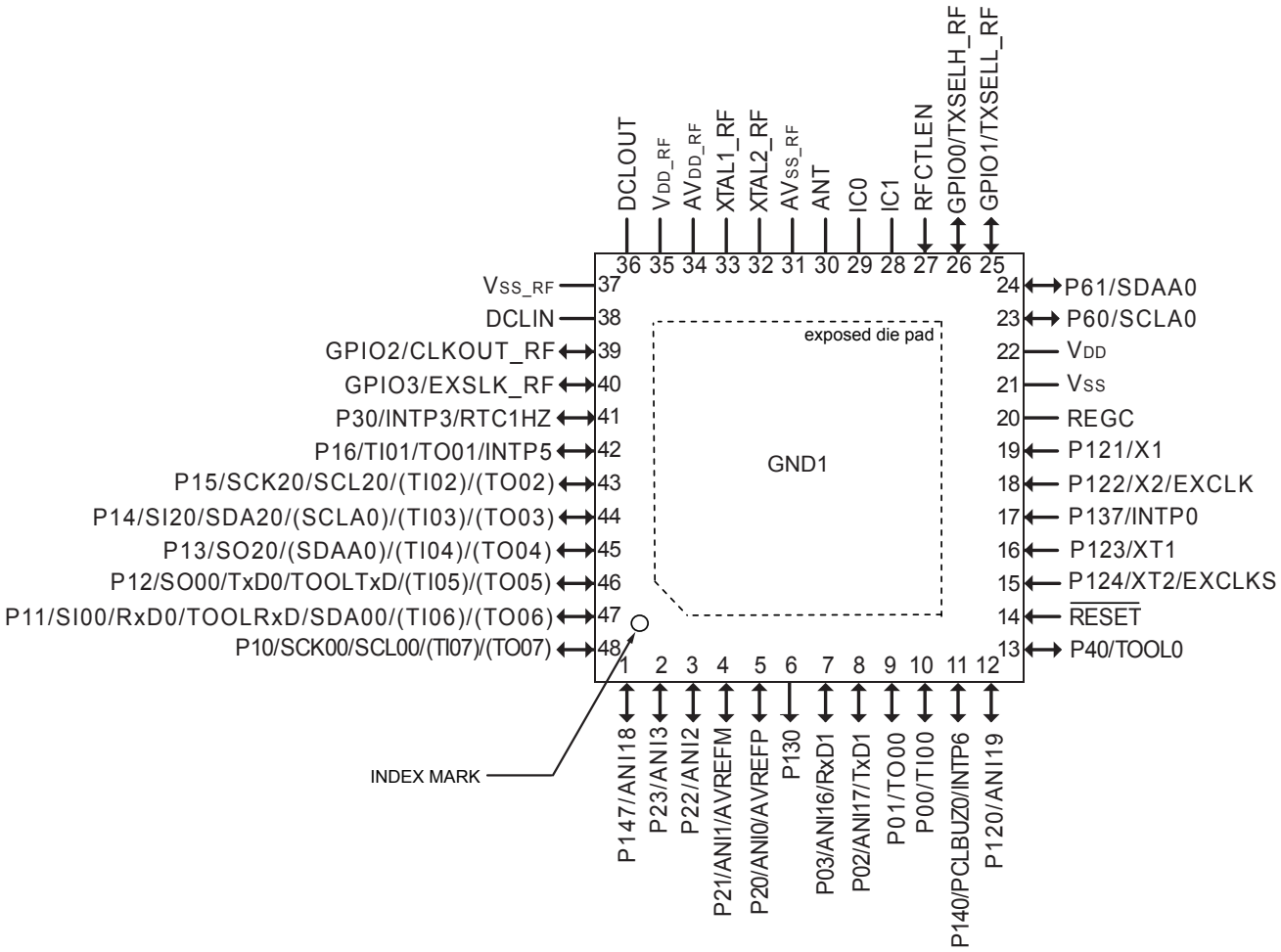
| Pin count | Package | Fields of Application[Note] | Ordering Part Number | Code Flash Memory | Data Flash Memory |
|---|---|---|---|---|---|
| 48 pins | Plastic WQFN (6 × 6) | A | R5F11AGGANB#20<br>R5F11AGGANB#40 | 128 KB | 8 KB |
| | | D | R5F11AGGDNB#20<br>R5F11AGGDNB#40 | | |
| | | A | R5F11AGHANB#20<br>R5F11AGHANB#40 | 192 KB | 8 KB |
| | | D | R5F11AGHDNB#20<br>R5F11AGHDNB#40 | | |
| | | A | R5F11AGJANB#20<br>R5F11AGJANB#40 | 256 KB | 8 KB |
| | | D | R5F11AGJDNB#20<br>R5F11AGJDNB#40 | | |

**Note** For the fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/G1D**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

## 1.3 Pin Configuration (Top View)

<R> ● 48-pin plastic WQFN (6 × 6 mm, 0.4 mm pitch)



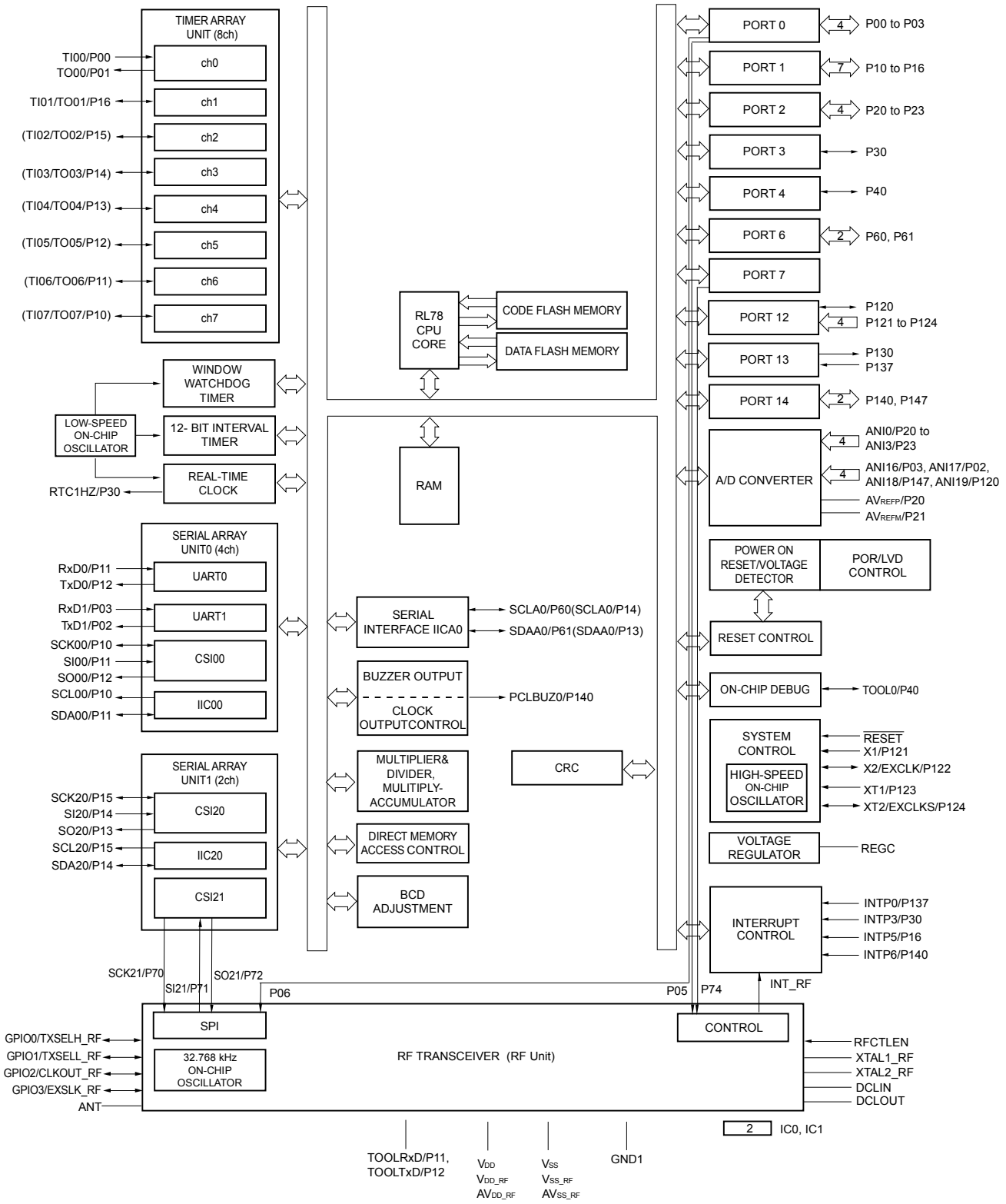

**Cautions 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).**

**2. Connect the metal pad (GND1) on the back of the package that has the same potential as $AV_{SS\_RF}$.**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)..

## 1.5 Block Diagram




**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

**Notes 1.** This is about 19 KB when the self-programming function is used.

**2.** When RF is used, this count includes the pins that connect the MCU with the RF transceiver by the user externally on the board.

# 2. ELECTRICAL SPECIFICATIONS

**Caution The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**Absolute Maximum Ratings ($T_A$ = 25°C) (2/2)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Output current, high | $I_{OH1}$ | Per pin | (This is applicable to all pins listed below.) | –40 | mA |
| | | Total of all pins –170mA | P00, P01, P02, P03, P40, P120, P130, P140 | –70 | mA |
| | | | P10, P11, P12, P13, P14, P15, P16, P30, P147 | –100 | mA |
| | $I_{OH2}$ | Per pin | (This is applicable to all pins listed below.) | –0.5 | mA |
| | | Total of all pins | P20, P21, P22, P23 | –2 | mA |
| | $I_{OHMRF}$ | Per pin | GPIO0, GPIO1, GPIO2, GPIO3 | –17 | mA |
| Output current, low | $I_{OL1}$ | Per pin | (This is applicable to all pins listed below.) | 40 | mA |
| | | Total of all pins 170mA | P00, P01, P02, P03, P40, P120, P130, P140 | 70 | mA |
| | | | P10, P11, P12, P13, P14, P15, P16, P30, P60, P61, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | (This is applicable to all pins listed below.) | 1 | mA |
| | | Total of all pins | P20, P21, P22, P23 | 5 | mA |
| | $I_{OLRF}$ | Per pin | GPIO0, GPIO1, GPIO2, GPIO3 | 17 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | –40 to +85 | °C |
| | | In flash memory programming mode | | –40 to +85 | °C |
| Storage temperature | Tstg | | | –65 to +150 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.** $AV_{REF(+)}$ : + side reference voltage of the A/D converter.

**3.** Reference voltage is $V_{SS}$.

### 2.4.4 Input leakage current

**($T_A$ = –40 to +85°C, 1.6 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | VI = $V_{DD}$ | P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P60, P61, P120, P140, P147 | | | 1 | μA |
| | $I_{LIH2}$ | VI = $V_{DD}$ | P20, P21, P22, P23, P137, $\overline{\text{RESET}}$ | | | 1 | μA |
| | $I_{LIH3}$ | VI = $V_{DD}$ | P121, P122, P123, P124 (EXCLK, EXCLKS) (XT1, XT2) In input port | | | 1 | μA |
| | | | In external clock input | | | 1 | μA |
| | | | In resonator connection | | | 10 | μA |
| | $I_{LIHRF}$ | VI = $V_{DD\_RF}$ | GPIO0, GPIO1, GPIO2, GPIO3 | | | 10 | μA |
| Input leakage current, low | $I_{LIL1}$ | VI = $V_{SS}$ | P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P60, P61, P120, P140, P147 | | | -1 | μA |
| | $I_{LIL2}$ | VI = $V_{SS}$ | P20, P21, P22, P23, P137, $\overline{\text{RESET}}$ | | | -1 | μA |
| | $I_{LIL3}$ | VI = $V_{SS}$ | P121, P122, P123, P124 (EXCLK, EXCLKS) (XT1, XT2) In input port | | | -1 | μA |
| | | | In external clock input | | | -1 | μA |
| | | | In resonator connection | | | -10 | μA |
| | $I_{LILRF}$ | VI = $V_{SS\_RF}$ | GPIO0, GPIO1, GPIO2, GPIO3 | | | -10 | μA |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

### 2.4.5 Resistance

**($T_A$ = –40 to +85°C, 1.6 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| On-chip pll-up resistance | $R_U$ | VI = $V_{SS}$ | P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P140, P147 In input mode | 10 | 20 | 100 | kΩ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Notes 1.** Current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**4.** When high-speed system clock and subsystem clock are stopped.

**5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 3.6 V@1 MHz to 4 MHz

**8.** If operation of the subsystem clock when STOP mode, same as when HALT mode of subsystem clock operation.

**9.** The upper value is for square-wave input and the lower is with an oscillator connected.

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (External main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

### (3) Current for each peripheral circuit

**($T_A$ = –40 to +85°C, 1.6 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed on-chip oscillator operating current | $I_{FIL}$ Note 1 | | | | 0.20 | | μA |
| Current when PCLBUZ0 and EXSLK_RF are connected together and MCU supplies RF slow clock to RF | $I_{PCEX}$ Note 1 | | | | 1.0 | | μA |
| RTC operating current | $I_{RTC}$ Notes 1, 2, 3 | | | | 0.02 | | μA |
| 12-bit interval timer operating current | $I_{IT}$ Notes 1, 2, 4 | | | | 0.02 | | μA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 5 | $f_{IL}$ is 15 kHz | | | 0.22 | | μA |
| A/D converter operating current | $I_{ADC}$ Notes 1, 6 | When conversion at maximum speed | $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 0.5 | 0.7 | mA |
| A/D converter reference voltage current | $I_{ADREF}$ Note 1 | | | | 75.0 | | μA |
| Thermometer sensor operating current | $I_{TMPS}$ Note 1 | | | | 75.0 | | μA |
| LVD operating current | $I_{LVI}$ Note 1, 7 | | | | 0.08 | | μA |
| Flash self-programming operating current | $I_{FSP}$ Notes 1, 9 | | | | 2.50 | 12.20 | mA |
| BGO current | $I_{BGO}$ Notes 1, 8 | | | | 2.50 | 12.20 | mA |
| SNOOZE operating current | $I_{SNOZ}$ Note 1 | ADC operation | The mode is performed Note 10 | | 0.50 | 0.60 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 1.20 | 1.44 | mA |
| | | CSI/UART operation | | | 0.70 | 0.84 | mA |

**Notes 1.** Current flowing to $V_{DD}$.

**2.** When high speed on-chip oscillator and high-speed system clock are stopped.

**3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the XT1 oscillator). The value of the current value of the RL78 microcontroller is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{RTC}$, when the real-time clock operates in operation mode or HALT mode. Also, add the value of IFIL in case of selecting low-speed on-chip oscillator. $I_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.

**4.** Current flowing only to the 12 bit interval timer (including the operating current of the low-speed on-chip oscillator). The current value of the MCU is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{IT}$ when $f_{CLK}$ = $f_{SUB}$ when the watchdog timer operates in STOP mode. When using low-speed on-chip oscillator, add $I_{FIL}$.

**5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the MCU is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer is in operation.

**6.** Current flowing only to the A/D converter. The current value of MCU is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

**7.** Current flowing only to the LVD circuit. The current value of MCU is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVI}$ when the LVD circuit is in operation.

**8.** Current flowing when operates rewriting to Data flash.

**9.** Current flowing when operates flash self-programming.

**10.** Shift time to the SNOOZE mode is referred User's Manual: Hardware.

(**Remarks** are listed on the next page.)

**(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, supporting CSI00 only)**

**($T_A$ = –40 to +85°C, 2.7 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 2/f_{CLK}$ | 83.3 | | 250 | | 500 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | | $t_{KCY1}/2 - 10$ | | $t_{KCY1}/2 - 50$ | | $t_{KCY1}/2 - 50$ | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | | 33 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↓ to SOp output Note 2 | $t_{KSO1}$ | C = 20 pF Note 3 | | 10 | | 10 | | 10 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** C is the load capacitance of the SCKp and SOp output lines.

**Cautions Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remarks 1.** This specification is valid only when CSI00's peripheral I/O redirect function is not used.

**2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

### (3) During communication at same potential (CSI mode) (Internal communication, supporting CSI21 only)

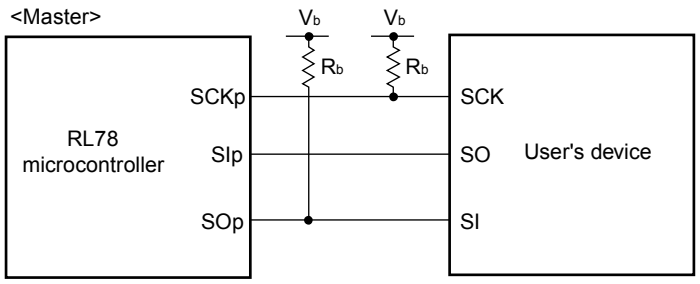
**($T_A$ = –40 to +85°C, 1.6 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ $2/f_{CLK}$ Note | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | 250 | | 250 | | 500 | | ns |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | – | | 250 | | 500 | | ns |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | – | | – | | 500 | | ns |

**Note** Use the $f_{CLK}$ more than 6.5 MHz and lower than 24 MHz.

**Remark** This specification is for CSI21 only.

**CSI mode connection diagram (during communication at different potential)**

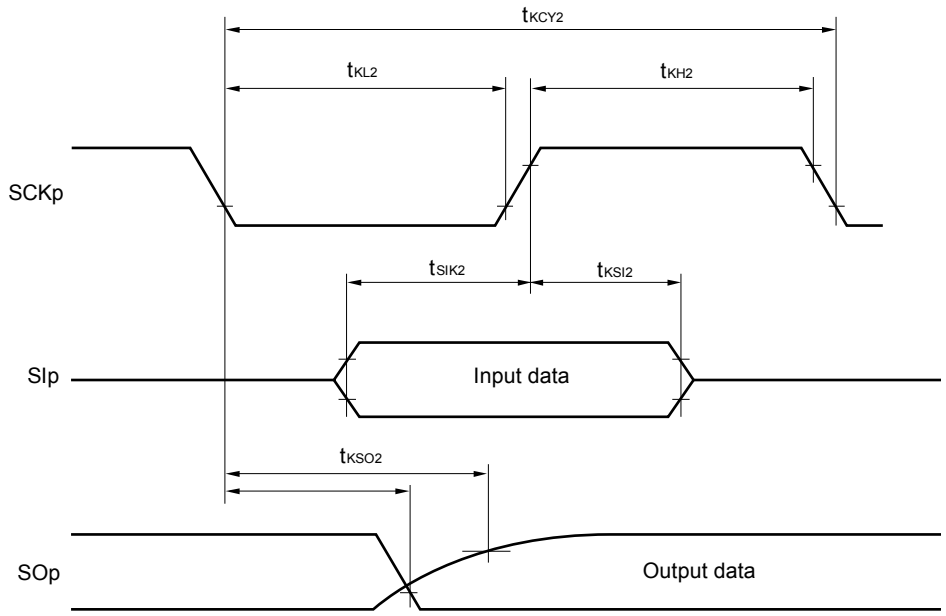



**Remarks 1.** $R_b$[Ω]:Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

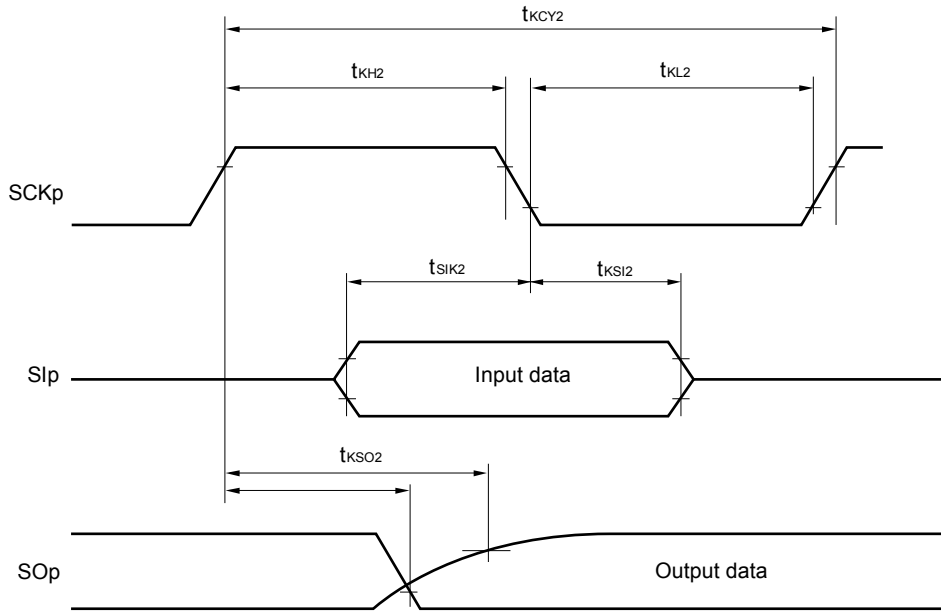
**2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

**3.** $f_{MCK}$ : Operation clock frequency of the serial array unit
(Operation clock to be set by the CKSmn bit of the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



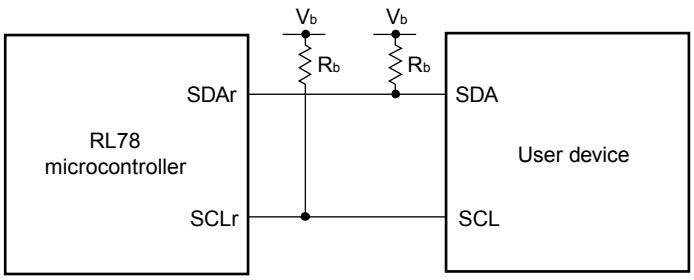

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



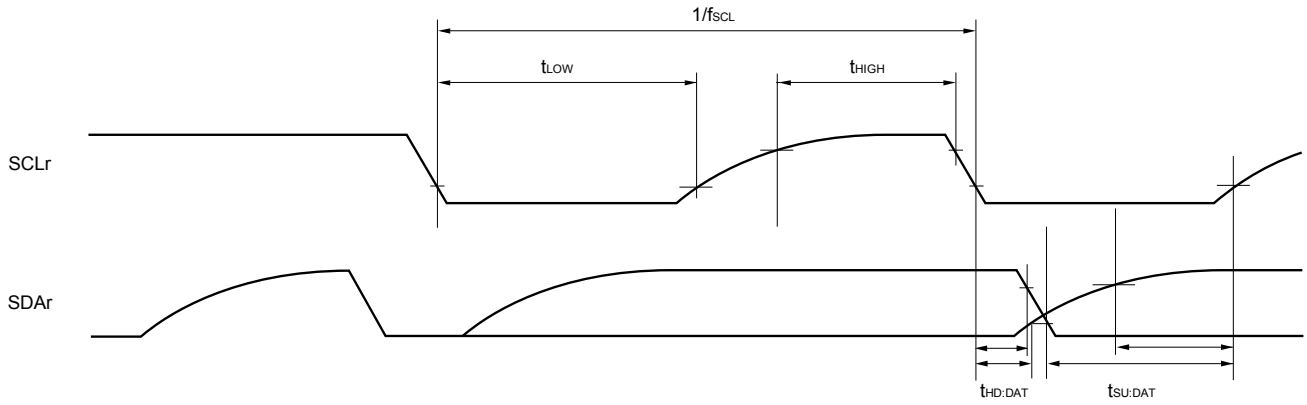

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

**Simplified I²C mode connection diagram (during communication at different potential)**




**Simplified I²C mode serial transfer timing (during communication at different potential)**




**Remarks 1.** $R_b$[Ω]:Communication line (SDAr, SCLr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance, $V_b$[V]: Communication line voltage

**2.** r: IIC number (r = 00, 10), g: PIM, POM number (g = 0, 1)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02))

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

**Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.
Standard mode: $C_b$ = 400 pF, $R_b$ = 2.7 kΩ

### 2.8.2 Temperature sensor and internal reference voltage characteristics

**($T_A$ = –40 to +85°C, 2.4 V ≤ $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ ≤ 3.6 V, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V, HS (high-speed main) mode)**

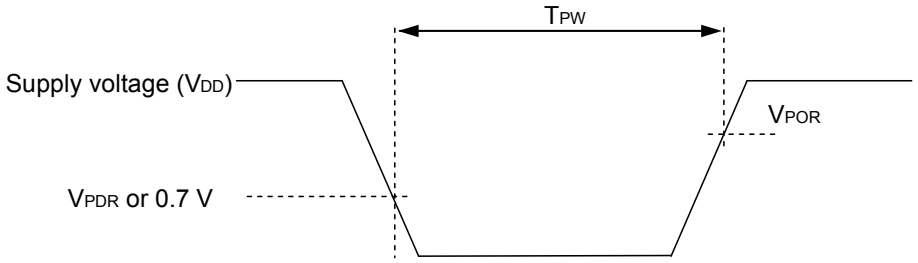
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor output voltage that depends on the temperature | | –3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

### 2.8.3 POR circuit characteristics

**($T_A$ = –40 to +85°C, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{POR}$ | Rise time | 1.47 | 1.51 | 1.55 | V |
| | $V_{PDR}$ | Fall time | 1.46 | 1.50 | 1.54 | V |
| Minimum pulse width[Note] | $T_{PW}$ | Other than STOP/SUB_RUN/SUB_HALT | 300 | | | μs |

**Note** This is the time required for the POR circuit to execute a reset operation when $V_{DD}$ falls below $V_{PDR}$. When the main system clock ($f_{MAIN}$) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC) or when the microcontroller enters STOP mode, this is the time required for the POR circuit to execute a reset operation between when $V_{DD}$ falls below 0.7 V and when $V_{DD}$ rises to $V_{POR}$ or higher.



### 2.8.4 LVD circuit characteristics

**LVD Detection Voltage of Reset Mode and Interrupt Mode**
**($T_A$ = –40 to +85°C, $V_{PDR} \leq V_{DD} = V_{DD\_RF} = AV_{DD\_RF} \leq 3.6$ V, $V_{SS} = V_{SS\_RF} = AV_{SS\_RF}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Detection voltage | Supply voltage | $V_{LVI2}$ | Power supply rise time | 3.07 | 3.13 | 3.19 | V |
| | | | Power supply fall time | 3 | 3.06 | 3.12 | V |
| | | $V_{LVI3}$ | Power supply rise time | 2.96 | 3.02 | 3.08 | V |
| | | | Power supply fall time | 2.9 | 2.96 | 3.02 | V |
| | | $V_{LVI4}$ | Power supply rise time | 2.86 | 2.92 | 2.97 | V |
| | | | Power supply fall time | 2.8 | 2.86 | 2.91 | V |
| | | $V_{LVI5}$ | Power supply rise time | 2.76 | 2.81 | 2.87 | V |
| | | | Power supply fall time | 2.7 | 2.75 | 2.81 | V |
| | | $V_{LVI6}$ | Power supply rise time | 2.66 | 2.71 | 2.76 | V |
| | | | Power supply fall time | 2.6 | 2.65 | 2.7 | V |
| | | $V_{LVI7}$ | Power supply rise time | 2.56 | 2.61 | 2.66 | V |
| | | | Power supply fall time | 2.5 | 2.55 | 2.6 | V |
| | | $V_{LVI8}$ | Power supply rise time | 2.45 | 2.5 | 2.55 | V |
| | | | Power supply fall time | 2.4 | 2.45 | 2.5 | V |
| | | $V_{LVI9}$ | Power supply rise time | 2.05 | 2.09 | 2.13 | V |
| | | | Power supply fall time | 2 | 2.04 | 2.08 | V |
| | | $V_{LVI10}$ | Power supply rise time | 1.94 | 1.98 | 2.02 | V |
| | | | Power supply fall time | 1.9 | 1.94 | 1.98 | V |
| | | $V_{LVI11}$ | Power supply rise time | 1.84 | 1.88 | 1.91 | V |
| | | | Power supply fall time | 1.8 | 1.84 | 1.87 | V |
| | | $V_{LVI12}$ | Power supply rise time | 1.74 | 1.77 | 1.81 | V |
| | | | Power supply fall time | 1.7 | 1.73 | 1.77 | V |
| | | $V_{LVI13}$ | Power supply rise time | 1.64 | 1.67 | 1.7 | V |
| | | | Power supply fall time | 1.6 | 1.63 | 1.66 | V |
| Minimum pulse width | | $T_{LW}$ | | 300 | | | μs |
| Detection delay time | | | | | | 300 | μs |

## 2.9 RF Transceiver Characteristics

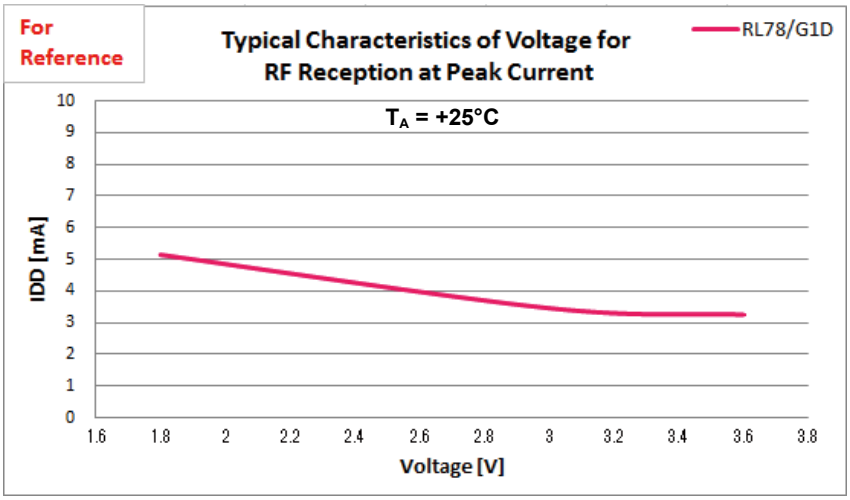
### 2.9.1 RF transmission characteristics

Unless specified otherwise, the measurement is performed by our evaluation board.

**($T_A$ = +25°C, $V_{DD}$ = $V_{DD\_RF}$ = $AV_{DD\_RF}$ = 3.0 V, f = 2440 MHz, $V_{SS}$ = $V_{SS\_RF}$ = $AV_{SS\_RF}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| RF frequency range | $RF_{CF}$ | | | 2402 | | 2480 | MHz |
| Data rate | $RF_{DATA}$ | | | | 1 | | Mbps |
| Maximum transmitted output power | $RF_{POWER}$ | RF output pin | RF low power mode | -18 | -15 | -12 | dBm |
| | | | RF normal mode | -3 | 0 | 3 | dBm |
| | | | RF high performance mode | -3 | 0 | 3 | dBm |
| Transmitted output power setting | $RF_{TXPOW}$ | 0, -1, -2, -7, -10, -15 dBm | | -15 | | 0 | dBm |
| Spurious radiation | $RF_{TXSP}$ | 30 to 88 MHz | | | -76 | -55 | dBm |
| | | 88 to 216 MHz | | | -76 | -52 | dBm |
| | | 216 to 960 MHz | | | -74 | -49 | dBm |
| | | 960 to 1000 MHz | | | -74 | -30 | dBm |
| | | 1 to 12.75 GHz | | | -42 | -41 | dBm |
| | | 1.8 to 1.9 GHz | | | -73 | -47 | dBm |
| | | 5.15 to 5.3 GHz | | | -71 | -47 | dBm |
| Harmonics | $RF_{TXHC1}$ | $2^{nd}$ Harmonics | | | -52 | -41 | dBm |
| | $RF_{TXHC2}$ | $3^{rd}$ Harmonics | | | -51 | -41 | dBm |
| Frequency tolerance | $RF_{TXFERR}$ | | | -30 | | +30 | ppm |
| Impedance | $RF_{Z1}$ | | | | 50+j0 | | Ω |

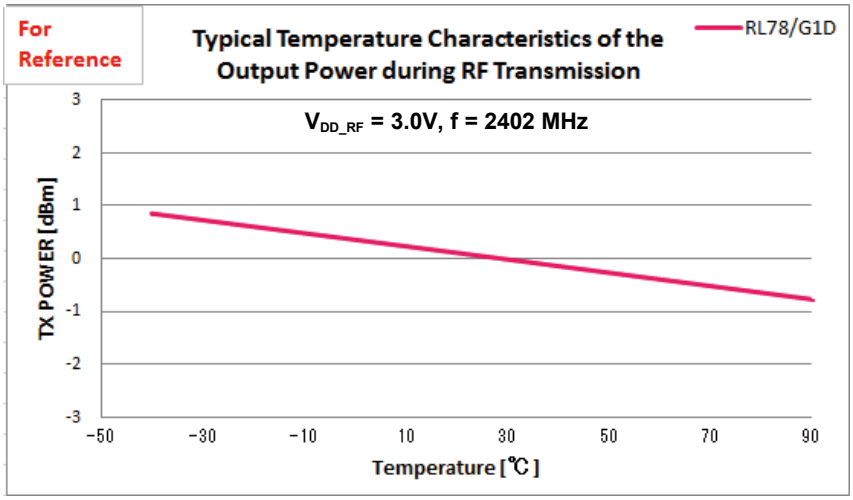
**Caution Install EMI countermeasures as required to prevent EMI effects of the RF transmission characteristics.**




**(3) RF Output Power during Transmission**

Unless specified otherwise, the measurement is performed by our evaluation board.

Current consumption is not including MCU unit.

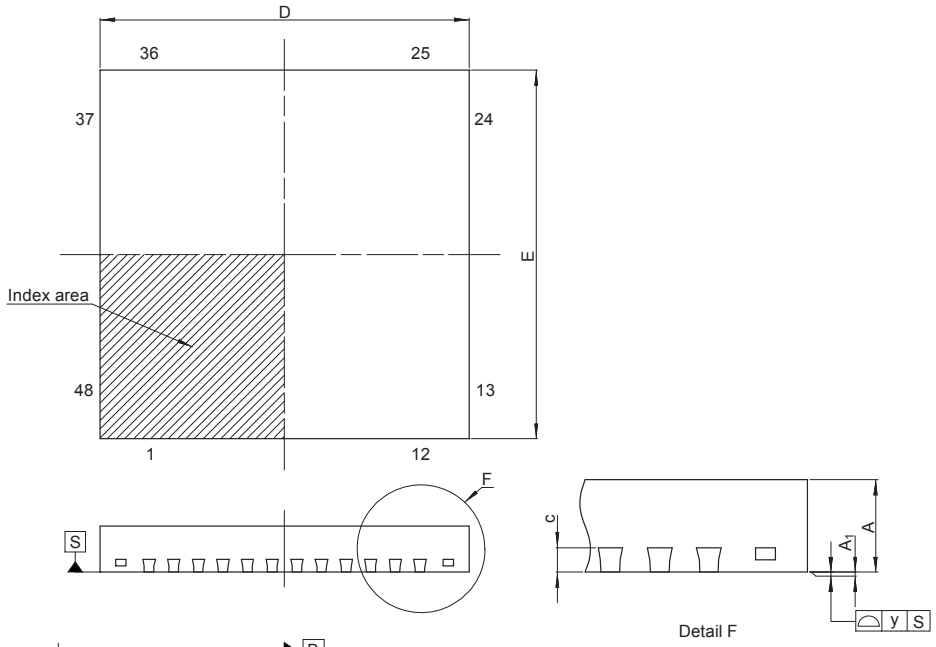


# 3. PACKAGE DRAWINGS

## 3.1 48-pin plastic WQFN (6 × 6)

| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-HWQFN48-6x6-0.40 | PWQN0048LB-A | - | 0.07 |

Unit: mm




| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 5.90 | 6.00 | 6.10 |
| E | 5.90 | 6.00 | 6.10 |
| A | - | - | 0.80 |
| $A_1$ | 0.00 | - | - |
| b | 0.15 | 0.20 | 0.25 |
| e | - | 0.40 | - |
| $L_P$ | 0.20 | 0.30 | 0.40 |
| x | - | - | 0.05 |
| y | - | - | 0.05 |
| $Z_D$ | - | 0.80 | - |
| $Z_E$ | - | 0.80 | - |
| c | - | 0.20 | - |
| $D_2$ | - | 4.73 | - |
| $E_2$ | - | 4.73 | - |