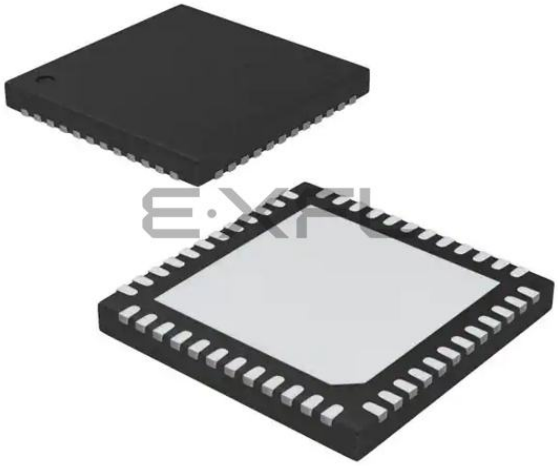
Renesas Electronics America Inc - R5F11AGJDNB#40 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	32
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11agjdnb-40

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G1D

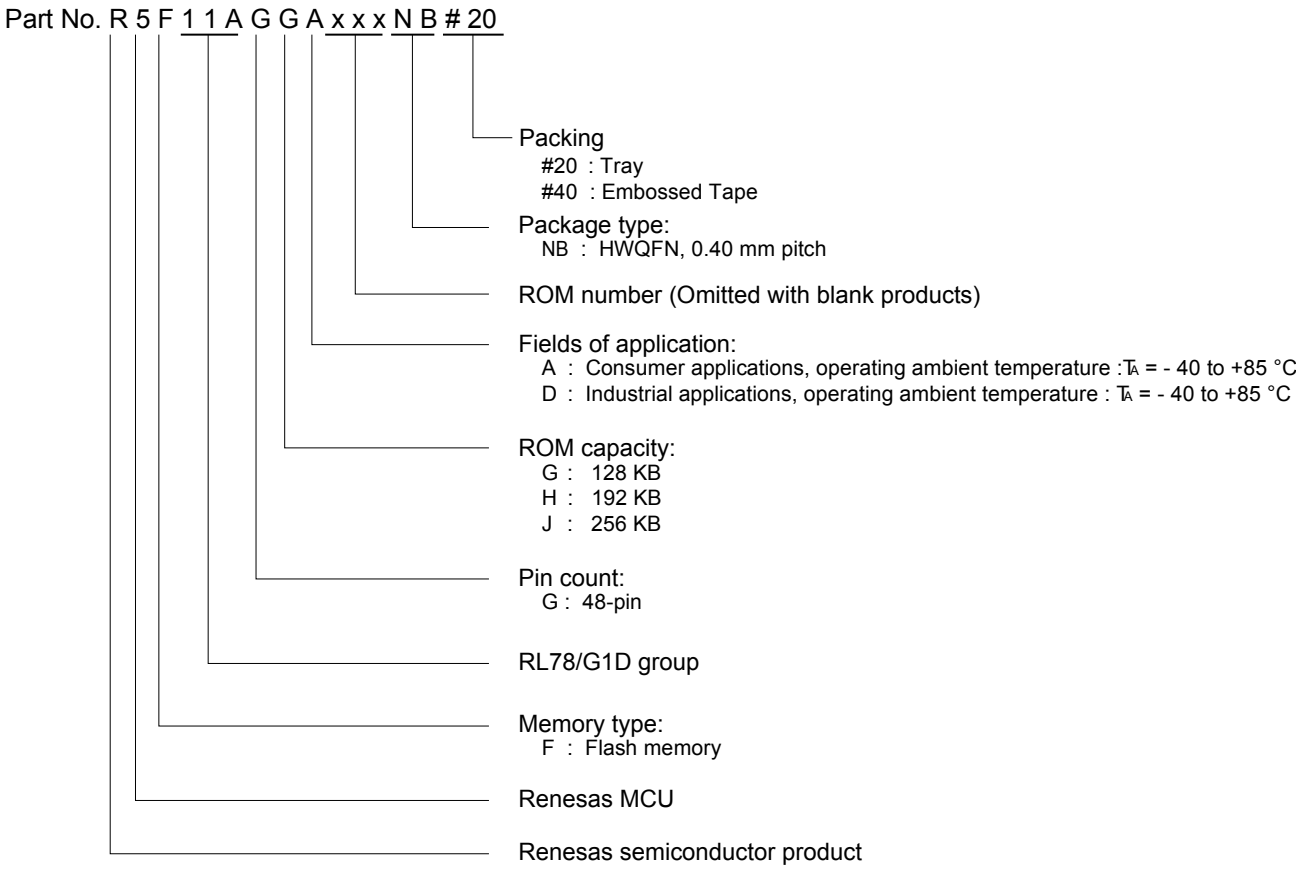


Table 1-1. List of Ordering Part Numbers

Pin count	Package	Fields of Application[Note]	Ordering Part Number	Code Flash Memory	Data Flash Memory
48 pins	Plastic WQFN (6 × 6)	A	R5F11AGGANB#20 R5F11AGGANB#40	128 KB	8 KB
		D	R5F11AGGDNB#20 R5F11AGGDNB#40		
		A	R5F11AGHANB#20 R5F11AGHANB#40	192 KB	8 KB
		D	R5F11AGHDNB#20 R5F11AGHDNB#40		
		A	R5F11AGJANB#20 R5F11AGJANB#40	256 KB	8 KB
		D	R5F11AGJDNB#20 R5F11AGJDNB#40		

Note For the fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/G1D**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.6 Outline of Functions

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		R5F11AGG	R5F11AGH	R5F11AGJ
Code flash memory		128 KB	192 KB	256 KB
Data flash memory		8 KB	8 KB	8 KB
RAM		12 KB	16 KB	20 KB[Note 1]
Address space		1 MB		
System clock (RF side)		32 MHz		
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 3.6 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 3.6 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 3.6 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 3.6 V)		
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 3.6 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 3.6 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 3.6 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 3.6 V)		
Subsystem clock		XT1 (Crystal) oscillation, External main system clock input (EXCLKS) 32.768 kHz		
RF slow clock	External input	External clock input for RF block (EXSLK_RF) 32.768 kHz (TYP.)		
	On-chip Oscillator	32.768 kHz (TYP.)		
Low-speed on-chip oscillator		15 kHz (TYP.)		
General-purpose register		(8-bit register × 8) × 4 banks		
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillation clock: f_{IH} = 32 MHz operation)		
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)		
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)		
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.		
I/O port	Total	32[Note 2]		
	CMOS I/O	20[Note 2]		
	CMOS input	5[Note 2]		
	CMOS output	1[Note 2]		
	N-ch O.D. I/O (withstand voltage: 6 V)	2		
	GPIO (RF block)	4		
2.4 GHz RF transceiver		Supporting Bluetooth v4.1 Specification (Single mode). 2.4 GHz ISM Band, GFSK modulation, TDMA/TDD frequency hopping (Including AES encryption circuit.) Adaptivity (Only in slave operation)		
Timer	16-bit timer	8 channels		
	Watchdog timer	1 channel		
	Real-time clock (RTC)	1 channel		
	12-bit interval timer	1 channel		

(Notes are listed on the next page.)

2.4.3 Output voltage

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	I_{OH} = –2.0 mA	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P140, P147	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} – 0.6			V
		I_{OH} = –1.5 mA		1.8 V ≤ V_{DD} ≤ 3.6 V	V_{DD} – 0.5			V
		I_{OH} = –1.0 mA		1.6 V ≤ V_{DD} ≤ 3.6 V	V_{DD} – 0.5			V
		I_{OH} = –10 μA	P130		V_{DD} – 0.3			V
	V_{OH2}	I_{OH} = –100 μA	P20, P21, P22, P23		V_{DD} – 0.5			V
	V_{OHRF}	I_{OH} = –2.0 mA	GPIO0, GPIO1, GPIO2, GPIO3	2.7 V ≤ V_{DD_RF} ≤ 3.6 V	V_{DD_RF} – 0.3			V
		I_{OH} = –1.5 mA		1.8 V ≤ V_{DD_RF} ≤ 3.6 V	V_{DD_RF} – 0.3			V
Output voltage, low	V_{OL1}	I_{OL} = 3.0 mA	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P130, P140, P147	2.7 V ≤ V_{DD} ≤ 3.6 V			0.6	V
		I_{OL} = 1.5 mA					0.4	V
		I_{OL} = 0.6 mA		1.8 V ≤ V_{DD} ≤ 3.6 V			0.4	V
		I_{OL} = 0.3 mA		1.6 V ≤ V_{DD} ≤ 3.6 V			0.4	V
	V_{OL2}	I_{OL} = 400 μA	P20, P21, P22, P23				0.4	V
	V_{OLRF}		GPIO0, GPIO1, GPIO2, GPIO3				0.3	V

Caution P00, P02, P03, and P10 to P15 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.4.4 Input leakage current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	VI = V_{DD}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P60, P61, P120, P140, P147			1	μA
	I_{LIH2}	VI = V_{DD}	P20, P21, P22, P23, P137, $\overline{\text{RESET}}$			1	μA
	I_{LIH3}	VI = V_{DD}	P121, P122, P123, P124 (EXCLK, EXCLKS) (XT1, XT2) In input port			1	μA
			In external clock input			1	μA
			In resonator connection			10	μA
	I_{LIHRF}	VI = V_{DD_RF}	GPIO0, GPIO1, GPIO2, GPIO3			10	μA
Input leakage current, low	I_{LIL1}	VI = V_{SS}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P60, P61, P120, P140, P147			-1	μA
	I_{LIL2}	VI = V_{SS}	P20, P21, P22, P23, P137, $\overline{\text{RESET}}$			-1	μA
	I_{LIL3}	VI = V_{SS}	P121, P122, P123, P124 (EXCLK, EXCLKS) (XT1, XT2) In input port			-1	μA
			In external clock input			-1	μA
			In resonator connection			-10	μA
	I_{LILRF}	VI = V_{SS_RF}	GPIO0, GPIO1, GPIO2, GPIO3			-10	μA

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.4.5 Resistance

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
On-chip pll-up resistance	R_U	VI = V_{SS}	P00, P01, P02, P03, P10, P11, P12, P13, P14, P15, P16, P30, P40, P120, P140, P147 In input mode	10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.5 Current Consumption

The Current Consumption by the RL78/G1D is the total current including that for the MCU (current flowing into the V_{DD} pin) and that for the RF unit (current flowing into the V_{DD_RF}, AV_{DD_RF} pins).

The characteristics of the MCU (current flowing into the V_{DD} pin) are given in 2.5.1 and the characteristics of the RF unit (current flowing into the V_{DD_RF}/AV_{DD_RF} pins) are given in 2.5.2

2.5.1 MCU

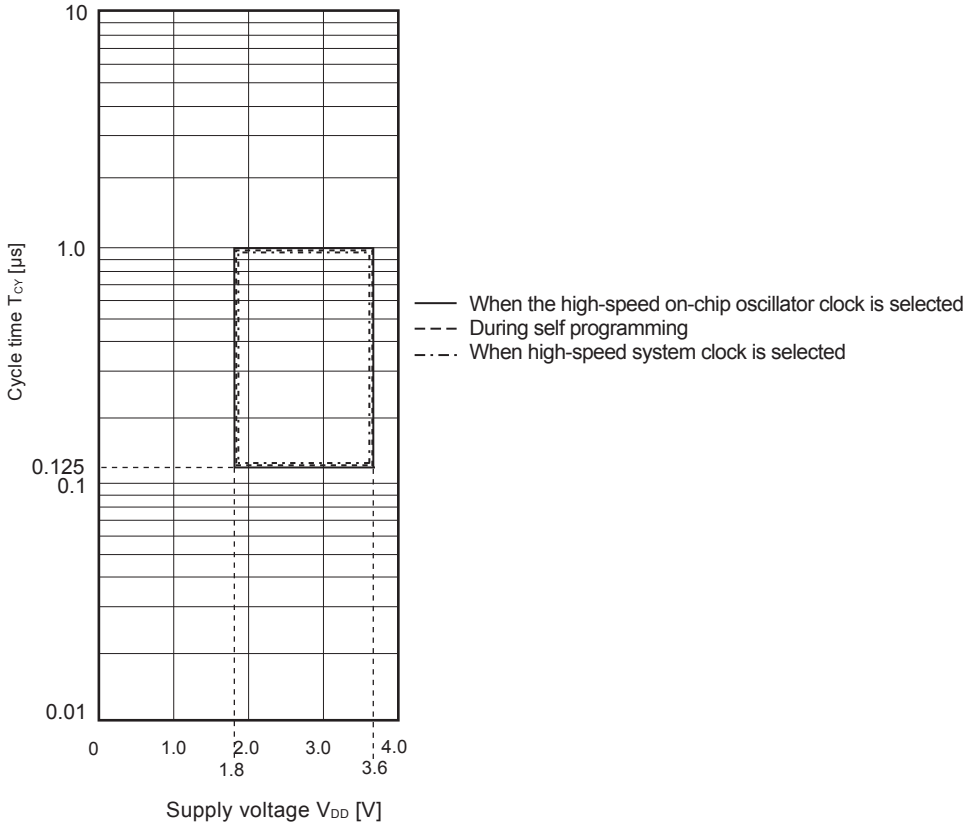
(1) Operating current

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

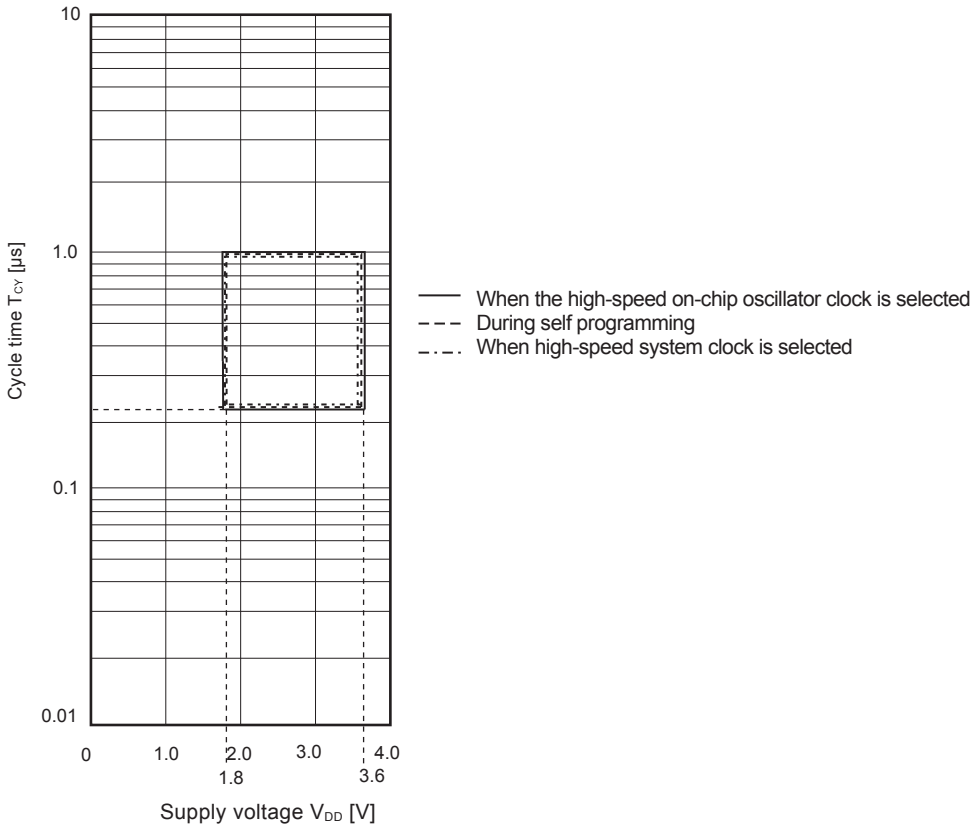
Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Operating current Note 1	I_{DD1}	HS (high-speed main) mode Note 5	Basic operation	f_{IH} = 32 MHz Note 2	V_{DD} = 3.0 V		2.3		mA
			Normal operation	f_{IH} = 32 MHz Note 2	V_{DD} = 3.0 V		5.2	8.5	mA
				f_{IH} = 24 MHz Note 2	V_{DD} = 3.0 V		4.1	6.6	mA
				f_{IH} = 16 MHz Note 2	V_{DD} = 3.0 V		3.0	4.7	mA
		LS(low-speed main) mode Note 5	Normal operation	f_{IH} = 8 MHz Note 2	V_{DD} = 3.0 V		1.3	2.1	mA
					V_{DD} = 2.0 V		1.3	2.1	mA
		LV (low-voltage main) mode Note 5	Normal operation	f_{IH} = 4 MHz Note 2	V_{DD} = 3.0 V		1.3	1.8	mA
					V_{DD} = 2.0 V		1.3	1.8	mA
		HS (high-speed main) mode Note 5	Normal operation	f_{MX} = 20 MHz Note 3	V_{DD} = 3.0 V Note 6		3.4	5.5	mA
							3.6	5.7	mA
				f_{MX} = 10 MHz Note 3	V_{DD} = 3.0 V Note 6		2.1	3.2	mA
							2.1	3.2	mA
		LS (low-speed main) mode Note 5	Normal operation	f_{MX} = 8 MHz Note 3	V_{DD} = 3.0 V Note 6		1.2	2.0	mA
							1.2	2.0	mA
					V_{DD} = 2.0 V Note 6		1.2	2.0	mA
							1.2	2.0	mA
		Subsystem clock operation	Normal operation	f_{SUB} = 32.768 kHz Note 4	T_A = -40°C Note 6		4.8	5.9	µA
							4.9	6.0	µA
					T_A = +25°C Note 6		4.9	5.9	µA
							5.0	6.0	µA
					T_A = +50°C Note 6		5.0	7.6	µA
							5.1	7.7	µA
					T_A = +70°C Note 6		5.2	9.3	µA
							5.3	9.4	µA
					T_A = +85°C Note 6		5.7	13.3	µA
							5.8	13.4	µA

(**Notes** and **Remarks** are listed on the next page.)

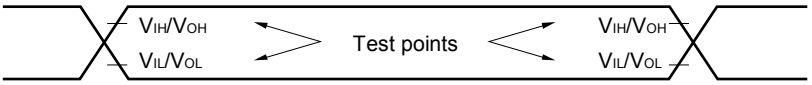
T_{CY} vs V_{DD} (LS (low-speed main) mode)



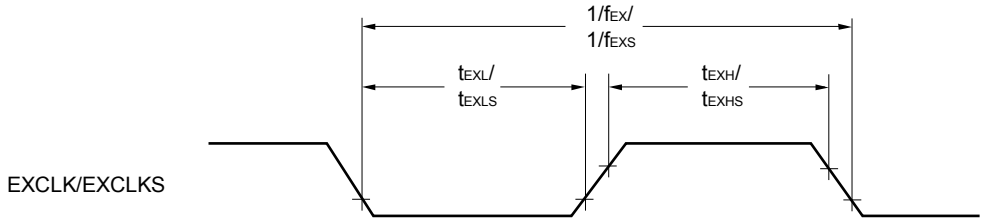
T_{CY} vs V_{DD} (LV (low-voltage main) mode)



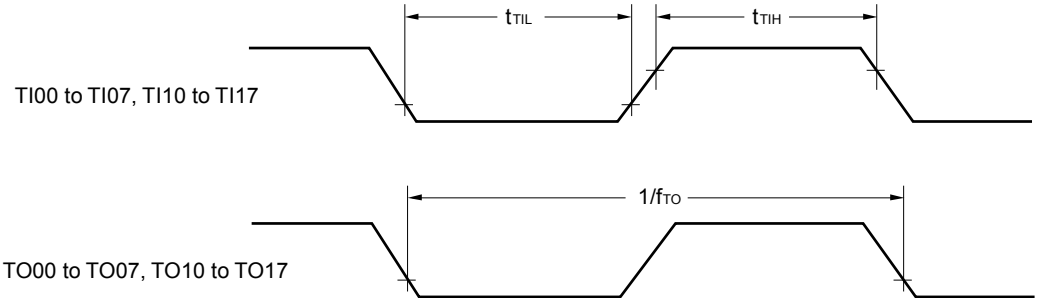
AC Timing Test Points



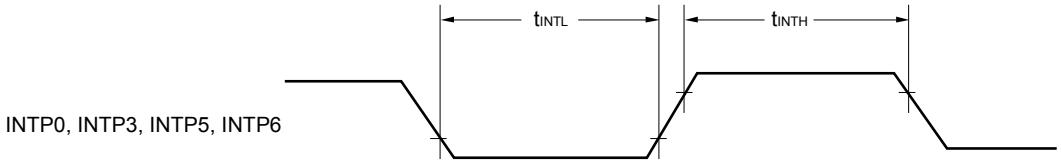
External System Clock Timing



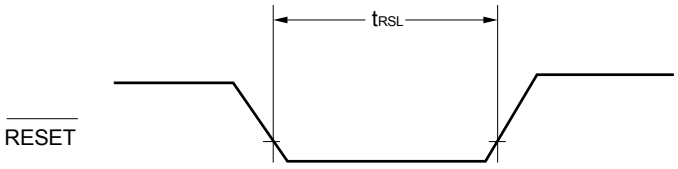
TI/TO Timing



Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



(3) During communication at same potential (CSI mode) (Internal communication, supporting CSI21 only)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ $2/f_{CLK}$ Note	2.4 V ≤ V_{DD} ≤ 3.6 V	250		250		500		ns
			1.8 V ≤ V_{DD} ≤ 3.6 V	–		250		500		ns
			1.6 V ≤ V_{DD} ≤ 3.6 V	–		–		500		ns

Note Use the f_{CLK} more than 6.5 MHz and lower than 24 MHz.

Remark This specification is for CSI21 only.

(6) During communication at same potential (simplified I^2C mode) (1/2)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		400 Note 1		400 Note 1	kHz
		2.4 V ≤ V_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ V_{DD} < 3.6 V, C_b = 100 pF, R_b = 3 kΩ		–		400 Note 1		400 Note 1	kHz
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		–		300 Note 1		300 Note 1	kHz
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		–		–		250 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ V_{DD} < 3.6 V, C_b = 100 pF, R_b = 3 kΩ	–		1150		1150		ns
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	–		1550		1550		ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–		–		1850		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ V_{DD} < 3.6 V, C_b = 100 pF, R_b = 3 kΩ	–		1150		1150		ns
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	–		1550		1550		ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–		–		1850		ns

(**Notes**, **Caution**, and **Remarks** are listed on the page after the next page.)

Maximum transfer rate = 1/{-Cb × Rb × ln (1 - 1.5/Vb)} × 3 [bps]

Baud rate error (theoretical value) =

(1/transfer rate × 2 - {-Cb × Rb × ln (1 - 1.5/Vb)} / (1/transfer rate) × number of transferred bits)

Note 7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

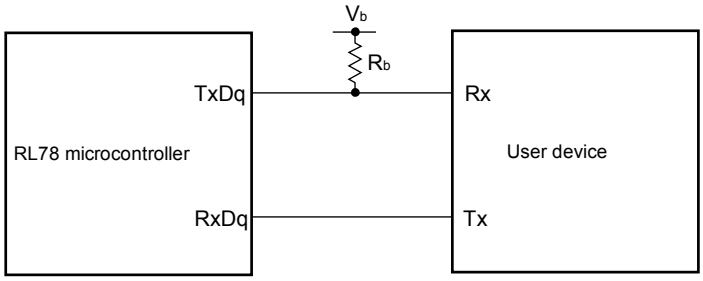
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]:Communication line (TxDq) pull-up resistance,
C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

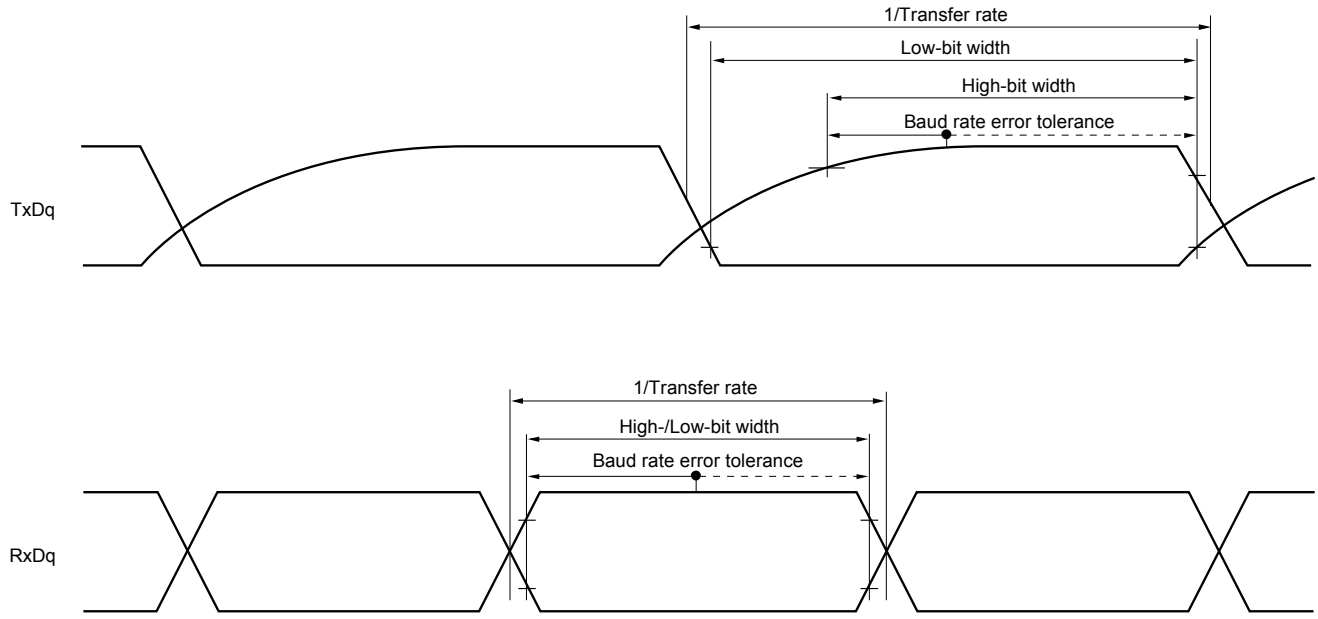
2. q: UART number (q = 0, 1), g: PIM and POM numbers (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03))

UART mode connection diagram (during communication at different potential)



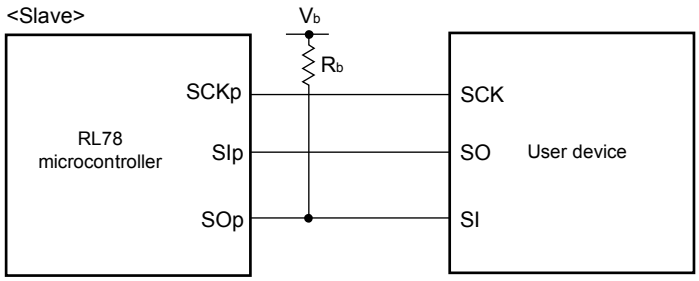
UART mode bit width (during communication at different potential) (reference)



Remarks1. R_b[Ω]:Communication line (TxDq) pull-up resistance, V_b[V]: Communication line voltage

2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

CSI mode connection diagram (during communication at different potential)



Remarks 1. R_b[Ω]:Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 20), m: Unit number, n: Channel number (mn = 00, 10), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 10))

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 135 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 100 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 100 pF, R_b = 5.5 kΩ	$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 100 pF, R_b = 5.5 kΩ	–		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 50 pF, R_b = 2.7 kΩ	0 Note 4	305	0 Note 4	305	0 Note 4	305	ns
		2.7 V ≤ V_{DD} ≤ 3.6 V 2.3 V ≤ V_b ≤ 2.7 V C_b = 100 pF, R_b = 2.7 kΩ	0 Note 4	355	0 Note 4	355	0 Note 4	355	ns
		2.4 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V C_b = 100 pF, R_b = 5.5 kΩ	0 Note 4	405	0 Note 4	405	0 Note 4	405	ns
		1.8 V ≤ V_{DD} < 3.3 V 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 100 pF, R_b = 5.5 kΩ	–	–	0 Note 4	405	0 Note 4	405	ns

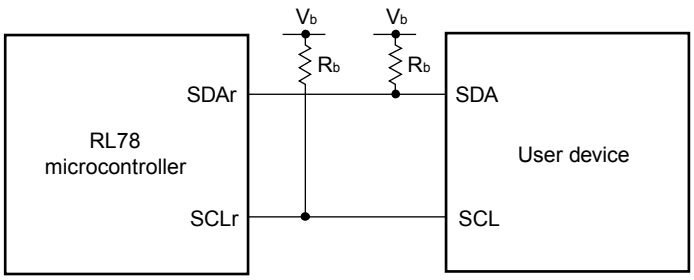
Notes 1. The value must also be f_{MCK}/4 or lower.

2. Use it with $V_{DD} \geq V_b$.

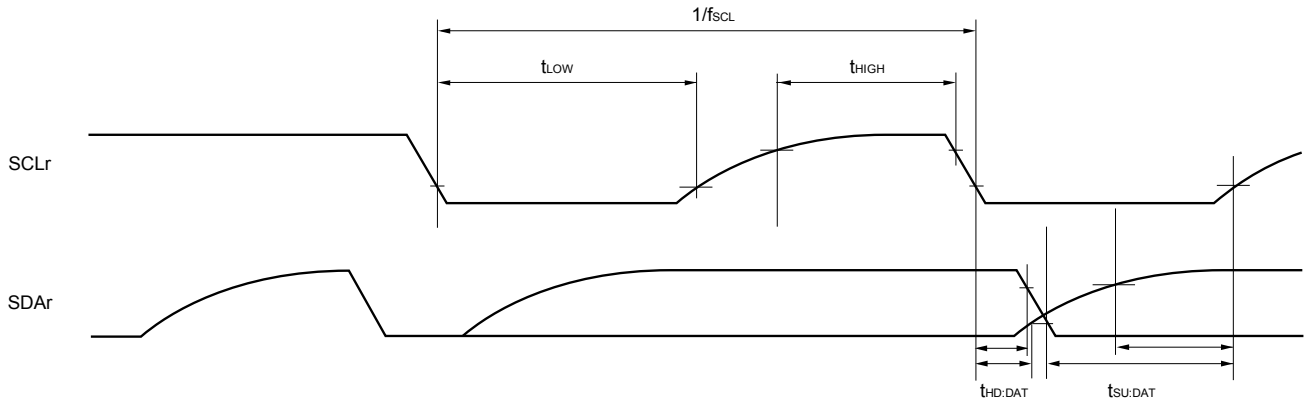
3. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remarks 1. R_b[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 00, 10), g: PIM, POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02))

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.
Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), conversion target : ANI0 to ANI3, ANI16 to ANI19, Internal reference voltage, Temperature sensor output voltage

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V		1.2	±7.0	LSB
			1.6 V ≤ V_{DD} ≤ 3.6 V Note 3		1.2	±10.5	LSB
Conversion time	T_{conv}	10-bit resolution conversion target : ANI0 to ANI3, ANI16 to ANI19	2.7 V ≤ V_{DD} ≤ 3.6 V	3.1875		39	µs
			1.8 V ≤ V_{DD} ≤ 3.6 V	17		39	µs
			1.6 V ≤ V_{DD} ≤ 3.6 V	57		95	µs
		10-bit resolution conversion target : Internal reference voltage, Temperature sensor output voltage (HS (high-speed main) Mode)	2.7 V ≤ V_{DD} ≤ 3.6 V	3.5635		39	µs
			2.7 V ≤ V_{DD} ≤ 3.6 V	17		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±0.60	%FSR
			1.6 V ≤ V_{DD} ≤ 3.6 V Note 3			±0.85	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±0.60	%FSR
			1.6 V ≤ V_{DD} ≤ 3.6 V Note 3			±0.85	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±4.0	LSB
			1.6 V ≤ V_{DD} ≤ 3.6 V Note 3			±6.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±2.0	LSB
			1.6 V ≤ V_{DD} ≤ 3.6 V Note 3			±2.5	LSB
<R> Analog input voltage	V_{AIN}	ANI0 to ANI3, ANI16 to ANI19		0		V_{DD}	V
		Select internal reference voltage 2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode		V_{BGR} Note 4			V
		Select temperature sensor output voltage 2.4 V ≤ V_{DD} ≤ 3.6 V, HS (high-speed main) mode		V_{TMPS25} Note 4			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the the conversion time is set to 57 µs (min.) and 95 µs (max.).

4. Refer to **2.8.2 Temperature sensor and internal reference voltage characteristics**

LVD Detection Voltage of Interrupt & Reset Mode
(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDA0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 0, falling reset voltage		1.60	1.63	1.66	V
	V_{LVDA1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	V_{LVDA2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.8	1.84	1.87	V
	V_{LVDA3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDB0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1, falling reset voltage		1.80	1.84	1.87	V
	V_{LVDB1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVDB2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVDB3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVDC0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	V_{LVDC1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	V_{LVDD1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V

2.8.5 Supply voltage rise time

(T_A = –40 to +85°C, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD} rise slope	S_{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.6 AC Characteristics.

2.9 RF Transceiver Characteristics

2.9.1 RF transmission characteristics

Unless specified otherwise, the measurement is performed by our evaluation board.

(T_A = +25°C, V_{DD} = V_{DD_RF} = AV_{DD_RF} = 3.0 V, f = 2440 MHz, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RF frequency range	RF_{CF}			2402		2480	MHz
Data rate	RF_{DATA}				1		Mbps
Maximum transmitted output power	RF_{POWER}	RF output pin	RF low power mode	-18	-15	-12	dBm
			RF normal mode	-3	0	3	dBm
			RF high performance mode	-3	0	3	dBm
Transmitted output power setting	RF_{TXPOW}	0, -1, -2, -7, -10, -15 dBm		-15		0	dBm
Spurious radiation	RF_{TXSP}	30 to 88 MHz			-76	-55	dBm
		88 to 216 MHz			-76	-52	dBm
		216 to 960 MHz			-74	-49	dBm
		960 to 1000 MHz			-74	-30	dBm
		1 to 12.75 GHz			-42	-41	dBm
		1.8 to 1.9 GHz			-73	-47	dBm
		5.15 to 5.3 GHz			-71	-47	dBm
Harmonics	RF_{TXHC1}	2^{nd} Harmonics			-52	-41	dBm
	RF_{TXHC2}	3^{rd} Harmonics			-51	-41	dBm
Frequency tolerance	RF_{TXFERR}			-30		+30	ppm
Impedance	RF_{Z1}				50+j0		Ω

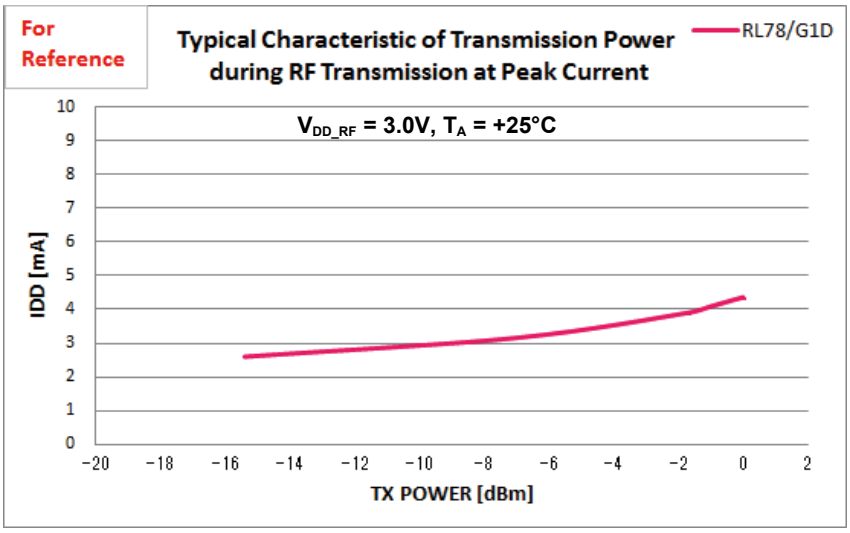
Caution Install EMI countermeasures as required to prevent EMI effects of the RF transmission characteristics.

2.9.2 RF reception characteristics

Unless specified otherwise, the measurement is performed by our evaluation board.

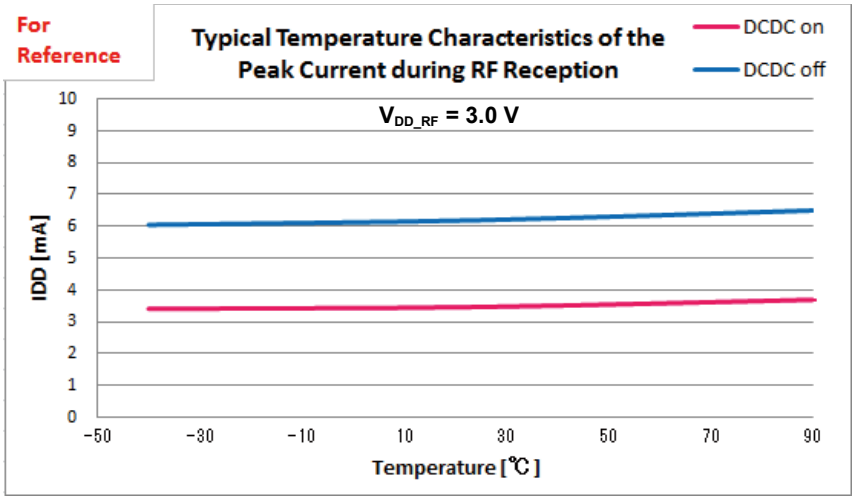
(T_A = +25°C, V_{DD} = V_{DD_RF} = AV_{DD_RF} = 3.0 V, f = 2440 MHz, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RF input frequency	RF_{RXFRIN}			2402		2480	MHz
Maximum input level	RF_{LEVL}	PER ≤ 30.8% RF input pin	RF low power mode	-10	0	-	dBm
			RF normal mode	-10	1	-	dBm
			RF high performance mode	-10	1	-	dBm
Receiver sensitivity	RF_{STY}	PER ≤ 30.8%	RF low power mode	-	-60	-50	dBm
			RF normal mode	-	-90	-70	dBm
			RF high performance mode	-	-92	-70	dBm
Secondary radiation	RF_{RXSP}		30 MHz to 1 GHz	-	-72	-57	dBm/ 100 kHz
			1 GHz to 12 GHz	-	-57	-54	dBm/ 100 kHz
Common channel rejection ratio	RF_{CCR}	PER ≤ 30.8%, Prf = –67dBm		-21	-12	-	dB
Adjacent channel rejection ratio	RF_{ADCR}	PER ≤ 30.8% Prf = –67 dBm	±1 MHz	-15	-5	-	dB
			±2 MHz	17	29	-	dB
			±3 MHz	27	34	-	dB
Blocking	RF_{BLK}	PER ≤ 30.8% Prf = –67 dBm	30 MHz - 2000 MHz	-30	-13	-	dB
			2000 MHz to 2399 MHz	-35	-30	-	dBm
			2484 MHz to 3000 MHz	-35	-30	-	dBm
			> 3000 MHz	-30	-17	-	dBm
Frequency tolerance	RF_{RXFERR}	PER ≤ 30.8%		-250		+250	kHz
RSSI accuracy	RF_{RSSIS}	T_A = +25°C, –70 dBm ≤ Prf ≤ –10 dBm		-4	0	4	dB



(2) Peak Current during RF Reception

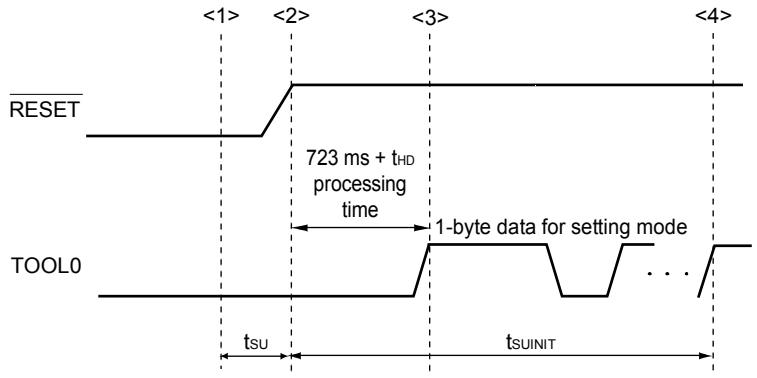
Unless specified otherwise, the measurement is performed by our evaluation board.
Current consumption is not including MCU unit.



2.13 Timing of Entry to Flash Memory Programming Modes

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = V_{DD_RF} = AV_{DD_RF} ≤ 3.6 V, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.		100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10		μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1		ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.
t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level
t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)