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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	FlexIO, I²C, SPI, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	58
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	68K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke14f256vlh16

1 Ordering information

The following chips are available for ordering.

Table 1. Ordering information

Product		Memory			Package		IO and ADC channel			Communication
Part number	Marking (Line1/Line2)	Flash (KB)	SRAM (KB)	FlexNVM/ FlexRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/HD)[1]	ADC channels	FlexCAN
MKE18F512VLL16	MKE18F512 / VLL16	512	64	64/4	100	LQFP	89	89/8	16	2
MKE18F512VLH16	MKE18F512 / VLH16	512	64	64/4	64	LQFP	58	58/8	16	2
MKE18F256VLL16	MKE18F256 / VLL16	256	32	64/4	100	LQFP	89	89/8	16	2
MKE18F256VLH16	MKE18F256 / VLH16	256	32	64/4	64	LQFP	58	58/8	16	2
MKE16F512VLL16	MKE16F512 / VLL16	512	64	64/4	100	LQFP	89	89/8	16	1
MKE16F512VLH16	MKE16F512 / VLH16	512	64	64/4	64	LQFP	58	58/8	16	1
MKE16F256VLL16	MKE16F256 / VLL16	256	32	64/4	100	LQFP	89	89/8	16	1
MKE16F256VLH16	MKE16F256 / VLH16	256	32	64/4	64	LQFP	58	58/8	16	1
MKE14F512VLL16	MKE14F512 / VLL16	512	64	64/4	100	LQFP	89	89/8	16	0
MKE14F512VLH16	MKE14F512 / VLH16	512	64	64/4	64	LQFP	58	58/8	16	0
MKE14F256VLL16	MKE14F256 / VLL16	256	32	64/4	100	LQFP	89	89/8	16	0
MKE14F256VLH16	MKE14F256 / VLH16	256	32	64/4	64	LQFP	58	58/8	16	0

1. INT: interrupt pin numbers; HD: high drive pin numbers

2 Overview

The following figure shows the system diagram of this device.

2.1.1 ARM Cortex-M4 core

The ARM Cortex-M4 is the member of the Cortex M Series of processors targeting microcontroller cores focused on very cost sensitive, deterministic, interrupt driven environments. The Cortex M4 processor is based on the ARMv7 Architecture and Thumb®-2 ISA and is upward compatible with the Cortex M3, Cortex M1, and Cortex M0 architectures. Cortex M4 improvements include an ARMv7 Thumb-2 DSP (ported from the ARMv7-A/R profile architectures) providing 32-bit instructions with SIMD (single instruction multiple data) DSP style multiply-accumulates and saturating arithmetic.

2.1.2 NVIC

The Nested Vectored Interrupt Controller supports nested interrupts and 16 priority levels for interrupts. In the NVIC, each source in the IPR registers contains 4 bits. It also differs in number of interrupt sources and supports 240 interrupt vectors.

The Cortex-M family uses a number of methods to improve interrupt latency . It also can be used to wake the MCU core from Wait and VLPW modes.

2.1.3 AWIC

The asynchronous wake-up interrupt controller (AWIC) is used to detect asynchronous wake-up events in Stop mode and signal to clock control logic to resume system clocking. After clock restarts, the NVIC observes the pending interrupt and performs the normal interrupt or event processing. The AWIC can be used to wake MCU core from Partial Stop, Stop and VLPS modes.

Wake-up sources for this SoC are listed as below:

Table 2. AWIC Stop and VLPS Wake-up Sources

Wake-up source	Description
Available system resets	RESET pin, WDOG, JTAG , loss of clock(LOC) reset and loss of lock (LOL) reset
Pin interrupts	Port Control Module - Any enabled pin interrupt is capable of waking the system
ADCx	ADCx is optional functional with clock source from SIRC or OSC
CMPx	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPI2C	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPUART	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPSPI	Functional in Stop/VLPS modes with clock source from SIRC or OSC

Table continues on the next page...

segments is controlled as the FAC provides a cycle-by-cycle evaluation of the access rights for each transaction routed to the on-chip flash memory. Configurability allows an increasing number of protected segments while supporting two levels of vendors adding their proprietary software to a device.

2.1.7.2 Error-correcting code (ECC)

The ECC detection is also supported on Flash and SRAM memories. It supports auto correction of one-bit error and reporting more than one-bit error.

2.1.8 Power management

The Power Management Controller (PMC) expands upon ARM's operational modes of Run, Sleep, and Deep Sleep, to provide multiple configurable modes. These modes can be used to optimize current consumption for a wide range of applications. The WFI or WFE instruction invokes a Wait or a Stop mode, depending on the current configuration. For more information on ARM's operational modes, See the ARM® Cortex® User Guide.

The PMC provides High Speed Run (HSRUN), Normal Run (RUN), and Very Low Power Run (VLPR) configurations in ARM's Run operation mode. In these modes, the MCU core is active and can access all peripherals. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption. The configuration that matches the power versus performance requirements of the application can be selected.

The PMC provides Wait (Wait) and Very Low Power Wait (VLPW) configurations in ARM's Sleep operation mode. In these modes, even though the MCU core is inactive, all of the peripherals can be enabled and operate as programmed. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption.

The PMC provides Stop (Stop), Very Low Power Stop (VLPS) configurations in ARM's Deep Sleep operational mode. In these modes, the MCU core and most of the peripherals are disabled. Depending on the requirements of the application, different portions of the analog, logic, and memory can be retained or disabled to conserve power.

- Transmit and receive baud rate can operate asynchronous to the bus clock and can be configured independently of the bus clock frequency, support operation in Stop mode
- Interrupt, DMA or polled operation
- Hardware parity generation and checking
- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods
  - Idle line wakeup
  - Address mark wakeup
  - Receive data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity

2.2.12 LPSPI

This device contains two LPSPI modules. The LPSPI is a low power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus as a master and/or a slave. The LPSPI can continue operating in stop modes provided an appropriate clock is available and is designed for low CPU overhead with DMA offloading of FIFO register accesses.

The LPSPI modules have the following features:

- Command/transmit FIFO of 4 words
- Receive FIFO of 4 words
- Host request input can be used to control the start time of an SPI bus transfer

2.2.13 FlexCAN

This device contains two FlexCAN modules. The FlexCAN module is a communication controller implementing the CAN protocol according to the ISO 11898-1 standard and CAN 2.0 B protocol specifications.

4 Pinouts

4.1 KE1xF Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

On this device, there are several special ADC channels which support hardware interleave between multiple ADCs. Taking ADC0_SE4 and ADC1_SE14 channels as an example, these two channels can work independently, but they can also be hardware interleaved. In the hardware interleaved mode, a signal on the pin PTB0 can be sampled by both ADC0 and ADC1. The interleaved mode is enabled by SIM_CHIPCTL[ADC_INTERLEAVE_EN] bits. For more information, see "ADC Hardware Interleaved Channels" in the ADC chapter of Reference Manual.

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	10	VREFL/ VSS	VREFL/ VSS	VREFL/ VSS							
1	—	PTE16	DISABLED		PTE16			FTM2_CH7		FXIO_D3	TRGMUX_ OUT7
2	—	PTE15	DISABLED		PTE15			FTM2_CH6		FXIO_D2	TRGMUX_ OUT6
3	1	PTD1	ADC2_SE1	ADC2_SE1	PTD1	FTM0_CH3	LPSPI1_SIN	FTM2_CH1		FXIO_D1	TRGMUX_ OUT2
4	2	PTD0	ADC2_SE0	ADC2_SE0	PTD0	FTM0_CH2	LPSPI1_SCK	FTM2_CH0		FXIO_D0	TRGMUX_ OUT1
5	3	PTE11	ADC2_SE13	ADC2_SE13	PTE11	PWT_IN1	LPTMR0_ ALT1	FTM2_CH5		FXIO_D5	TRGMUX_ OUT5
6	4	PTE10	ADC2_SE12	ADC2_SE12	PTE10	CLKOUT		FTM2_CH4		FXIO_D4	TRGMUX_ OUT4
7	—	PTE13	DISABLED		PTE13			FTM2_FLT0			
8	5	PTE5	DISABLED		PTE5	TCLK2	FTM2_QD_ PHA	FTM2_CH3	CAN0_TX	FXIO_D7	EWM_IN
9	6	PTE4	DISABLED		PTE4	BUSOUT	FTM2_QD_ PHB	FTM2_CH2	CAN0_RX	FXIO_D6	EWM_OUT_b

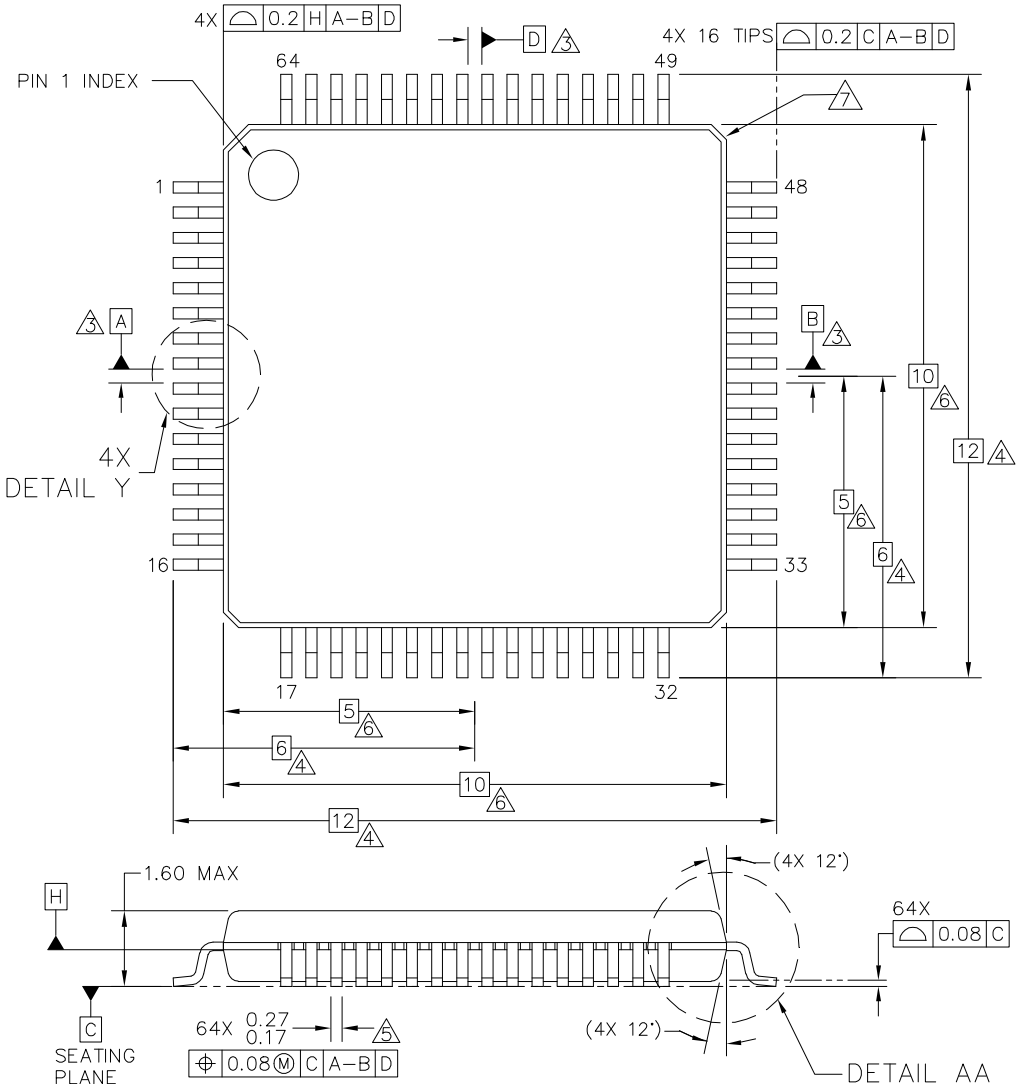

Figure 11. 64-pin LQFP package dimensions 1

Table 28. DC electrical specifications (continued)

Symbol	Parameter	Value			Unit	Notes
		Min	Typ	Max		
V_{il}	Input Buffer Low Voltage @ V_{DD} = 3.3 V	V_{SS} – 0.3	—	0.3 × V_{DD}	V	
	@ V_{DD} = 5.0 V	V_{SS} – 0.3	—	0.35 × V_{DD}	V	
V_{hys}	Input Buffer Hysteresis	0.06 × V_{DD}	—	—	V	
Ioh_5	Normal drive I/O current source capability measured when pad = (V_{DDE} – 0.8 V) @ V_{DD} = 3.3 V	2.8	—	—	mA	
	@ V_{DD} = 5.0 V	4.8	—	—	mA	
Iol_5	Normal drive I/O current sink capability measured when pad = 0.8 V @ V_{DD} = 3.3 V	2.4	—	—	mA	
	@ V_{DD} = 5.0 V	4.4	—	—	mA	
Ioh_20	High drive I/O current source capability measured when pad = (V_{DDE} – 0.8 V)[2] @ V_{DD} = 3.3 V	10.8	—	—	mA	
	@ V_{DD} = 5.0 V	18.5	—	—	mA [3]	
Iol_20	High drive I/O current sink capability measured when pad = 0.8 V[4] @ V_{DD} = 3.3 V	10.1	—	—	mA	
	@ V_{DD} = 5.0 V	18.5	—	—	mA [3]	
I_leak	Hi-Z (Off state) leakage current (per pin)	—	—	300	nA	5, 6
V_{OH}	Output high voltage					7
	Normal drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –2.8 mA)	V_{DD} – 0.8	—	—	V	
	Normal drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –4.8 mA)	V_{DD} – 0.8	—	—	V	
	High drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –10.8 mA)	V_{DD} – 0.8	—	—	V	
	High drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –18.5 mA)	V_{DD} – 0.8	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage					7
	Normal drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –2.8 mA)	—	—	0.8	V	
	Normal drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –4.8 mA)	—	—	0.8	V	
	High drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –10.8 mA)	—	—	0.8	V	
	High drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –18.5 mA)	—	—	0.8	V	

Table continues on the next page...

5.3.2.5 AC specifications at 5 V range

Table 37. Functional pad AC specifications

Characteristic	Symbol	Min	Typ	Max	Unit
I/O Supply Voltage	Vdd [1]	4		5.5	V

1. Max power supply ramp rate is 500 V/ms.

Name	Prop Delay (ns) [1]	Rise/Fall Edge (ns) [2]		Drive Load (pF)
	Max	Min	Max	
Normal drive I/O pad	12	3.6	10	25
	18	8	17	50
High drive I/O pad	13	3.6	10	25
	19	8	19	50
CMOS Input [3]	3	1.2	2.8	0.5

1. As measured from 50% of core side input to 50% of the output.
2. Edges measured using 20% and 80% of the VDD supply.
3. Input slope = 2 ns.

NOTE

All measurements were taken accounting for 150 mV drop across VDD and VSS.

5.3.3 Thermal specifications

5.3.3.1 Thermal operating requirements

Table 38. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + R_{\Theta JA} \times$ chip power dissipation.

5.3.3.2 Thermal attributes

Table 40. Thermal characteristics for the 100-pin LQFP package (continued)

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	44	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	47	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	38	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	30	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	14	°C/W
Thermal resistance, Junction to Package Top[6]	Natural Convection	ψ_{JT}	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.3.3.2.4 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

5.4.1 System modules

There are no specifications necessary for the device's system modules.

5.4.2 Clock interface modules

5.4.2.1 Oscillator electrical specifications

5.4.2.1.1 External Oscillator electrical specifications

Table 55. Comparator with 8-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ. [1]	Max.	Unit
	within ambient temperature range	—	48	133	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	within ambient temperature range	—	33	80	
I_{DAC8b}	8-bit DAC current adder (enabled)	—	10	16	µA
INL	8-bit DAC integral non-linearity	–0.6	—	0.5	LSB[5]
DNL	8-bit DAC differential non-linearity	–0.5	—	0.5	LSB

1. Typical values assumed at VDDA = 5.0 V, Temp = 25 °C, unless otherwise stated.
2. Difference at input > 200mV
3. Applied ± (100 mV + Hyst) around switch point
4. Applied ± (30 mV + 2 × Hyst) around switch point
5. 1 LSB = $V_{reference}/256$

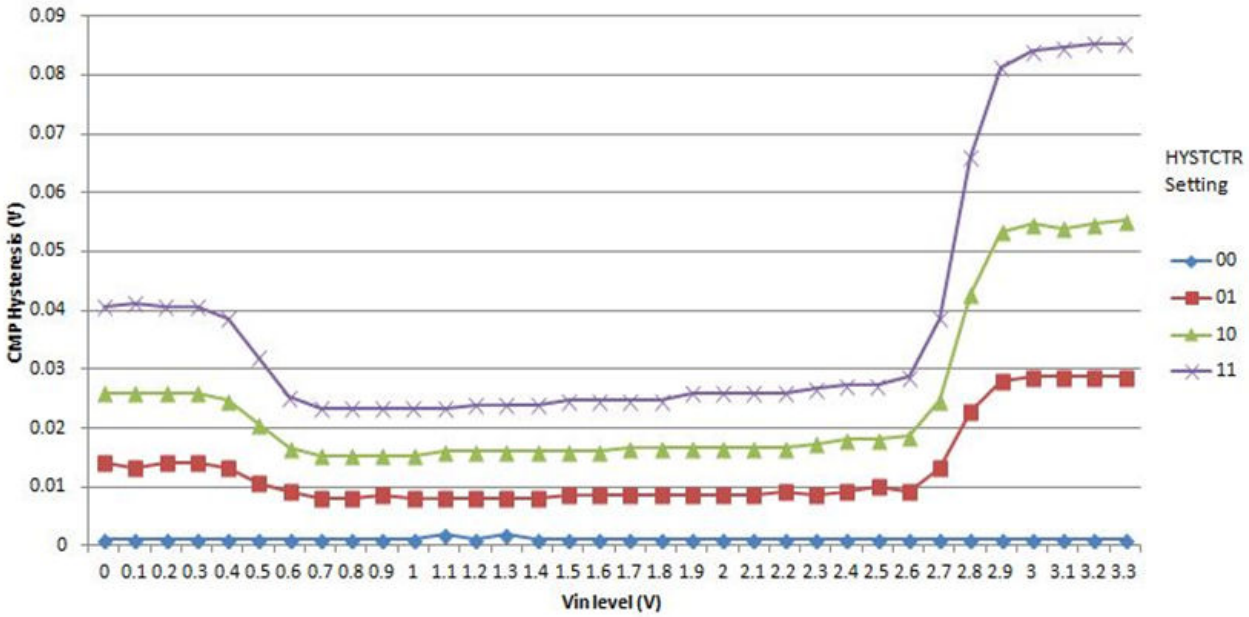

Figure 20. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

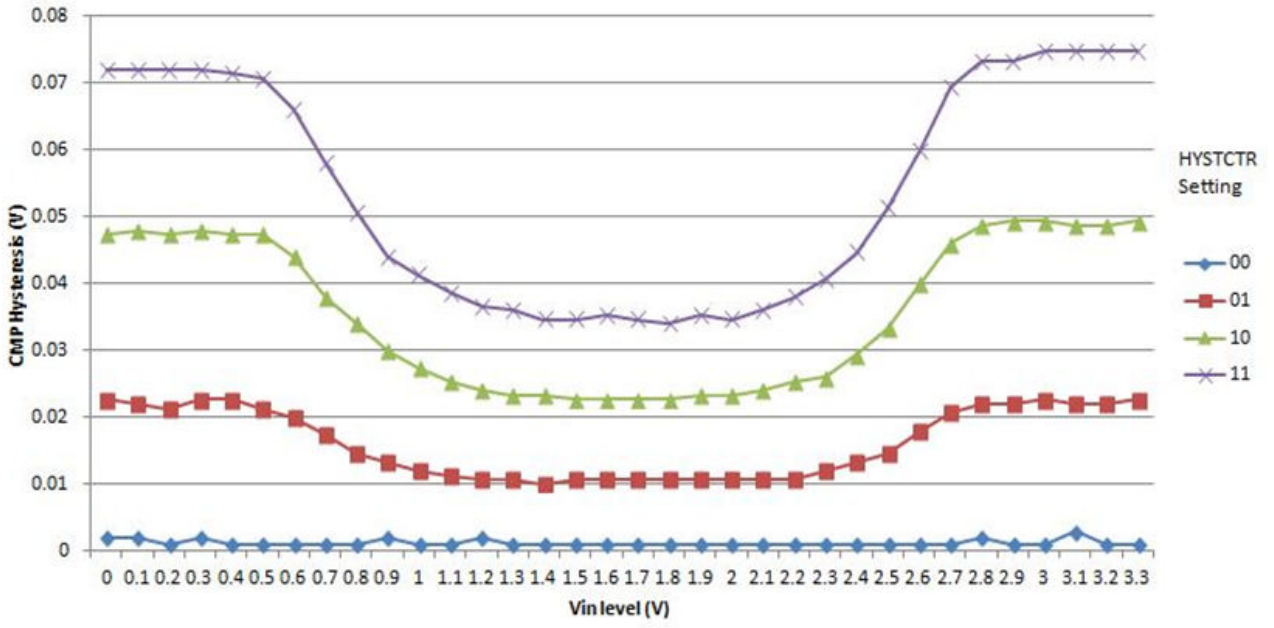

Figure 21. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

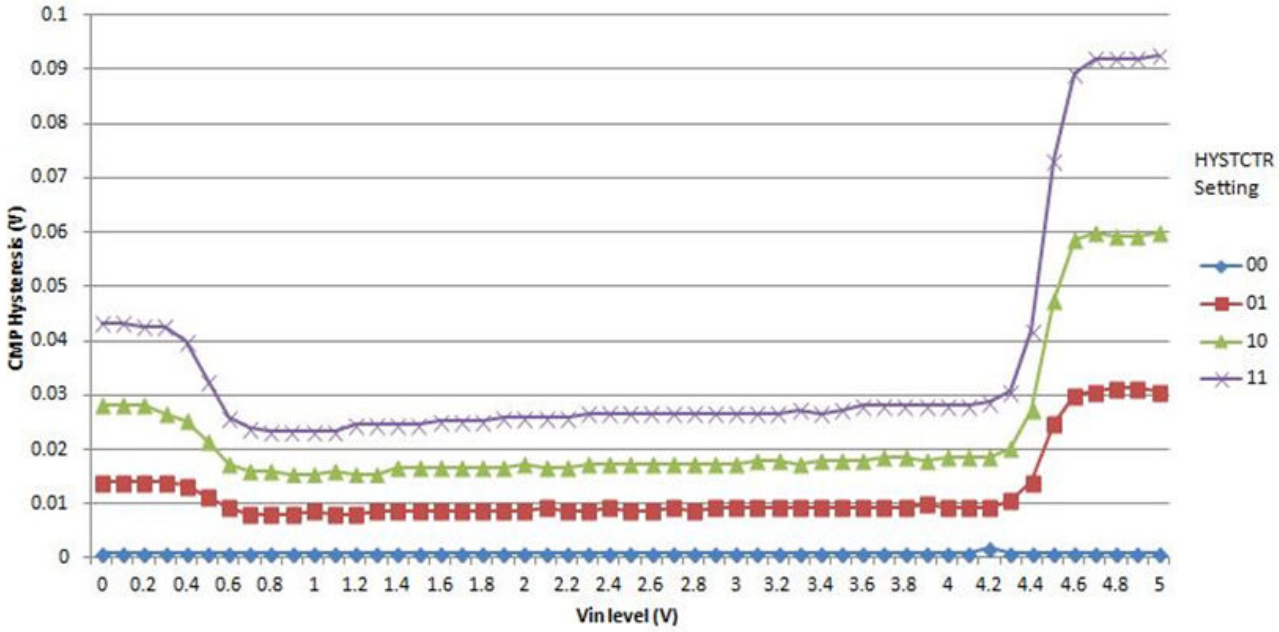

Figure 22. Typical hysteresis vs. Vin level (VDD = 5 V, PMODE = 0)

Table 57. 12-bit DAC operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	µs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode	—	—	5	µs	1
$t_{CCDACHP}$	Code-to-code settling time (0xBF8 to 0xC08) — high-power mode	—	0.7	—	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-power mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-power mode, no load, DAC set to 0xFFF	V_{DACR} – 100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high-power mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	3
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	4
E_G	Gain error	—	±0.1	±0.6	%FSR	4
PSRR	Power supply rejection ratio					
	High-power mode, code set to 3FF or BFF		68		dB	5
	Low-power mode, code set to 3FF or BFF		60			
T_{CO}	Temperature coefficient offset voltage	—	5	—	µV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
SR	Slew rate -80h→ F7Fh→ 80h • High power (SP_{HP}) • Low power (SP_{LP})	1 0.05	1.5 0.12	— —	V/µs	

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} –100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV with V_{DDA} > 2.4 V
4. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} – 100 mV
5. DAC reference to VREFH (DACREF_1)
6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

5.4.6 Communication interfaces

5.4.6.1 LPUART electrical specifications

Refer to General AC specifications for LPUART specifications.

5.4.6.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.

Table 58. LPSPI master mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} = LPSPI peripheral clock
2. $t_{periph} = 1/f_{periph}$

NOTE

High drive pin should be used for fast bit rate.

Table 59. LPSPI slave mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.5	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	31	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} = LPSPI peripheral clock
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

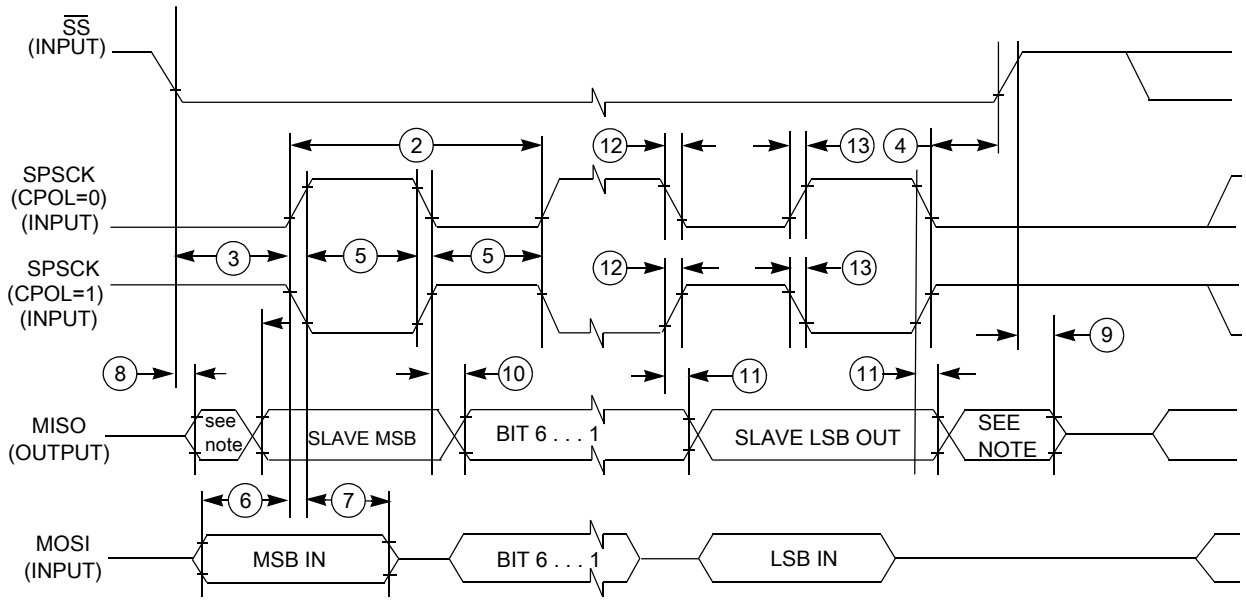

Figure 26. LPSPI slave mode timing (CPHA = 0)

5.4.7.2 JTAG electricals

Table 62. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	Boundary Scan	0	10	
	JTAG and CJTAG	0	20	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			ns
	Boundary Scan	50	—	
	JTAG and CJTAG	25	—	
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	19	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

Table 63. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
V_{DDA}	Operating voltage	2.7	5.5	V
J1	TCLK frequency of operation			MHz
	Boundary Scan	0	10	
	JTAG and CJTAG	0	15	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			ns
	Boundary Scan	50	—	
	JTAG and CJTAG	33	—	
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.4	—	ns
J7	TCLK low to boundary scan output data valid	—	27	ns
J8	TCLK low to boundary scan output high-Z	—	27	ns

Table continues on the next page...

Table 63. JTAG full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	26.2	ns
J12	TCLK low to TDO high-Z	—	26.2	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

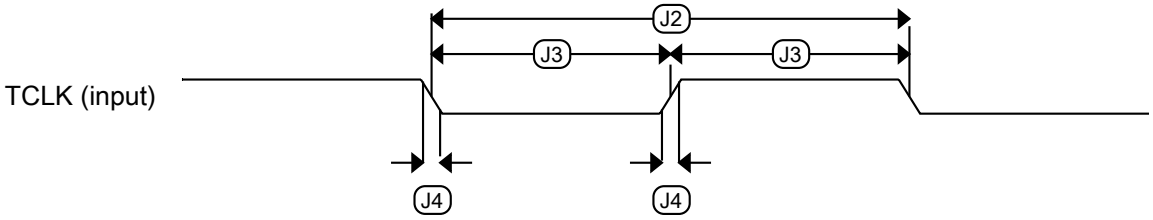

Figure 30. Test clock input timing

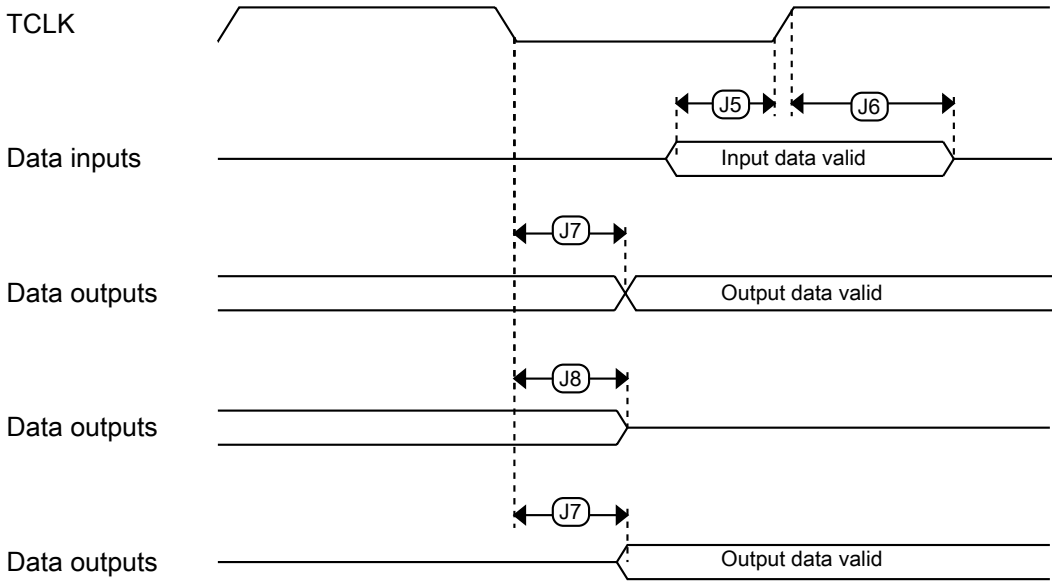

Figure 31. Boundary scan (JTAG) timing

The RESET_b pin is a pseudo open-drain I/O pin that has an internal pullup resistor. An external RC circuit is recommended to filter noise as shown in the following figure. The resistor value must be in the range of 4.7 kΩ to 10 kΩ; the recommended capacitance value is 0.1 µF. The RESET_b pin also has a selectable digital filter to reject spurious noise.

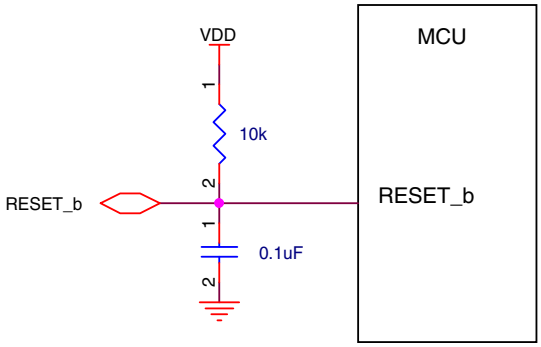

Figure 36. Reset circuit

When an external supervisor chip is connected to the RESET_b pin, a series resistor must be used to avoid damaging the supervisor chip or the RESET_b pin, as shown in the following figure. The series resistor value (RS below) must be in the range of 100 Ω to 1 kΩ depending on the external reset chip drive strength. The supervisor chip must have an active high, open-drain output.

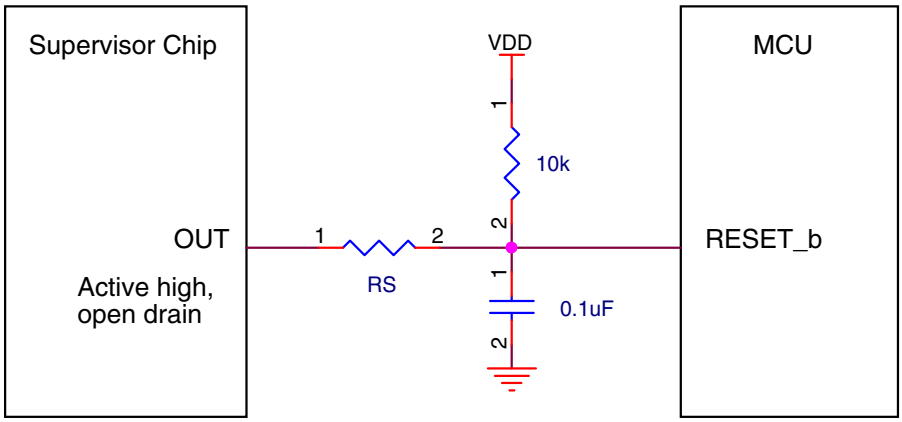

Figure 37. Reset signal connection to external reset chip

- NMI pin

Unused GPIO pins must be left floating (no electrical connections) with the MUX field of the pin's PORTx_PCRn register equal to 0:0:0. This disables the digital input path to the MCU.

6.1.5 Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

The feedback resistor, RF, is incorporated internally with the low power oscillators. An external feedback is required when using high gain (HGO=1) mode.

The series resistor, RS, is required in high gain (HGO=1) mode when the crystal or resonator frequency is below 2 MHz. Otherwise, the low power oscillator (HGO=0) must not have any series resistance; and the high frequency, high gain oscillator with a frequency above 2 MHz does not require any series resistance.

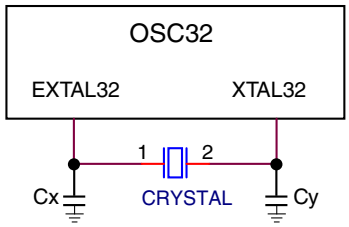

Figure 40. RTC Oscillator (OSC32) module connection – Diagram 1

Table 64. External crystal/resonator connections

Oscillator mode	Oscillator mode
Low frequency (32.768 kHz), high gain	Diagram 3
High frequency (1-32 MHz), low power	Diagram 2
High frequency (1-32 MHz), high gain	Diagram 3

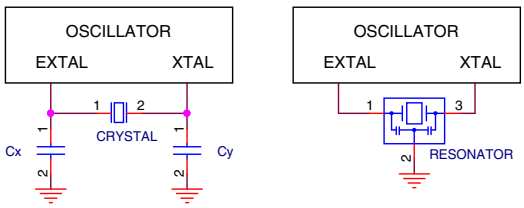

Figure 41. Crystal connection – Diagram 2

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