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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	FlexIO, I²C, SPI, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	89
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	68K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke14f256vll16

Table 2. AWIC Stop and VLPS Wake-up Sources (continued)

Wake-up source	Description
LPIT	Functional in Stop/VLPS modes with clock source from SIRC or OSC
FlexIO	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPTMR	Functional in Stop/VLPS modes
RTC	Functional in Stop/VLPS modes
SCG	Functional in Stop mode (Only SIRC)
CAN	CAN stop wakeup
NMI	Non-maskable interrupt

2.1.4 Memory

This device has the following features:

- Upto 512 KB of embedded program flash memory.
- Upto 64 KB of embedded SRAM accessible (read/write) at CPU clock speed with 0 wait states.
- The non-volatile memory is divided into several arrays:
  - 64 KB of embedded data flash memory
  - 4 KB of Emulated EEPROM
  - 16 KB ROM (built-in bootloader to support UART, I2C, and SPI interfaces)

The program flash memory contains a 16-byte flash configuration field that stores default protection settings and security information. The page size of program flash is 4 KB.

The protection setting can protect 32 regions of the program flash memory from unintended erase or program operations.

The security circuitry prevents unauthorized access to RAM or flash contents from debug port.

2.1.5 Reset and boot

The following table lists all the reset sources supported by this device.

NOTE

In the following table, Y means the specific module, except for the registers, bits or conditions mentioned in the footnote, is reset by the corresponding Reset source. N means the

specific module is not reset by the corresponding Reset source.

Table 3. Reset source

Reset sources	Descriptions	Modules									
		PMC	SIM	SMC	RCM	Reset pin is negated	WDOG	SCG	RTC	LPTMR	Others
POR reset	Power-on reset (POR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
System resets	Low-voltage detect (LVD)	Y[1]	Y	Y	Y	Y	Y	Y	N	Y	Y
	External pin reset ($\overline{\text{RESET}}$)	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Watchdog (WDOG) reset	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Multipurpose clock generator loss of clock (LOC) reset	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Multipurpose clock generator loss of lock (LOL) reset	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Stop mode acknowledge error (SACKERR)	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Software reset (SW)	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Lockup reset (LOCKUP)	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	MDM DAP system reset	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
Debug reset	Debug reset	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y

1. Except PMC_LVDSC1[LVDV] and PMC_LVDSC2[LVWV]
2. Except SIM_SOPT1
3. Except SMC_PMPROT, SMC_PMCTRL_RUM, SMC_PMCTRL_STOPM, SMC_STOPCTRL, SMC_PMSTAT
4. Except RCM_RPC, RCM_MR, RCM_FM, RCM_SRIE, RCM_SRS, RCM_SSRS
5. Except WDOG_CS[TST]
6. Except SCG_CSR and SCG_FIRCSTAT

This device supports booting from:

- internal flash
- boot ROM

segments is controlled as the FAC provides a cycle-by-cycle evaluation of the access rights for each transaction routed to the on-chip flash memory. Configurability allows an increasing number of protected segments while supporting two levels of vendors adding their proprietary software to a device.

2.1.7.2 Error-correcting code (ECC)

The ECC detection is also supported on Flash and SRAM memories. It supports auto correction of one-bit error and reporting more than one-bit error.

2.1.8 Power management

The Power Management Controller (PMC) expands upon ARM's operational modes of Run, Sleep, and Deep Sleep, to provide multiple configurable modes. These modes can be used to optimize current consumption for a wide range of applications. The WFI or WFE instruction invokes a Wait or a Stop mode, depending on the current configuration. For more information on ARM's operational modes, See the ARM® Cortex® User Guide.

The PMC provides High Speed Run (HSRUN), Normal Run (RUN), and Very Low Power Run (VLPR) configurations in ARM's Run operation mode. In these modes, the MCU core is active and can access all peripherals. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption. The configuration that matches the power versus performance requirements of the application can be selected.

The PMC provides Wait (Wait) and Very Low Power Wait (VLPW) configurations in ARM's Sleep operation mode. In these modes, even though the MCU core is inactive, all of the peripherals can be enabled and operate as programmed. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption.

The PMC provides Stop (Stop), Very Low Power Stop (VLPS) configurations in ARM's Deep Sleep operational mode. In these modes, the MCU core and most of the peripherals are disabled. Depending on the requirements of the application, different portions of the analog, logic, and memory can be retained or disabled to conserve power.

2.2.1 eDMA and DMAMUX

The eDMA is a highly programmable data-transfer engine optimized to minimize any required intervention from the host processor. It is intended for use in applications where the data size to be transferred is statically known and not defined within the transferred data itself. The DMA controller in this device implements 16 channels which can be routed from up to 63 DMA request sources through DMA MUX module.

Main features of eDMA are listed below:

- All data movement via dual-address transfers: read from source, write to destination
- 16-channel implementation that performs complex data transfers with minimal intervention from a host processor
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
- Channel activation via one of three methods
- Fixed-priority and round-robin channel arbitration
- Channel completion reported via programmable interrupt requests
- Programmable support for scatter/gather DMA processing
- Support for complex data structures

2.2.2 FTM

This device contains four FlexTimer modules.

The FlexTimer module (FTM) is a two-to-eight channel timer that supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The FTM time reference is a 16-bit counter that can be used as an unsigned or signed counter.

Several key enhancements of this module are made:

- Signed up counter
- Deadtime insertion hardware
- Fault control inputs
- Enhanced triggering functionality
- Initialization and polarity control

2.2.3 ADC

This device contains three 12-bit SAR ADC modules. The ADC module supports hardware triggers from FTM, LPTMR, PIT, RTC, external trigger pin and CMP output. It supports wakeup of MCU in low power mode when using internal clock source or external crystal clock.

ADC module has the following features:

- Linear successive approximation algorithm with up to 12-bit resolution
- Up to 16 single-ended external analog inputs
- Support 12-bit, 10-bit, and 8-bit single-ended output modes
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Input clock selectable from up to four sources
- Operation in low-power modes for lower noise
- Selectable hardware conversion trigger
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Hardware average function
- Selectable Voltage reference: from external or alternate
- Self-Calibration mode

2.2.3.1 Temperature sensor

This device contains one temperature sensor internally connected to the input channel of AD26, see ADC electrical characteristics for details of the linearity factor.

The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031 for more detailed application information of the temperature sensor.

2.2.4 DAC

The 12-bit digital-to-analog converter (DAC) is a low-power, general-purpose DAC. The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator, or ADC.

DAC module has the following features:

- On-chip programmable reference generator output. The voltage output range is from 1⁄4096 Vin to V_{in}, and the step is 1⁄4096 V_{in}, where V_{in} is the input voltage.
- V_{in} can be selected from two reference sources

4 Pinouts

4.1 KE1xF Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

On this device, there are several special ADC channels which support hardware interleave between multiple ADCs. Taking ADC0_SE4 and ADC1_SE14 channels as an example, these two channels can work independently, but they can also be hardware interleaved. In the hardware interleaved mode, a signal on the pin PTB0 can be sampled by both ADC0 and ADC1. The interleaved mode is enabled by SIM_CHIPCTL[ADC_INTERLEAVE_EN] bits. For more information, see "ADC Hardware Interleaved Channels" in the ADC chapter of Reference Manual.

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	10	VREFL/ VSS	VREFL/ VSS	VREFL/ VSS							
1	—	PTE16	DISABLED		PTE16			FTM2_CH7		FXIO_D3	TRGMUX_ OUT7
2	—	PTE15	DISABLED		PTE15			FTM2_CH6		FXIO_D2	TRGMUX_ OUT6
3	1	PTD1	ADC2_SE1	ADC2_SE1	PTD1	FTM0_CH3	LPSPI1_SIN	FTM2_CH1		FXIO_D1	TRGMUX_ OUT2
4	2	PTD0	ADC2_SE0	ADC2_SE0	PTD0	FTM0_CH2	LPSPI1_SCK	FTM2_CH0		FXIO_D0	TRGMUX_ OUT1
5	3	PTE11	ADC2_SE13	ADC2_SE13	PTE11	PWT_IN1	LPTMR0_ ALT1	FTM2_CH5		FXIO_D5	TRGMUX_ OUT5
6	4	PTE10	ADC2_SE12	ADC2_SE12	PTE10	CLKOUT		FTM2_CH4		FXIO_D4	TRGMUX_ OUT4
7	—	PTE13	DISABLED		PTE13			FTM2_FLT0			
8	5	PTE5	DISABLED		PTE5	TCLK2	FTM2_QD_ PHA	FTM2_CH3	CAN0_TX	FXIO_D7	EWM_IN
9	6	PTE4	DISABLED		PTE4	BUSOUT	FTM2_QD_ PHB	FTM2_CH2	CAN0_RX	FXIO_D6	EWM_OUT_b

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
41	—	PTD9	ACMP1_IN5	ACMP1_IN5	PTD9	LPI2C1_SCL		FTM2_FLT3		FTM1_CH5	
42	—	PTD8	DISABLED		PTD8	LPI2C1_SDA		FTM2_FLT2		FTM1_CH4	
43	27	PTC17	ADC0_SE15	ADC0_SE15	PTC17	FTM1_FLT3		LPI2C1_SCLS			
44	28	PTC16	ADC0_SE14	ADC0_SE14	PTC16	FTM1_FLT2		LPI2C1_SDAS			
45	29	PTC15	ADC0_SE13/ ACMP2_IN4	ADC0_SE13/ ACMP2_IN4	PTC15	FTM1_CH3					
46	30	PTC14	ADC0_SE12/ ACMP2_IN5	ADC0_SE12/ ACMP2_IN5	PTC14	FTM1_CH2					
47	31	PTB3	ADC0_SE7	ADC0_SE7	PTB3	FTM1_CH1	LPSPI0_SIN	FTM1_QD_ PHA		TRGMUX_IN2	
48	32	PTB2	ADC0_SE6	ADC0_SE6	PTB2	FTM1_CH0	LPSPI0_SCK	FTM1_QD_ PHB		TRGMUX_IN3	
49	—	PTC13	DISABLED		PTC13	FTM3_CH7	FTM2_CH7				
50	—	PTC12	DISABLED		PTC12	FTM3_CH6	FTM2_CH6				
51	—	PTC11	DISABLED		PTC11	FTM3_CH5					
52	—	PTC10	DISABLED		PTC10	FTM3_CH4					
53	33	PTB1	ADC0_SE5	ADC0_SE5	PTB1	LPUART0_TX	LPSPI0_SOUT	TCLK0			
54	34	PTB0	ADC0_SE4	ADC0_SE4	PTB0	LPUART0_RX	LPSPI0_PCS0	LPTMR0_ ALT3	PWT_IN3		
55	35	PTC9	ADC2_SE15	ADC2_SE15	PTC9	LPUART1_TX	FTM1_FLT1			LPUART0_ RTS	
56	36	PTC8	ADC2_SE14	ADC2_SE14	PTC8	LPUART1_RX	FTM1_FLT0			LPUART0_ CTS	
57	37	PTA7	ADC0_SE3/ ACMP1_IN1	ADC0_SE3/ ACMP1_IN1	PTA7	FTM0_FLT2		RTC_CLKIN		LPUART1_ RTS	
58	38	PTA6	ADC0_SE2/ ACMP1_IN0	ADC0_SE2/ ACMP1_IN0	PTA6	FTM0_FLT1	LPSPI1_PCS1			LPUART1_ CTS	
59	39	PTE7	ADC2_SE2/ ACMP2_IN6	ADC2_SE2/ ACMP2_IN6	PTE7	FTM0_CH7	FTM3_FLT0				
60	40	VSS	VSS	VSS							
61	41	VDD	VDD	VDD							
62	—	PTA17	DISABLED		PTA17	FTM0_CH6	FTM3_FLT0	EWM_OUT_b			
63	—	PTB17	ADC2_SE3	ADC2_SE3	PTB17	FTM0_CH5	LPSPI1_PCS3				
64	—	PTB16	ADC1_SE15	ADC1_SE15	PTB16	FTM0_CH4	LPSPI1_SOUT				
65	—	PTB15	ADC1_SE14	ADC1_SE14	PTB15	FTM0_CH3	LPSPI1_SIN				
66	—	PTB14	ADC1_SE9	ADC1_SE9	PTB14	FTM0_CH2	LPSPI1_SCK				
67	42	PTB13	ADC1_SE8	ADC1_SE8	PTB13	FTM0_CH1	FTM3_FLT1				
68	43	PTB12	ADC1_SE7	ADC1_SE7	PTB12	FTM0_CH0	FTM3_FLT2				
69	44	PTD4	ADC1_SE6/ ACMP1_IN6	ADC1_SE6/ ACMP1_IN6	PTD4	FTM0_FLT3	FTM3_FLT3				
70	45	PTD3	NMI_b	ADC1_SE3	PTD3	FTM3_CH5	LPSPI1_PCS0	FXIO_D5		TRGMUX_IN4	NMI_b
71	46	PTD2	ADC1_SE2	ADC1_SE2	PTD2	FTM3_CH4	LPSPI1_SOUT	FXIO_D4		TRGMUX_IN5	
72	47	PTA3	ADC1_SE1	ADC1_SE1	PTA3	FTM3_CH1	LPI2C0_SCL	EWM_IN		LPUART0_TX	

Table 11. EWM Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EWM_IN	EWM_in	EWM input for safety status of external safety circuits. The polarity of EWM_IN is programmable using the EWM_CTRL[ASSIN] bit. The default polarity is active-low.	I
EWM_OUT_b	$\overline{\text{EWM\_out}}$	EWM reset out signal	O

4.3.3 Clock Modules

Table 12. OSC (in SCG) Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL	EXTAL	External clock/Oscillator input	I
XTAL	XTAL	Oscillator output	O

Table 13. RTC Oscillator (OSC32) Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL32	EXTAL32	32.768 kHz oscillator input	I
XTAL32	XTAL32	32.768 kHz oscillator output	O

4.3.4 Analog

Table 14. ADC*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
ADC*n*_SE[15:0]	AD[15:0]	Single-Ended Analog Channel Inputs	I
VREFH	V_{REFSH}	Voltage Reference Select High	I
VREFL	V_{REFSL}	Voltage Reference Select Low	I
VDDA	V_{DDA}	Analog Power Supply	I

Table 15. DAC0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
DAC0_OUT	—	DAC output	O

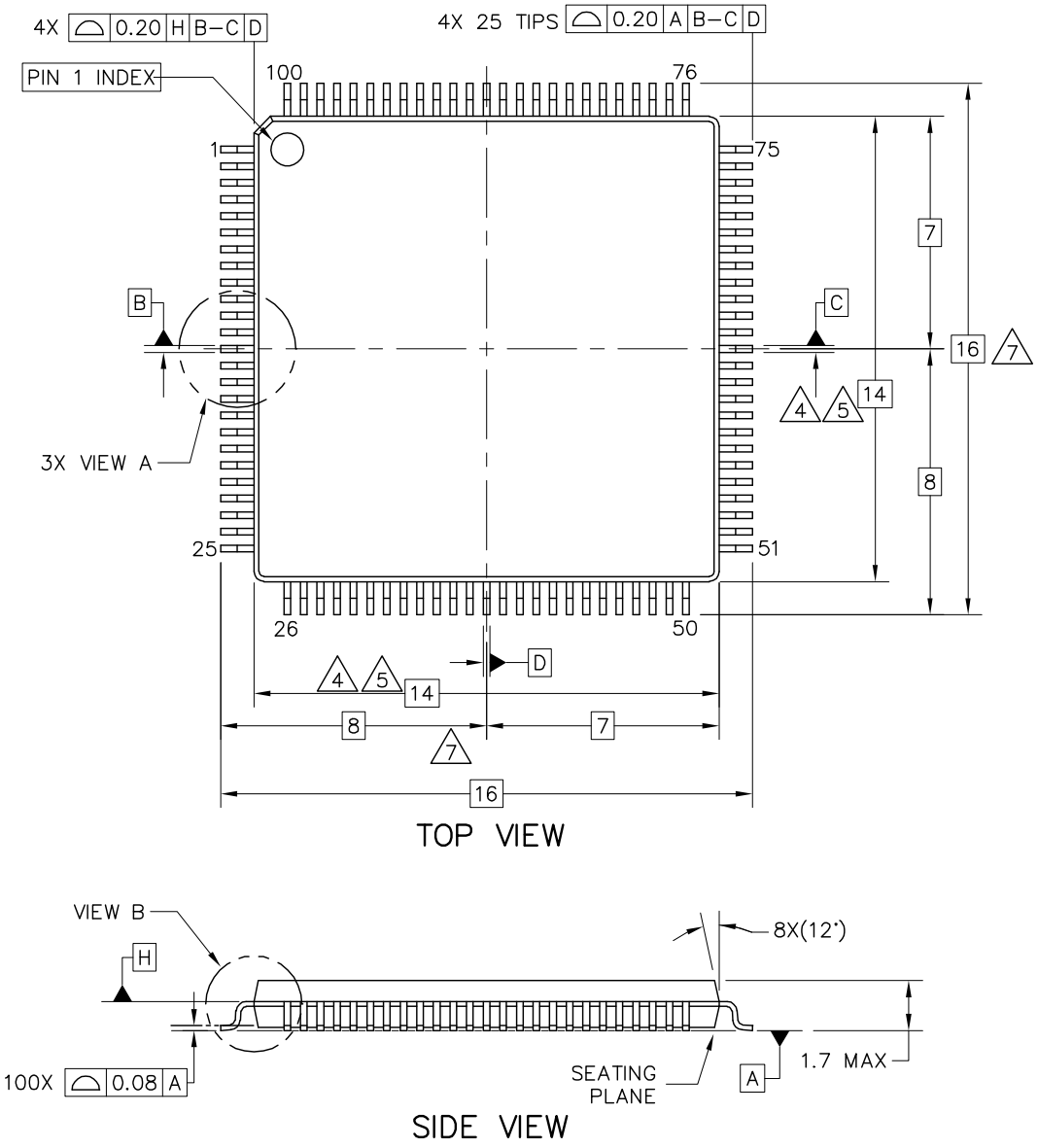

Figure 9. 100-pin LQFP package dimensions 1

Table 32. Power consumption operating behaviors (continued)

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max[1]	Units
		PLL	Running While(1) loop in Flash all peripheral clock enabled. Core@120MHz, bus @60MHz,flash @24MHz VDD=5V	25 ℃	—	39.87	40.50	
				105 ℃	—	46.03	51.64	
		IRC48M	Running CoreMark in Flash in **Compute Operation** mode. Core@48MHz, bus @48MHz, flash @24MHz , VDD=5V	25 ℃	—	14.02	14.65	
				105 ℃	—	19.76	25.37	
		IRC48M	Running CoreMark in Flash all peripheral clock disabled. Core@48MHz, bus @48MHz, flash @24MHz , VDD=5V	25 ℃	—	16.83	17.46	
				105 ℃	—	22.64	28.25	
		IRC48M	Running CoreMark in Flash, all peripheral clock enabled. Core@48MHz, bus @48MHz, flash @24MHz , VDD=5V	25 ℃	—	19.70	20.33	
				105 ℃	—	25.59	31.20	
		IRC48M	Running While(1) loop in Flash, all peripheral clock disabled. Core@48MHz, bus @48MHz, flash @24MHz , VDD=5V	25 ℃	—	17.22	17.85	
				105 ℃	—	23.23	28.84	
VLPR	I_{DD_VLPR}	IRC8M	Very Low Power Run Core Mark in Flash in **Compute Operation** mode. Core@4MHz, bus @4MHz, flash @1MHz, VDD=5V	25 ℃	—	1.52	1.63	mA
		IRC8M	Very Low Power Run Core Mark in Flash all peripheral clock disabled. Core@4MHz, bus @4MHz, flash @1MHz, VDD=5V	25 ℃	—	1.73	1.84	
		IRC8M	Very Low Power Run Core Mark in Flash all peripheral clock enabled. Core@4MHz, bus @4MHz, flash @1MHz, VDD=5V	25 ℃	—	1.95	2.06	
		IRC8M	Very Low Power Run While(1) loop in Flash all peripheral clock disabled. Core@4MHz, bus @4MHz, flash @1MHz, VDD=5V	25 ℃	—	1.77	1.88	
		IRC8M	Very Low Power Run While(1) loop in Flash all peripheral clock enabled. Core@4MHz, bus @4MHz, flash @1MHz, VDD=5V	25 ℃	—	1.96	2.07	
		IRC2M	Very Low Power Run While(1) loop in Flash all peripheral clock disabled.	25 ℃	—	1.19	1.30	

Table continues on the next page...

Table 34. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{FLASH}	Flash clock	—	25	MHz	
Normal RUN mode					
f_{SYS}	System and core clock	—	120	MHz	
f_{BUS}	Bus clock	—	60	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	50	MHz	
VLPR / VLPW mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR}	LPTMR clock	—	13	MHz	
$f_{FlexCAN}$	FlexCAN clock	—	4	MHz	

1. The frequency limitations in VLPR / VLPW mode here override any frequency specification listed in the timing specification for any other module.

5.3.2.2 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

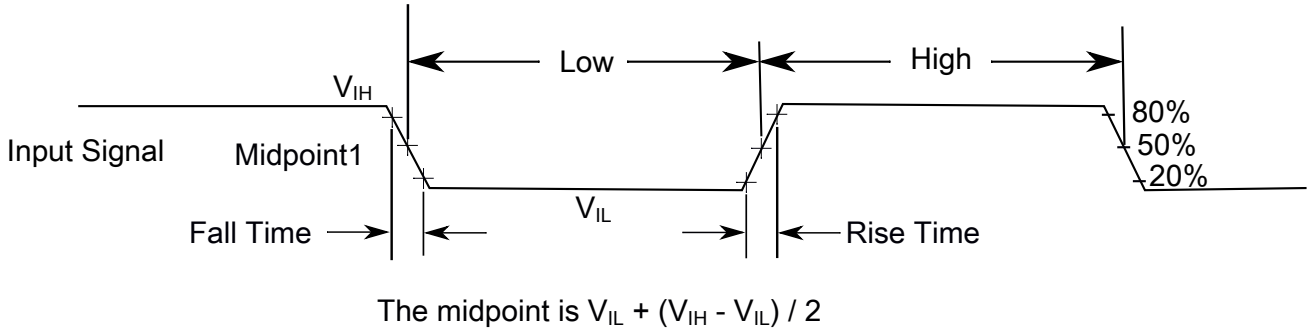

Figure 16. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L=30 pF loads
- Normal drive strength

5.3.3.2.1 Description

The tables in the following sections describe the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

5.3.3.2.2 Thermal characteristics for the 64-pin LQFP package

Table 39. Thermal characteristics for the 64-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	60	°C/W
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	42	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	49	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	36	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	24	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	12	°C/W
Thermal resistance, Junction to Package Top[6]	Natural Convection	Ψ_{JT}	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.3.3.2.3 Thermal characteristics for the 100-pin LQFP package

Table 40. Thermal characteristics for the 100-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	57	°C/W

Table continues on the next page...

Table 40. Thermal characteristics for the 100-pin LQFP package (continued)

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	44	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	47	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	38	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	30	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	14	°C/W
Thermal resistance, Junction to Package Top[6]	Natural Convection	ψ_{JT}	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.3.3.2.4 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

Table 41. External Oscillator electrical specifications (OSC32) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{IH}	Input high voltage — EXTAL32 pin in external clock mode	0.7 x V_{DD}	—	V_{DD}	V	
V_{IL}	Input low voltage — EXTAL32 pin in external clock mode	V_{SS}	—	0.35 x V_{DD}	V	
C_1	EXTAL32 load capacitance	—	—	—		2
C_2	XTAL32 load capacitance	—	—	—		2
R_F	Feedback resistor	—	—	—	MΩ	
R_S	Series resistor	—	—	—	MΩ	
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)	—	0.6	—	V	3

1. Measured at V_{DD} = 5 V, Temperature = 25 °C. The current consumption is according to the crystal or resonator, loading capacitance.
2. C1 and C2 must be provided by external capacitors and their load capacitance depends on the crystal or resonator manufacturers' recommendation. Please check the crystal datasheet for the recommended values.
3. The EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

Table 42. External Oscillator electrical specifications (OSC)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	—	5.5	V	
I_{DDOSC}	Supply current — low-gain mode (low-power mode) (HGO=0)					1
	4 MHz	—	200	—	µA	
	8 MHz	—	300	—	µA	
	16 MHz	—	1.2	—	mA	
	24 MHz	—	1.6	—	mA	
	32 MHz	—	2	—	mA	
	40 MHz	—	2.6	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	4 MHz	—	1	—	mA	
	8 MHz	—	1.2	—	mA	
	16 MHz	—	3.5	—	mA	
	24 MHz	—	5	—	mA	
	32 MHz	—	5.5	—	mA	
	40 MHz	—	6	—	mA	
g_{mXOSC}	Fast external crystal oscillator transconductance					
	32 kHz, Low Frequency Range, High Gain (32 kHz)	15	—	45	µA / V	
	High Frequency Range 1 (4-8 MHz)	2.2	—	9.7	mA / V	
	High Frequency Range 2 (8-40 MHz)	16		37	mA / V	
V_{EXTAL}	EXTAL input voltage — external clock mode	0	—	V_{DD}	V	

Table continues on the next page...

Table 50. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	385	1700	µs	
$t_{eewr16b48k}$	• 48 KB EEPROM backup	—	430	1850	µs	
$t_{eewr16b64k}$	• 64 KB EEPROM backup	—	475	2000	µs	
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	1500	µs	
	32-bit write to FlexRAM execution time:					
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	630	2000	µs	
$t_{eewr32b48k}$	• 48 KB EEPROM backup	—	720	2125	µs	
$t_{eewr32b64k}$	• 64 KB EEPROM backup	—	810	2250	µs	

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

5.4.3.1.3 Flash high voltage current behaviors

Table 51. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	3.5	7.5	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

5.4.3.1.4 Reliability specifications

Table 52. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
$n_{nvmcycee}$	Cycling endurance for EEPROM backup	20 K	50 K	—	cycles	2

Table continues on the next page...

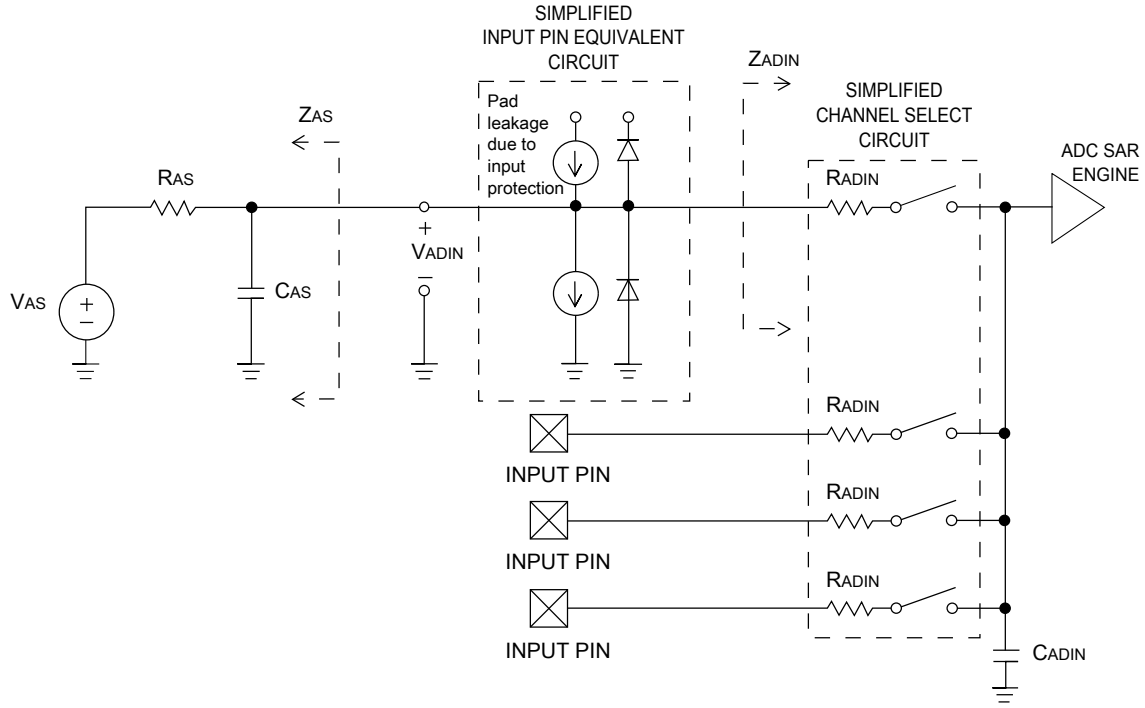

Figure 19. ADC input impedance equivalency diagram

5.4.5.1.2 12-bit ADC electrical characteristics

NOTE

All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

For ADC signals adjacent to VDD/VSS or the XTAL pins some degradation in the ADC performance may be observed.

NOTE

All values guarantee the performance of the ADC for the multiple ADC input channel pins. When using the ADC to monitor the internal analogue parameters, please assume minor degradation.

Table 54. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max. [3]	Unit	Notes
I_{DDA_ADC}	Supply current at 2.7 to 5.5 V		621	658 µA @ 5 V	696	mA	4

Table continues on the next page...

Table 55. Comparator with 8-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ. [1]	Max.	Unit
	within ambient temperature range	—	48	133	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	within ambient temperature range	—	33	80	
I_{DAC8b}	8-bit DAC current adder (enabled)	—	10	16	µA
INL	8-bit DAC integral non-linearity	–0.6	—	0.5	LSB[5]
DNL	8-bit DAC differential non-linearity	–0.5	—	0.5	LSB

1. Typical values assumed at VDDA = 5.0 V, Temp = 25 °C, unless otherwise stated.
2. Difference at input > 200mV
3. Applied ± (100 mV + Hyst) around switch point
4. Applied ± (30 mV + 2 × Hyst) around switch point
5. 1 LSB = $V_{reference}/256$

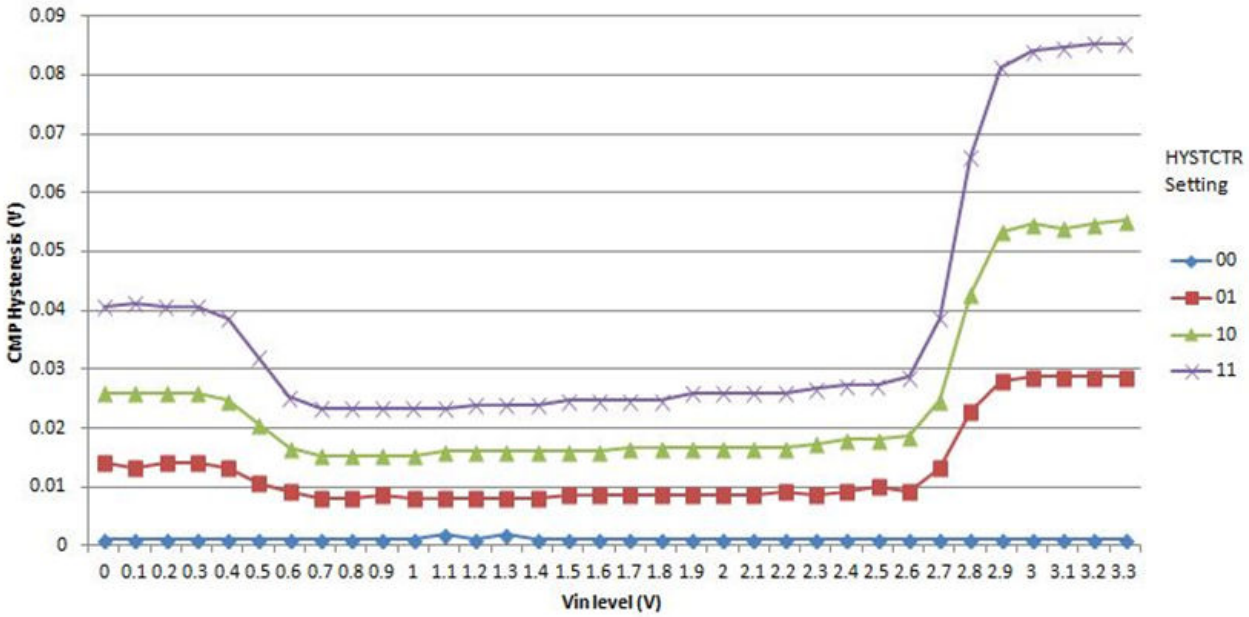

Figure 20. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

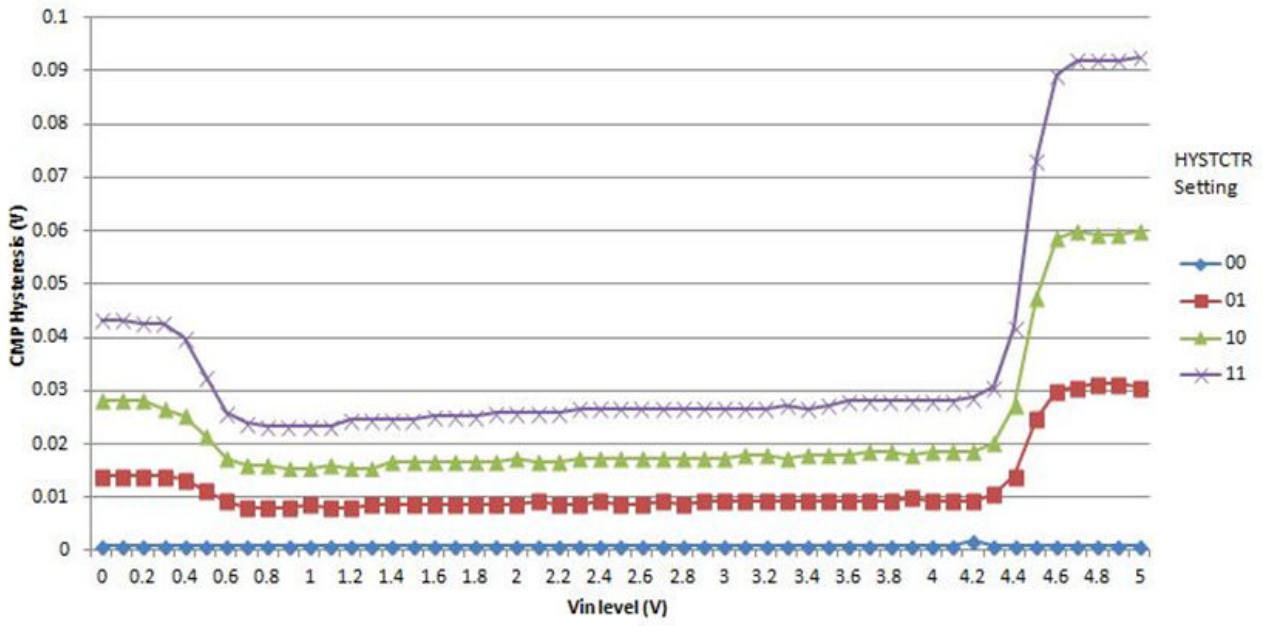

Figure 23. Typical hysteresis vs. Vin level (VDD = 5 V, PMODE = 1)

5.4.5.3 12-bit DAC electrical characteristics

5.4.5.3.1 12-bit DAC operating requirements

Table 56. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	2.7	5.5	V	
V_{DACR}	Reference voltage	2.7	5.5	V	1
C_L	Output load capacitance	20	100	pF	2
I_L	Output load current	—	1	mA	3

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance can improve the bandwidth performance of the DAC.
3. Output range is from ground + 0.2 to V_{DACR} - 0.2

5.4.5.3.2 12-bit DAC operating behaviors

Table 57. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	330	µA	
I_{DDA_DACHP}	Supply current — high-power mode	—	—	1200	µA	

Table continues on the next page...

5.4.6.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.

Table 58. LPSPI master mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} = LPSPI peripheral clock
2. $t_{periph} = 1/f_{periph}$

NOTE

High drive pin should be used for fast bit rate.

5.4.7.1 SWD electricals

Table 61. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
V_{DDA}	Operating voltage	2.7	5.5	V
S1	SWD_CLK frequency of operation	0	25	MHz
S2	SWD_CLK cycle period	1/S1	—	ns
S3	SWD_CLK clock pulse width	15	—	ns
S4	SWD_CLK rise and fall times	—	3	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	8	—	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	1.4	—	ns
S11	SWD_CLK high to SWD_DIO data valid	—	25	ns
S12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

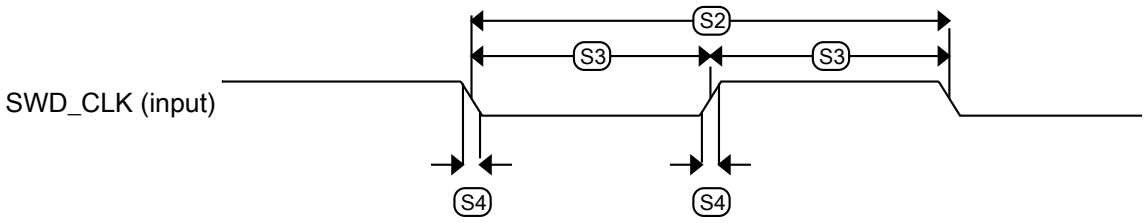

Figure 28. Serial wire clock input timing

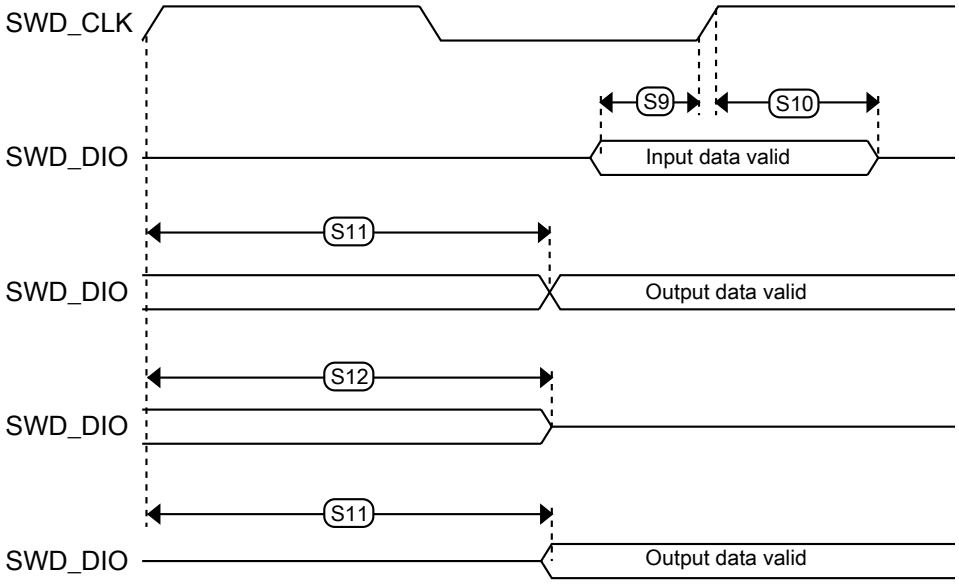

Figure 29. Serial wire data timing