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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	FlexIO, I²C, SPI, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	58
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	68K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke14f512vlh16

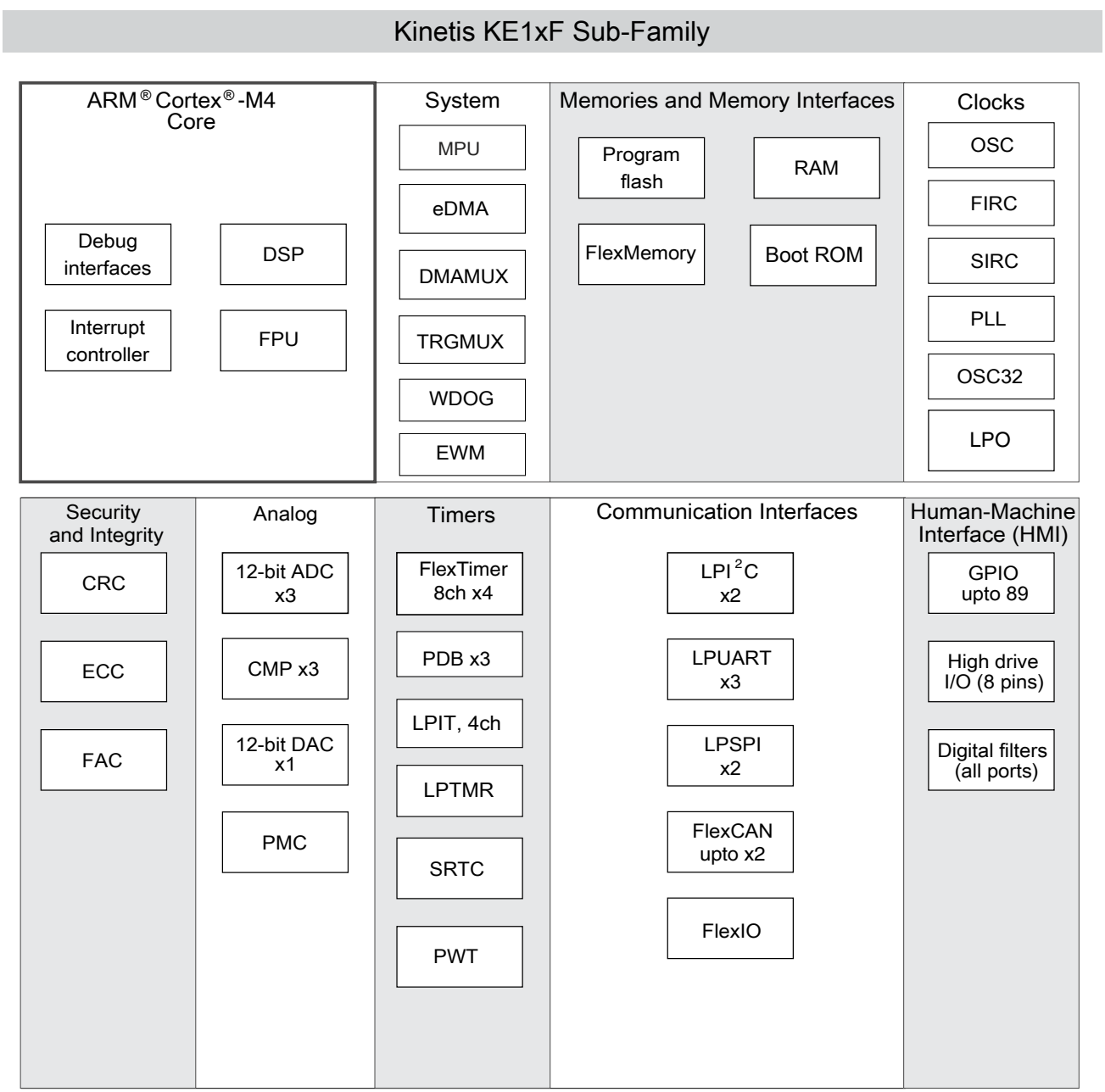


Figure 1. Functional block diagram

2.1.1 ARM Cortex-M4 core

The ARM Cortex-M4 is the member of the Cortex M Series of processors targeting microcontroller cores focused on very cost sensitive, deterministic, interrupt driven environments. The Cortex M4 processor is based on the ARMv7 Architecture and Thumb®-2 ISA and is upward compatible with the Cortex M3, Cortex M1, and Cortex M0 architectures. Cortex M4 improvements include an ARMv7 Thumb-2 DSP (ported from the ARMv7-A/R profile architectures) providing 32-bit instructions with SIMD (single instruction multiple data) DSP style multiply-accumulates and saturating arithmetic.

2.1.2 NVIC

The Nested Vectored Interrupt Controller supports nested interrupts and 16 priority levels for interrupts. In the NVIC, each source in the IPR registers contains 4 bits. It also differs in number of interrupt sources and supports 240 interrupt vectors.

The Cortex-M family uses a number of methods to improve interrupt latency . It also can be used to wake the MCU core from Wait and VLPW modes.

2.1.3 AWIC

The asynchronous wake-up interrupt controller (AWIC) is used to detect asynchronous wake-up events in Stop mode and signal to clock control logic to resume system clocking. After clock restarts, the NVIC observes the pending interrupt and performs the normal interrupt or event processing. The AWIC can be used to wake MCU core from Partial Stop, Stop and VLPS modes.

Wake-up sources for this SoC are listed as below:

Table 2. AWIC Stop and VLPS Wake-up Sources

Wake-up source	Description
Available system resets	RESET pin, WDOG, JTAG , loss of clock(LOC) reset and loss of lock (LOL) reset
Pin interrupts	Port Control Module - Any enabled pin interrupt is capable of waking the system
ADCx	ADCx is optional functional with clock source from SIRC or OSC
CMPx	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPI2C	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPUART	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPSPI	Functional in Stop/VLPS modes with clock source from SIRC or OSC

Table continues on the next page...

- Transmit and receive baud rate can operate asynchronous to the bus clock and can be configured independently of the bus clock frequency, support operation in Stop mode
- Interrupt, DMA or polled operation
- Hardware parity generation and checking
- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods
  - Idle line wakeup
  - Address mark wakeup
  - Receive data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity

2.2.12 LPSPI

This device contains two LPSPI modules. The LPSPI is a low power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus as a master and/or a slave. The LPSPI can continue operating in stop modes provided an appropriate clock is available and is designed for low CPU overhead with DMA offloading of FIFO register accesses.

The LPSPI modules have the following features:

- Command/transmit FIFO of 4 words
- Receive FIFO of 4 words
- Host request input can be used to control the start time of an SPI bus transfer

2.2.13 FlexCAN

This device contains two FlexCAN modules. The FlexCAN module is a communication controller implementing the CAN protocol according to the ISO 11898-1 standard and CAN 2.0 B protocol specifications.

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
41	—	PTD9	ACMP1_IN5	ACMP1_IN5	PTD9	LPI2C1_SCL		FTM2_FLT3		FTM1_CH5	
42	—	PTD8	DISABLED		PTD8	LPI2C1_SDA		FTM2_FLT2		FTM1_CH4	
43	27	PTC17	ADC0_SE15	ADC0_SE15	PTC17	FTM1_FLT3		LPI2C1_SCLS			
44	28	PTC16	ADC0_SE14	ADC0_SE14	PTC16	FTM1_FLT2		LPI2C1_SDAS			
45	29	PTC15	ADC0_SE13/ ACMP2_IN4	ADC0_SE13/ ACMP2_IN4	PTC15	FTM1_CH3					
46	30	PTC14	ADC0_SE12/ ACMP2_IN5	ADC0_SE12/ ACMP2_IN5	PTC14	FTM1_CH2					
47	31	PTB3	ADC0_SE7	ADC0_SE7	PTB3	FTM1_CH1	LPSPI0_SIN	FTM1_QD_ PHA		TRGMUX_IN2	
48	32	PTB2	ADC0_SE6	ADC0_SE6	PTB2	FTM1_CH0	LPSPI0_SCK	FTM1_QD_ PHB		TRGMUX_IN3	
49	—	PTC13	DISABLED		PTC13	FTM3_CH7	FTM2_CH7				
50	—	PTC12	DISABLED		PTC12	FTM3_CH6	FTM2_CH6				
51	—	PTC11	DISABLED		PTC11	FTM3_CH5					
52	—	PTC10	DISABLED		PTC10	FTM3_CH4					
53	33	PTB1	ADC0_SE5	ADC0_SE5	PTB1	LPUART0_TX	LPSPI0_SOUT	TCLK0			
54	34	PTB0	ADC0_SE4	ADC0_SE4	PTB0	LPUART0_RX	LPSPI0_PCS0	LPTMR0_ ALT3	PWT_IN3		
55	35	PTC9	ADC2_SE15	ADC2_SE15	PTC9	LPUART1_TX	FTM1_FLT1			LPUART0_ RTS	
56	36	PTC8	ADC2_SE14	ADC2_SE14	PTC8	LPUART1_RX	FTM1_FLT0			LPUART0_ CTS	
57	37	PTA7	ADC0_SE3/ ACMP1_IN1	ADC0_SE3/ ACMP1_IN1	PTA7	FTM0_FLT2		RTC_CLKIN		LPUART1_ RTS	
58	38	PTA6	ADC0_SE2/ ACMP1_IN0	ADC0_SE2/ ACMP1_IN0	PTA6	FTM0_FLT1	LPSPI1_PCS1			LPUART1_ CTS	
59	39	PTE7	ADC2_SE2/ ACMP2_IN6	ADC2_SE2/ ACMP2_IN6	PTE7	FTM0_CH7	FTM3_FLT0				
60	40	VSS	VSS	VSS							
61	41	VDD	VDD	VDD							
62	—	PTA17	DISABLED		PTA17	FTM0_CH6	FTM3_FLT0	EWM_OUT_b			
63	—	PTB17	ADC2_SE3	ADC2_SE3	PTB17	FTM0_CH5	LPSPI1_PCS3				
64	—	PTB16	ADC1_SE15	ADC1_SE15	PTB16	FTM0_CH4	LPSPI1_SOUT				
65	—	PTB15	ADC1_SE14	ADC1_SE14	PTB15	FTM0_CH3	LPSPI1_SIN				
66	—	PTB14	ADC1_SE9	ADC1_SE9	PTB14	FTM0_CH2	LPSPI1_SCK				
67	42	PTB13	ADC1_SE8	ADC1_SE8	PTB13	FTM0_CH1	FTM3_FLT1				
68	43	PTB12	ADC1_SE7	ADC1_SE7	PTB12	FTM0_CH0	FTM3_FLT2				
69	44	PTD4	ADC1_SE6/ ACMP1_IN6	ADC1_SE6/ ACMP1_IN6	PTD4	FTM0_FLT3	FTM3_FLT3				
70	45	PTD3	NMI_b	ADC1_SE3	PTD3	FTM3_CH5	LPSPI1_PCS0	FXIO_D5		TRGMUX_IN4	NMI_b
71	46	PTD2	ADC1_SE2	ADC1_SE2	PTD2	FTM3_CH4	LPSPI1_SOUT	FXIO_D4		TRGMUX_IN5	
72	47	PTA3	ADC1_SE1	ADC1_SE1	PTA3	FTM3_CH1	LPI2C0_SCL	EWM_IN		LPUART0_TX	

Table 16. ACMP*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
ACMP*n*_IN[6:0]	IN[6:0]	Analog voltage inputs	I
ACMP*n*_OUT	CMPO	Comparator output	O

4.3.5 Timer Modules

Table 17. LPTMR0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR0_ALT[3:1]	LPTMR_ALT*n*	Pulse Counter Input pin	I

Table 18. RTC Signal Descriptions

Chip signal name	Module signal name	Description	I/O
RTC_CLKOUT	RTC_CLKOUT	1 Hz square-wave output or 32 kHz clock	O

Table 19. FTM*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
FTM*n*_CH[7:0]	CHn	FTM channel (n), where n can be 7-0	I/O
FTM*n*_FLT[3:0]	FAULTj	Fault input (j), where j can be 3-0	I
TCLK[2:0]	EXTCLK	External clock. FTM external clock can be selected to drive the FTM counter.	I

4.3.6 Communication Interfaces

Table 20. CAN*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
CAN*n*_RX	CAN Rx	CAN Receive Pin	I
CAN*n*_TX	CAN Tx	CAN Transmit Pin	O

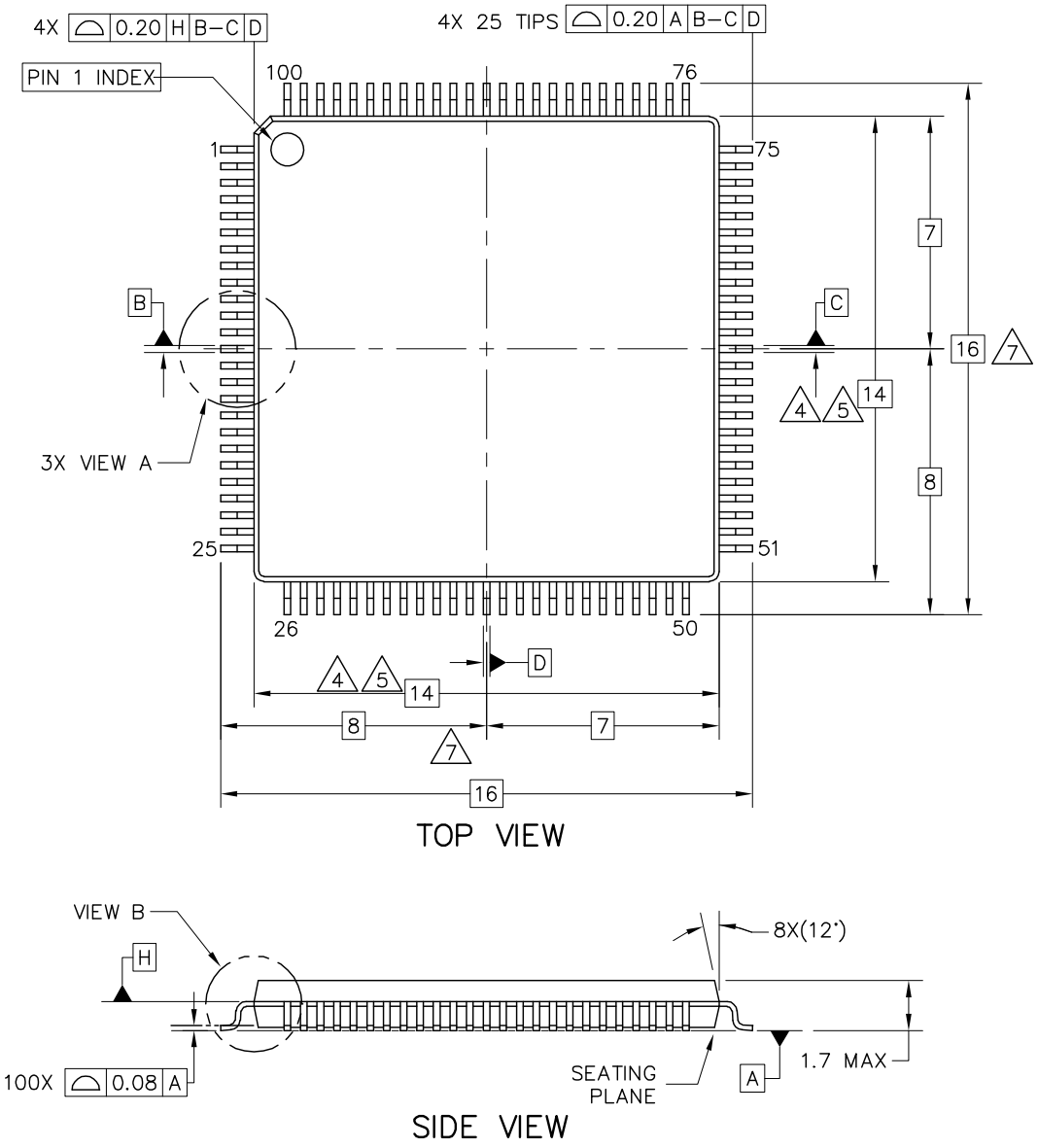
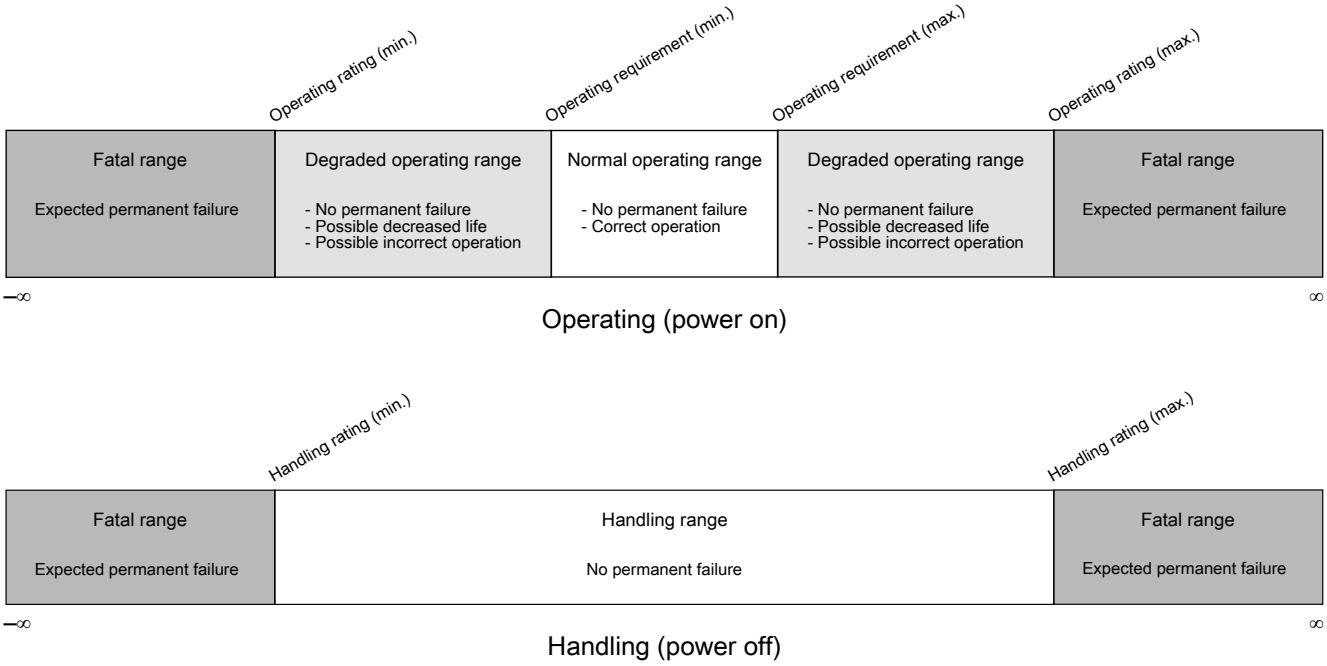


Figure 9. 100-pin LQFP package dimensions 1

5.1.4 Relationship between ratings and operating requirements



5.1.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

5.2 Ratings

5.2.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

Table 28. DC electrical specifications (continued)

Symbol	Parameter	Value			Unit	Notes
		Min	Typ	Max		
V_{il}	Input Buffer Low Voltage @ V_{DD} = 3.3 V	V_{SS} – 0.3	—	0.3 × V_{DD}	V	
	@ V_{DD} = 5.0 V	V_{SS} – 0.3	—	0.35 × V_{DD}	V	
V_{hys}	Input Buffer Hysteresis	0.06 × V_{DD}	—	—	V	
Ioh_5	Normal drive I/O current source capability measured when pad = (V_{DDE} – 0.8 V) @ V_{DD} = 3.3 V	2.8	—	—	mA	
	@ V_{DD} = 5.0 V	4.8	—	—	mA	
Iol_5	Normal drive I/O current sink capability measured when pad = 0.8 V @ V_{DD} = 3.3 V	2.4	—	—	mA	
	@ V_{DD} = 5.0 V	4.4	—	—	mA	
Ioh_20	High drive I/O current source capability measured when pad = (V_{DDE} – 0.8 V)[2] @ V_{DD} = 3.3 V	10.8	—	—	mA	
	@ V_{DD} = 5.0 V	18.5	—	—	mA [3]	
Iol_20	High drive I/O current sink capability measured when pad = 0.8 V[4] @ V_{DD} = 3.3 V	10.1	—	—	mA	
	@ V_{DD} = 5.0 V	18.5	—	—	mA [3]	
I_leak	Hi-Z (Off state) leakage current (per pin)	—	—	300	nA	5, 6
V_{OH}	Output high voltage					7
	Normal drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –2.8 mA)	V_{DD} – 0.8	—	—	V	
	Normal drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –4.8 mA)	V_{DD} – 0.8	—	—	V	
	High drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –10.8 mA)	V_{DD} – 0.8	—	—	V	
	High drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –18.5 mA)	V_{DD} – 0.8	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage					7
	Normal drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –2.8 mA)	—	—	0.8	V	
	Normal drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –4.8 mA)	—	—	0.8	V	
	High drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –10.8 mA)	—	—	0.8	V	
	High drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –18.5 mA)	—	—	0.8	V	

Table continues on the next page...

5.3.1.3 Voltage regulator electrical characteristics

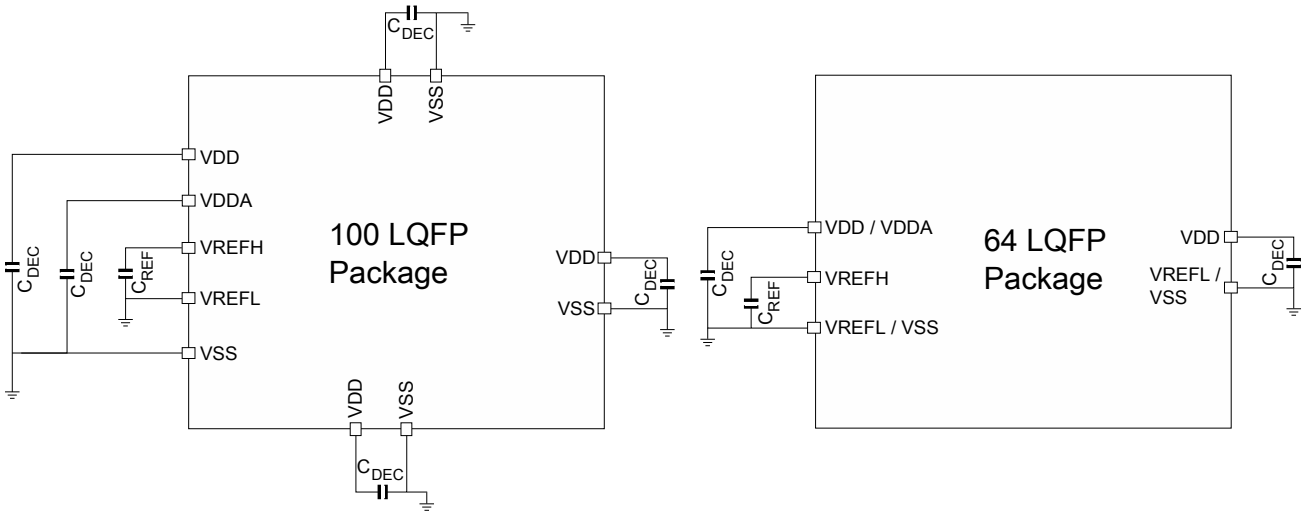


Figure 13. Pinout decoupling

Table 29. Voltage regulator electrical characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
C_{REF} [1, 2]	ADC reference high decoupling capacitance	—	100	—	nF
C_{DEC} [2, 3]	Recommended decoupling capacitance	—	100	—	nF

1. For improved ADC performance it is recommended to use 1 nF X7R/C0G and 10 nF X7R ceramics in parallel.
2. The capacitors should be placed as close as possible to the VREFH/VREFL pins or corresponding V_{DD}/V_{SS} pins.
3. The requirement and value of of C_{DEC} will be decided by the device application requirement.

NOTE

For 64 LQFP, the external decoupling capacitor C_{DEC} must be added, and the minimum value is 100 nF.

5.3.1.4 LVR, LVD and POR operating requirements

Table 30. V_{DD} supply LVR, LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and Falling V_{DD} POR detect voltage	1.1	1.6	2.0	V	
V_{LVRX}	LVRX falling threshold (RUN, HSRUN, and STOP modes)	2.50	2.58	2.7	V	
V_{LVRX_HYST}	LVRX hysteresis	—	45	—	mV	1
V_{LVRX_LP}	LVRX falling threshold (VLPS/VLPR modes)	1.97	2.12	2.44	V	
$V_{LVRX\_LP\_HYST}$	LVRX hysteresis (VLPS/VLPR modes)	—	40	—	mV	
V_{LVD}	Falling low-voltage detect threshold	2.8	2.88	3	V	

Table continues on the next page...

Table 32. Power consumption operating behaviors (continued)

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max[1]	Units
			Core@2MHz, bus @2MHz, flash @1MHz, VDD=5V					
		IRC2M	Very Low Power Run While(1) loop in Flash all peripheral clock enabled. Core@2MHz, bus @2MHz, flash @1MHz, VDD=5V	25 °C	—	1.28	1.39	
WAIT	I_{DD_WAIT}	PLL	core disabled, system@120MHz, bus @60MHz, flash disabled (**flash doze enabled**), VDD=5 V, all peripheral clocks disabled	25 °C	—	14.13	14.78	mA
		IRC48M	core disabled, system@48 MHz, bus @48MHz, flash disabled (**flash doze enabled**), VDD=5 V, all peripheral clocks disabled	25 °C	—	8.50	9.15	
VLPW	I_{DD_VLPW}	IRC8M	Very Low Power Wait current, core disabled system@4MHz, bus@4Mhz and flash@1MHz, all peripheral clocks disabled, VDD=5V	25 °C	—	0.84	0.94	mA
		IRC2M	Very Low Power Wait current, core disabled system@2MHz, bus@2Mhz and flash@1MHz, all peripheral clocks disabled, VDD=5V	25 °C	—	1.08	1.18	
STOP	I_{DD_STOP}	-	Stop mode current, VDD=5V, bias disabled [2]	25 °C and blew	—	175	484	µA
				50 °C	—	438	1014	
				85 °C	—	1433	2864	
				105 °C	—	2860	5263	
STOP	I_{DD_STOP}	-	Stop mode current, VDD=5V, bias enabled [2]	25 °C and blew	—	92	299	µA
				50 °C	—	211	530	
				85 °C	—	671	1397	
				105 °C	—	1287	2502	
VLPS	I_{DD_VLPS}	-	Very Low Power Stop current, VDD=5V, bias disabled [2]	25 °C and blew	—	175	483	µA
				50 °C	—	424	998	
				85 °C	—	1367	2792	
				105 °C	—	2864	5258	
VLPS	I_{DD_VLPS}	-	Very Low Power Stop current, VDD=5V, bias enabled [2]	25 °C and blew	—	91	298	µA
				50 °C	—	208	525	
				85 °C	—	656	1378	
				105 °C	—	1305	2514	

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

- T_T = thermocouple temperature on top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

5.4 Peripheral operating requirements and behaviors

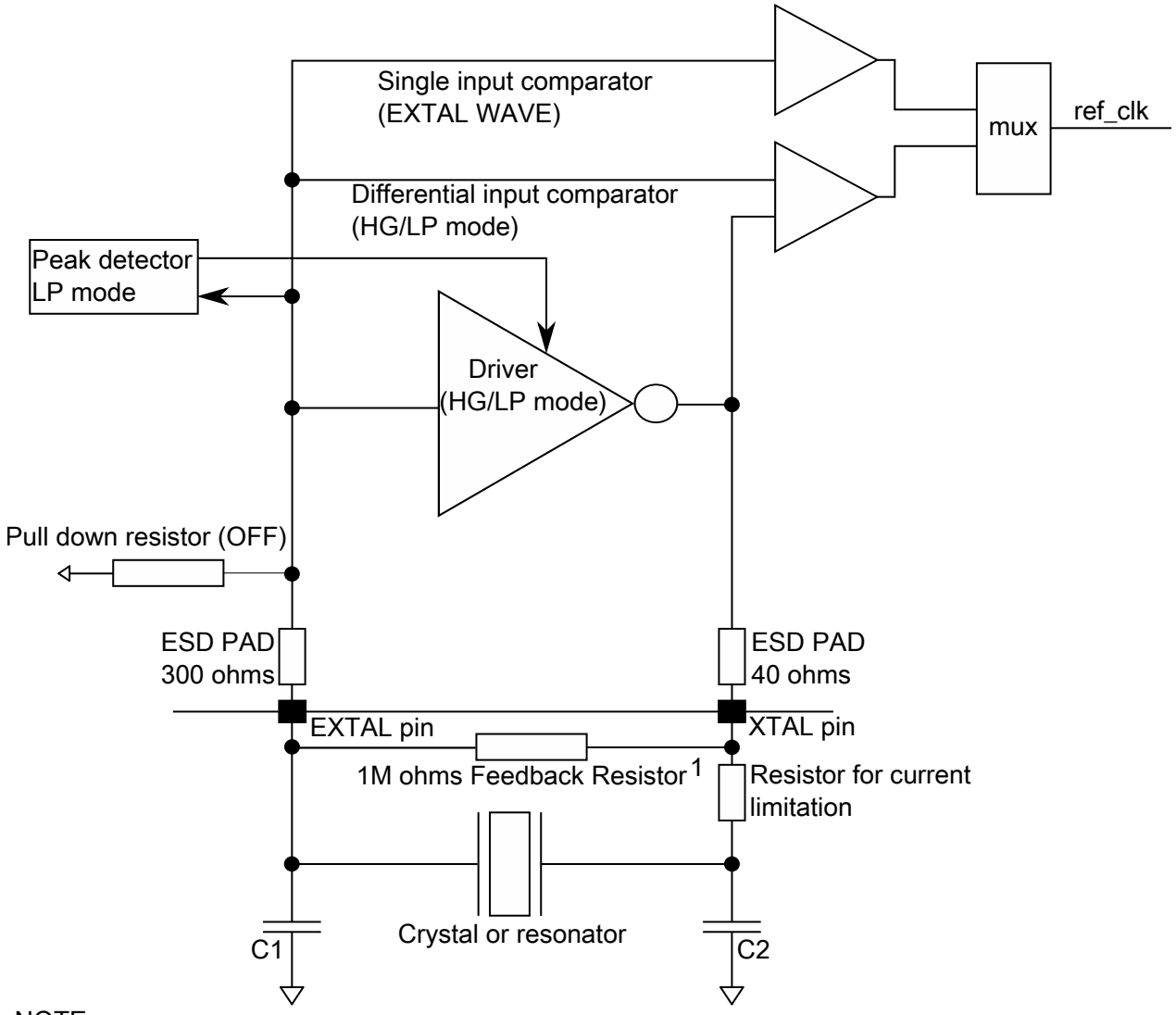
5.4.1 System modules

There are no specifications necessary for the device's system modules.

5.4.2 Clock interface modules

5.4.2.1 Oscillator electrical specifications

5.4.2.1.1 External Oscillator electrical specifications



NOTE:

1. 1M Feedback resistor is needed only for HG mode.

Figure 18. Oscillator connections scheme (OSC)

NOTE

Data values in the following "External Oscillator electrical specifications" tables are from simulation.

Table 41. External Oscillator electrical specifications (OSC32)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	—	5.5	V	
I_{DDOSC}	Supply current	—	25	—	µA	1
g_{mXOSC}	Oscillator transconductance	6	—	9	µA/V	
V_{EXTAL}	EXTAL32 input voltage — external clock mode	0	—	3.6	V	

Table continues on the next page...

Table 41. External Oscillator electrical specifications (OSC32) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{IH}	Input high voltage — EXTAL32 pin in external clock mode	0.7 x V_{DD}	—	V_{DD}	V	
V_{IL}	Input low voltage — EXTAL32 pin in external clock mode	V_{SS}	—	0.35 x V_{DD}	V	
C_1	EXTAL32 load capacitance	—	—	—		2
C_2	XTAL32 load capacitance	—	—	—		2
R_F	Feedback resistor	—	—	—	MΩ	
R_S	Series resistor	—	—	—	MΩ	
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)	—	0.6	—	V	3

1. Measured at V_{DD} = 5 V, Temperature = 25 °C. The current consumption is according to the crystal or resonator, loading capacitance.
2. C1 and C2 must be provided by external capacitors and their load capacitance depends on the crystal or resonator manufacturers' recommendation. Please check the crystal datasheet for the recommended values.
3. The EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

Table 42. External Oscillator electrical specifications (OSC)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	—	5.5	V	
I_{DDOSC}	Supply current — low-gain mode (low-power mode) (HGO=0)					1
	4 MHz	—	200	—	µA	
	8 MHz	—	300	—	µA	
	16 MHz	—	1.2	—	mA	
	24 MHz	—	1.6	—	mA	
	32 MHz	—	2	—	mA	
	40 MHz	—	2.6	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	4 MHz	—	1	—	mA	
	8 MHz	—	1.2	—	mA	
	16 MHz	—	3.5	—	mA	
	24 MHz	—	5	—	mA	
	32 MHz	—	5.5	—	mA	
	40 MHz	—	6	—	mA	
g_{mXOSC}	Fast external crystal oscillator transconductance					
	32 kHz, Low Frequency Range, High Gain (32 kHz)	15	—	45	µA / V	
	High Frequency Range 1 (4-8 MHz)	2.2	—	9.7	mA / V	
	High Frequency Range 2 (8-40 MHz)	16		37	mA / V	
V_{EXTAL}	EXTAL input voltage — external clock mode	0	—	V_{DD}	V	

Table continues on the next page...

Table 44. External Oscillator frequency specifications (OSC)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — Low Frequency, High Gain Mode	32	—	40	kHz	
f_{osc_me}	Oscillator crystal or resonator frequency — Medium Frequency	1	—	8	MHz	
f_{osc_hi}	Oscillator crystal or resonator frequency — High Frequency	8	—	32		
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz Low Frequency, High-Gain Mode	—	500	—	ms	1
	Crystal startup time — 8 MHz High Frequency, Low-Power Mode	—	1.5	—		
	Crystal startup time — 8 MHz High Frequency, High-Gain Mode	—	2.5	—		
	Crystal startup time — 40 MHz High Frequency, Low-Power Mode	—	2	—		
	Crystal startup time — 40 MHz High Frequency, High-Gain Mode	—	2.5	—		

1. The start-up measured after 4096 cycles. Proper PC board layout procedures must be followed to achieve specifications.

5.4.2.2 System Clock Generation (SCG) specifications

5.4.2.2.1 Fast internal RC Oscillator (FIRC) electrical specifications

Table 45. Fast internal RC Oscillator electrical specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{FIRC}	Fast internal reference frequency Trim range = 00 range = 01 (Note: 52/56 MHz are not trimmed) range = 10 (Note: 52/56 MHz are not trimmed) Trim range = 11	—	48 52 56 60	—	MHz
I_{VDD}	Supply current	—	400	500	µA
$F_{Untrimmed}$	IRC frequency (untrimmed)	F_{IRC}× (1-0.3)	—	F_{IRC}× (1+0.3)	MHz
ΔF_{OL}	Open loop total deviation of IRC frequency over voltage and temperature[1]				
	Regulator enable	—	±0.5	±1	$\%F_{FIRC}$
$T_{Startup}$	Startup time		—	3	µs[2]
T_{JIT}	Period jitter (RMS)	—	35	150	ps

Table 54. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max. [3]	Unit	Notes
	Sample Time		275	—	Refer to the device's *Reference Manual*	ns	
TUE	Total unadjusted error at 2.7 to 5.5 V		—	±4.5	±6.56	LSB[5]	6
DNL	Differential non-linearity at 2.7 to 5.5 V		—	±0.8	±1.07	LSB[5]	6
INL	Integral non-linearity at 2.7 to 5.5 V		—	±1.4	±3.95	LSB[5]	6
E_{FS}	Full-scale error at 2.7 to 5.5 V		—	–2	-3.40	LSB[5]	V_{ADIN} = V_{DDA}[6]
E_{ZS}	Zero-scale error at 2.7 to 5.5 V		—	–2.7	-4.14	LSB[5]	
E_Q	Quantization error at 2.7 to 5.5 V		—	—	±0.5	LSB[5]	
ENOB	Effective number of bits at 2.7 to 5.5 V		—	11.3	—	bits	7
SINAD	Signal-to-noise plus distortion at 2.7 to 5.5 V	See ENOB	—	70	—	dB	SINAD = 6.02 × ENOB + 1.76
E_{IL}	Input leakage error at 2.7 to 5.5 V		I_{In} × R_{AS}			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
V_{TEMP_S}	Temperature sensor slope at 2.7 to 5.5 V	Across the full temperature range of the device	1.492	1.564	1.636	mV/°C	8, 9
V_{TEMP25}	Temperatue sensor voltage at 2.7 to 5.5 V	25 °C	730	740.5	751	mV	8, 9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 48 MHz unless otherwise stated.
3. These values are based on characterization but not covered by test limits in production.
4. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
5. 1 LSB = (V_{REFH} - V_{REFL})/2^N
6. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
7. Input data is 100 Hz sine wave. ADC conversion clock < 40 MHz.
8. ADC conversion clock < 3 MHz
9. The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031 for more detailed application information of the temperature sensor.

Table 55. Comparator with 8-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ. [1]	Max.	Unit
	within ambient temperature range	—	48	133	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	within ambient temperature range	—	33	80	
I_{DAC8b}	8-bit DAC current adder (enabled)	—	10	16	µA
INL	8-bit DAC integral non-linearity	–0.6	—	0.5	LSB[5]
DNL	8-bit DAC differential non-linearity	–0.5	—	0.5	LSB

1. Typical values assumed at VDDA = 5.0 V, Temp = 25 °C, unless otherwise stated.
2. Difference at input > 200mV
3. Applied ± (100 mV + Hyst) around switch point
4. Applied ± (30 mV + 2 × Hyst) around switch point
5. 1 LSB = $V_{reference}/256$

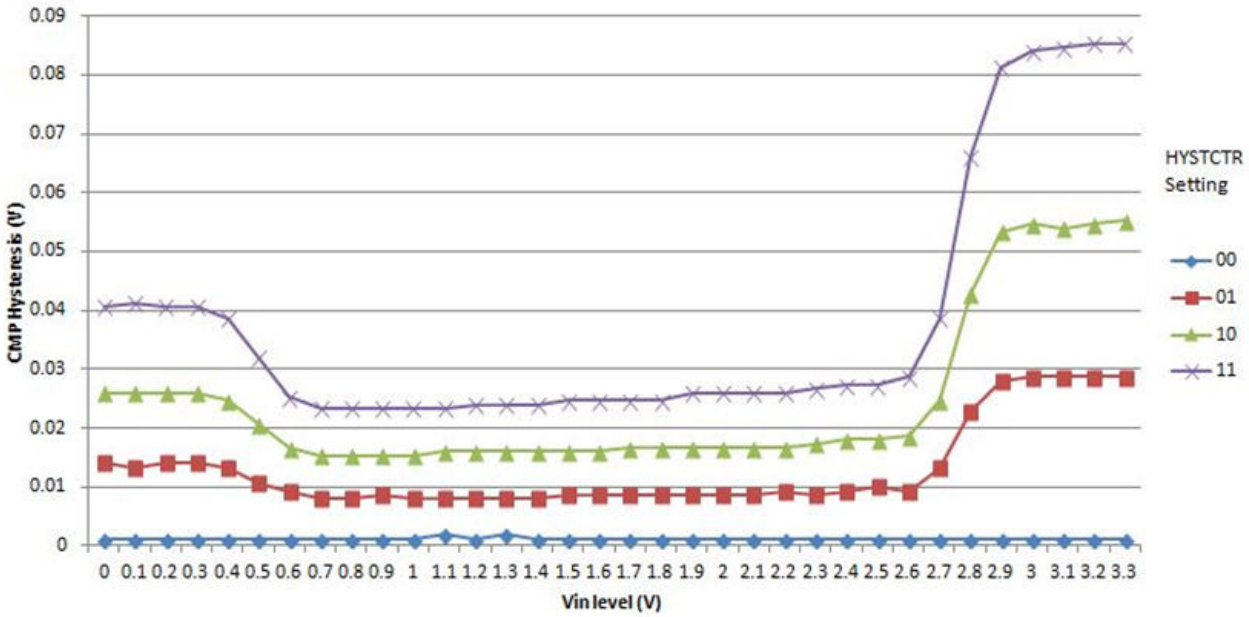


Figure 20. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

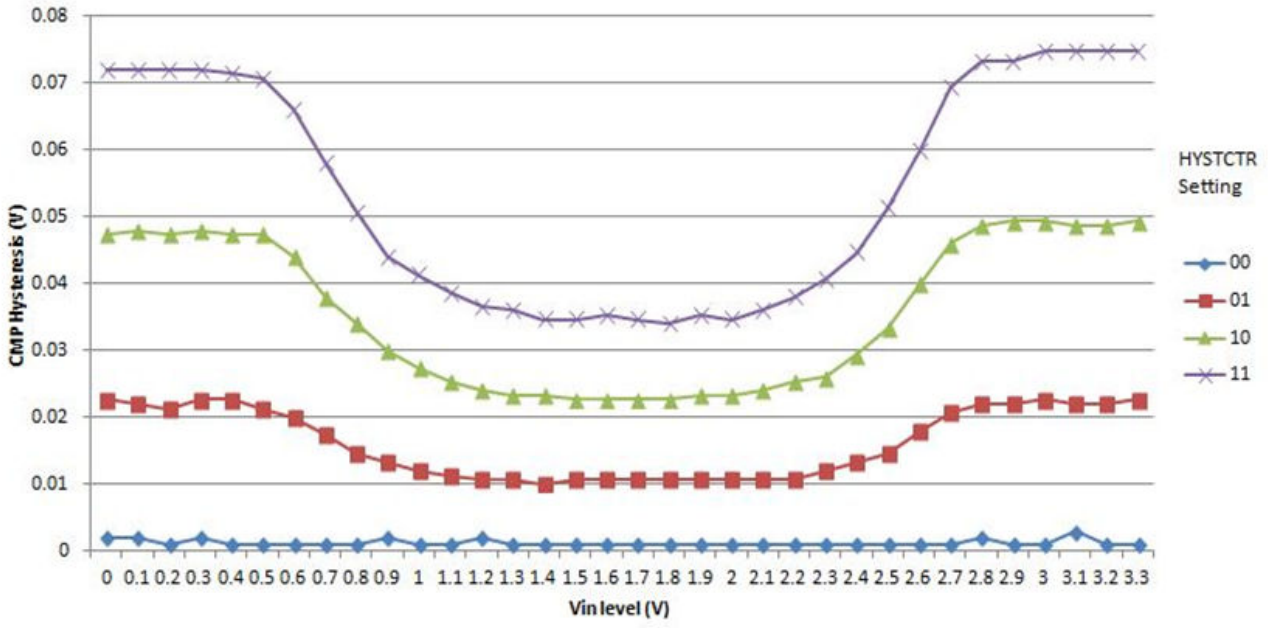


Figure 21. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

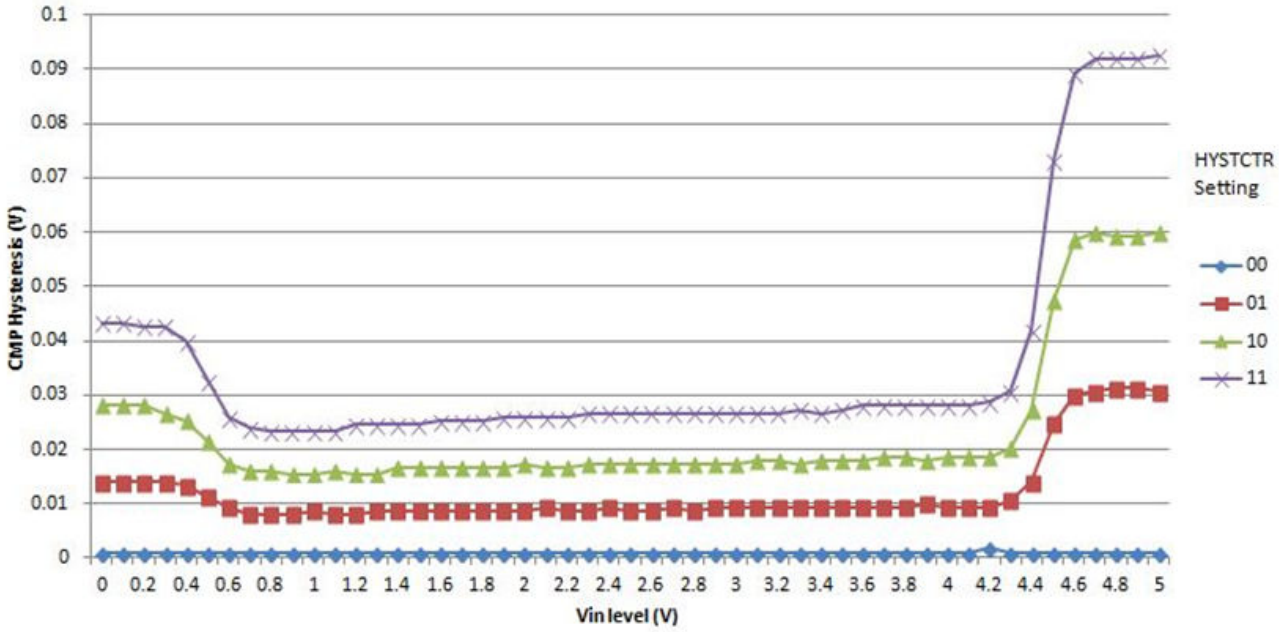


Figure 22. Typical hysteresis vs. Vin level (VDD = 5 V, PMODE = 0)

Do not add a pull-down resistor or capacitor on the NMI_b pin, because a low level on this pin will trigger non-maskable interrupt. When this pin is enabled as the NMI function, an external pull-up resistor (10 kΩ) as shown in the following figure is recommended for robustness.

If the NMI_b pin is used as an I/O pin, the non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.

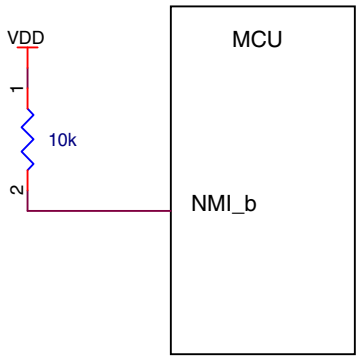


Figure 38. NMI pin biasing

- Debug interface

  This MCU uses the standard ARM SWD interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD_DIO has an internal pull-up and SWD_CLK has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The RESET_b pin recommendations mentioned above must also be considered.

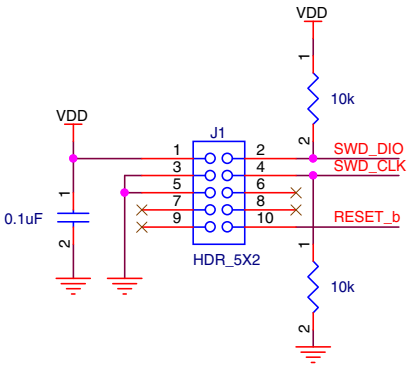


Figure 39. SWD debug interface

- Unused pin

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